# Active Access: A Mechanism for High-Performance Distributed Data-Centric Computations

MACIEJ BESTA, TORSTEN HOEFLER

# REMOTE MEMORY ACCESS (RMA) PROGRAMMING

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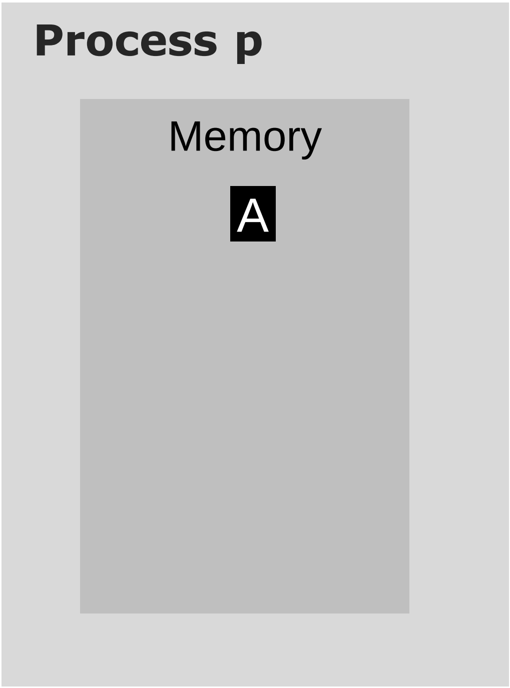

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A

**Process q**

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Cray BlueWaters

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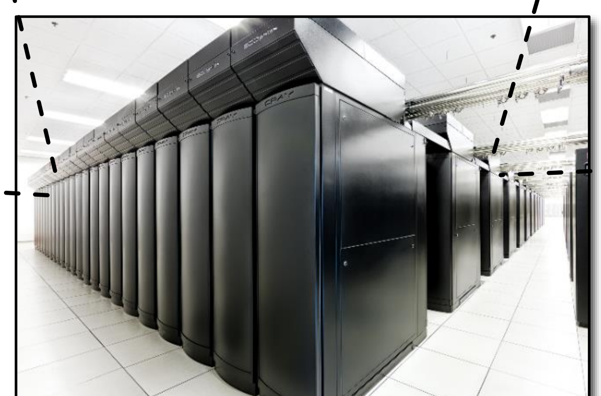

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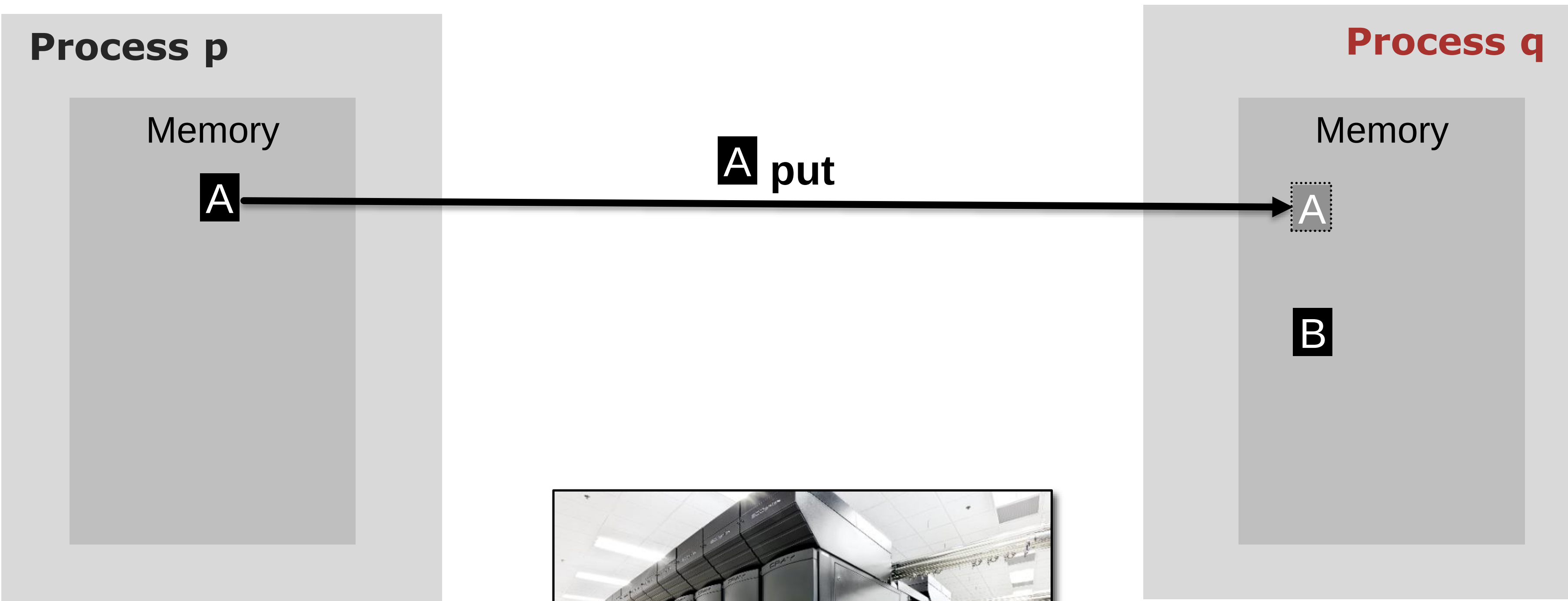


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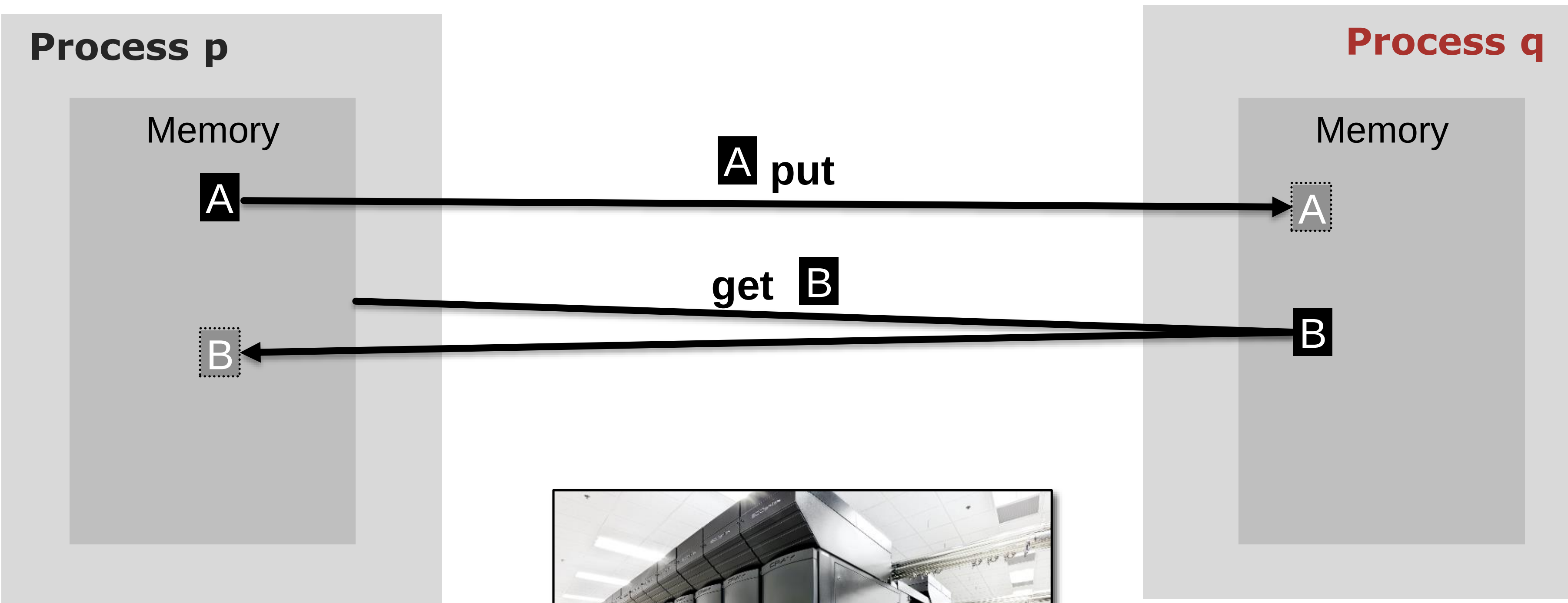


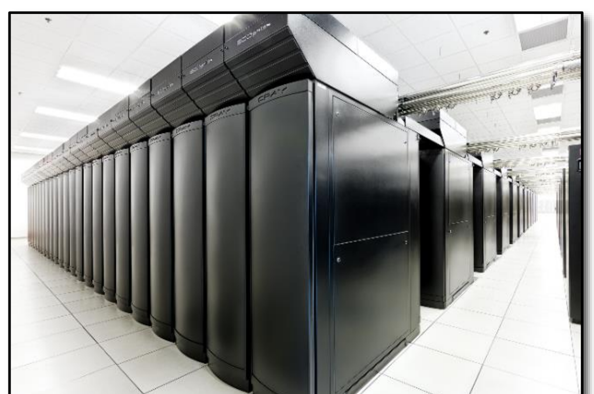

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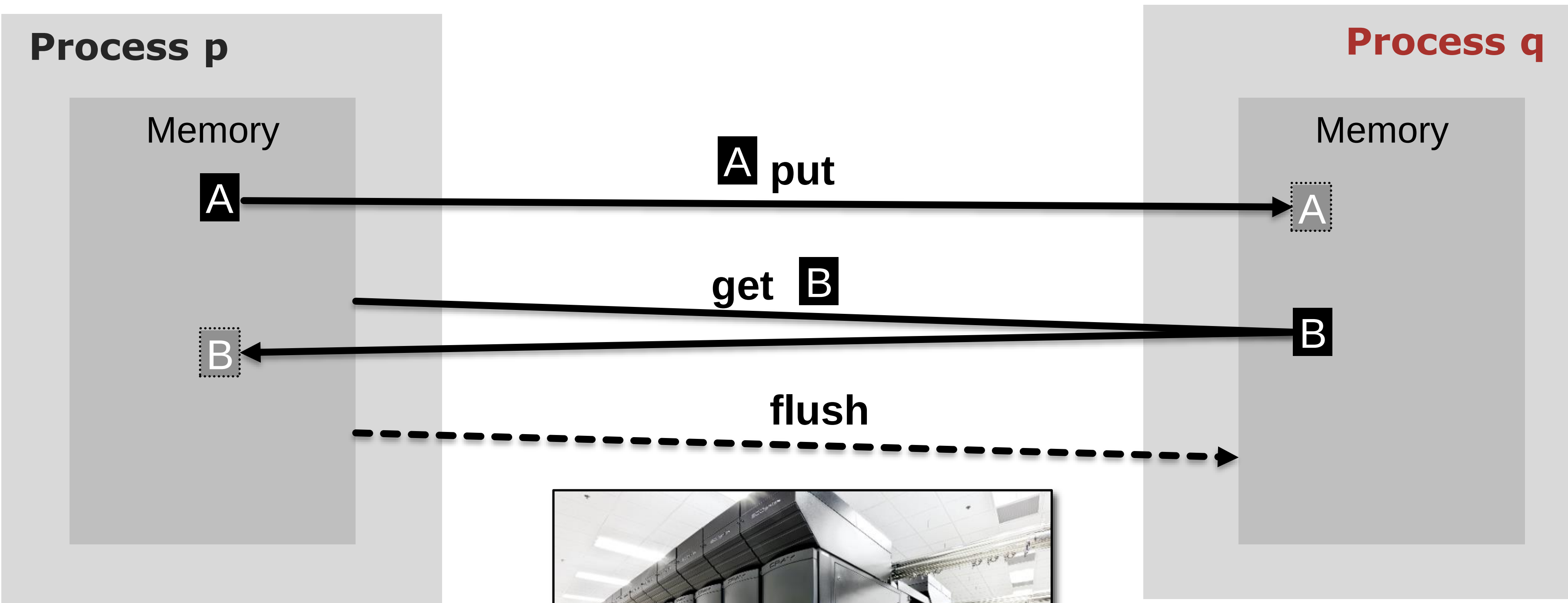


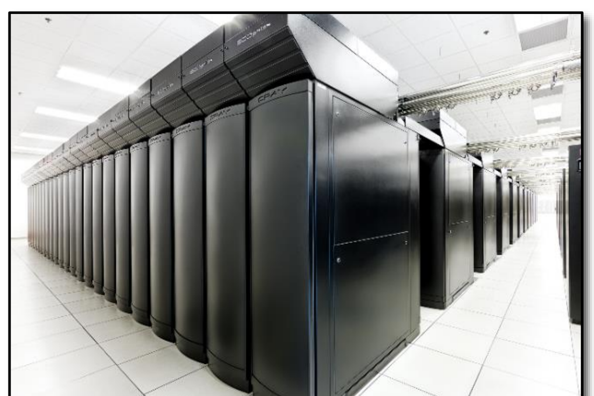

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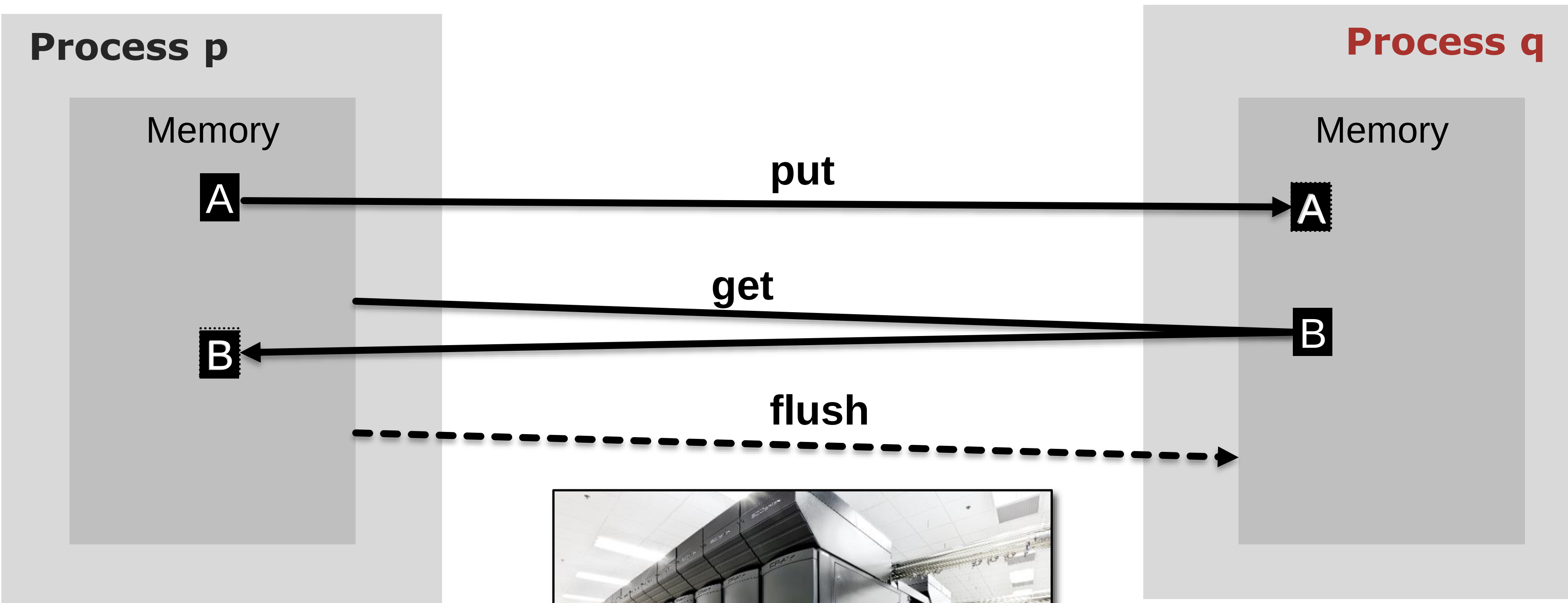


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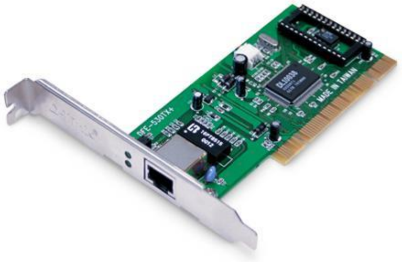

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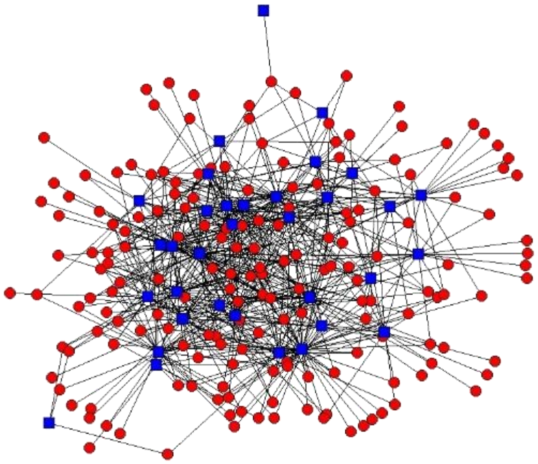

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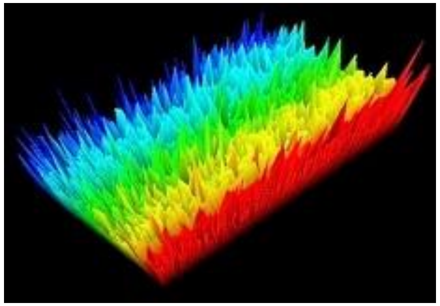

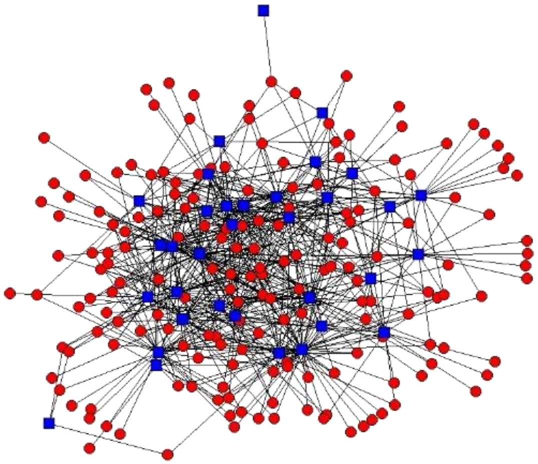

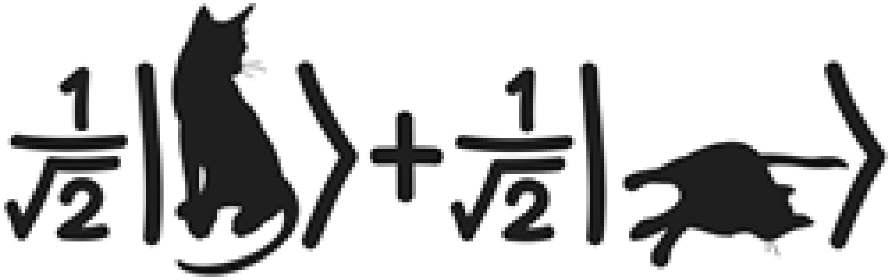

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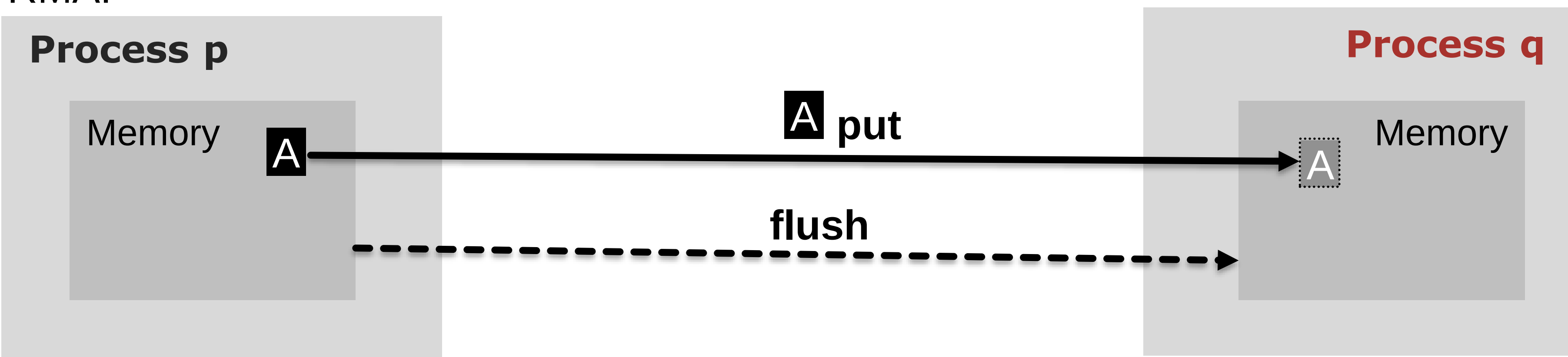

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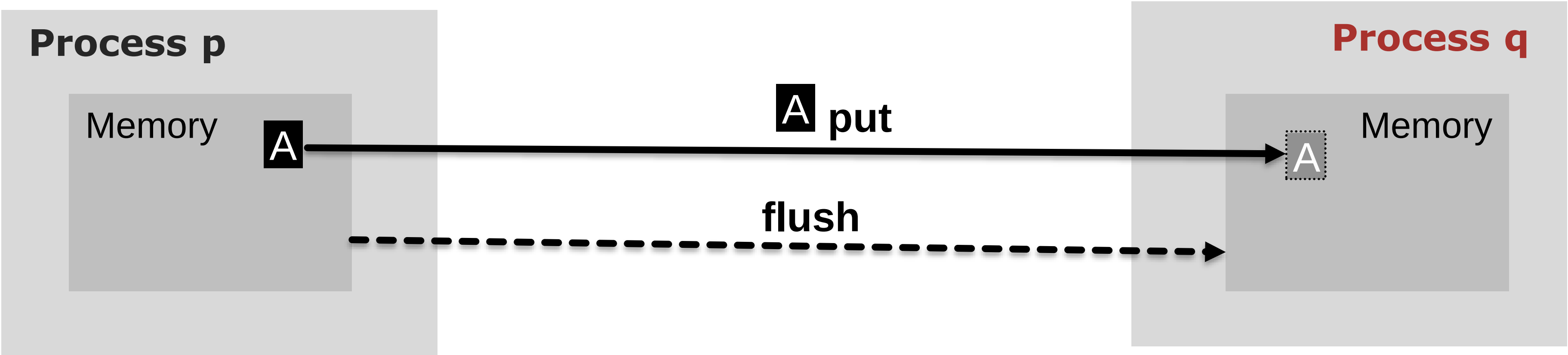


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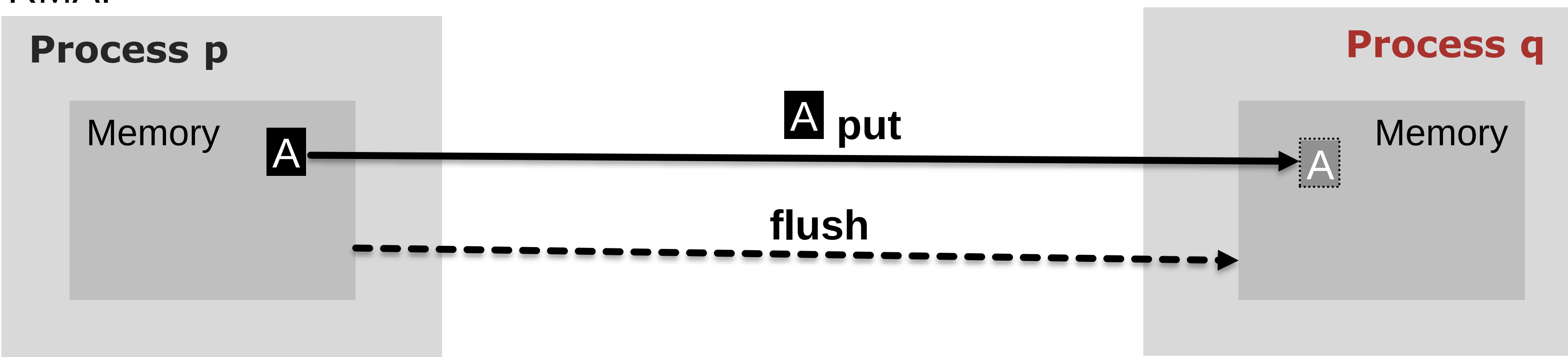


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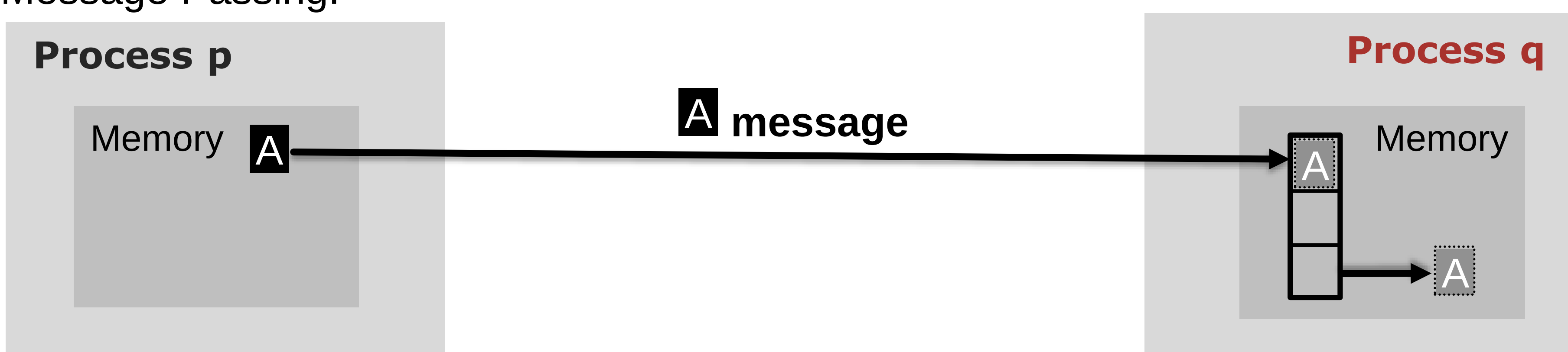

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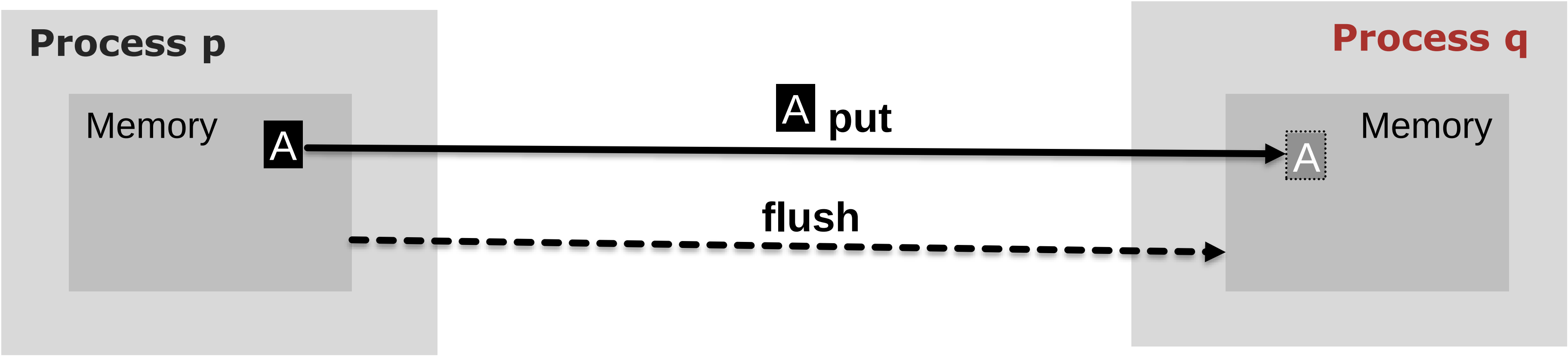


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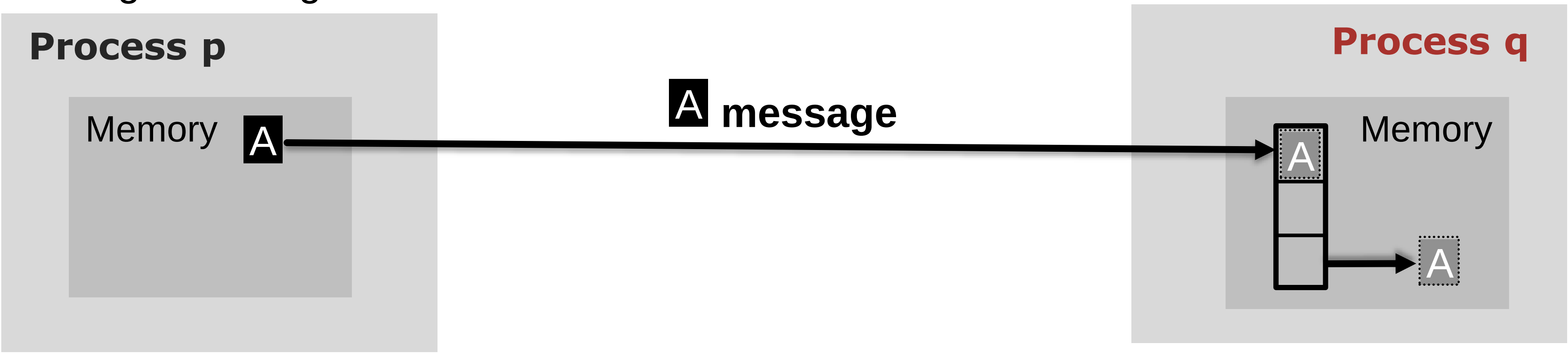

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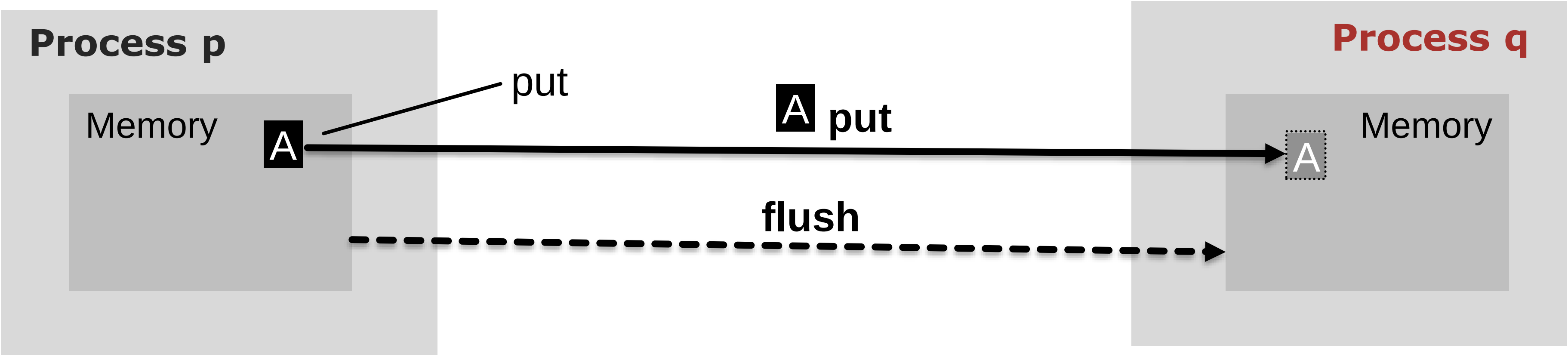


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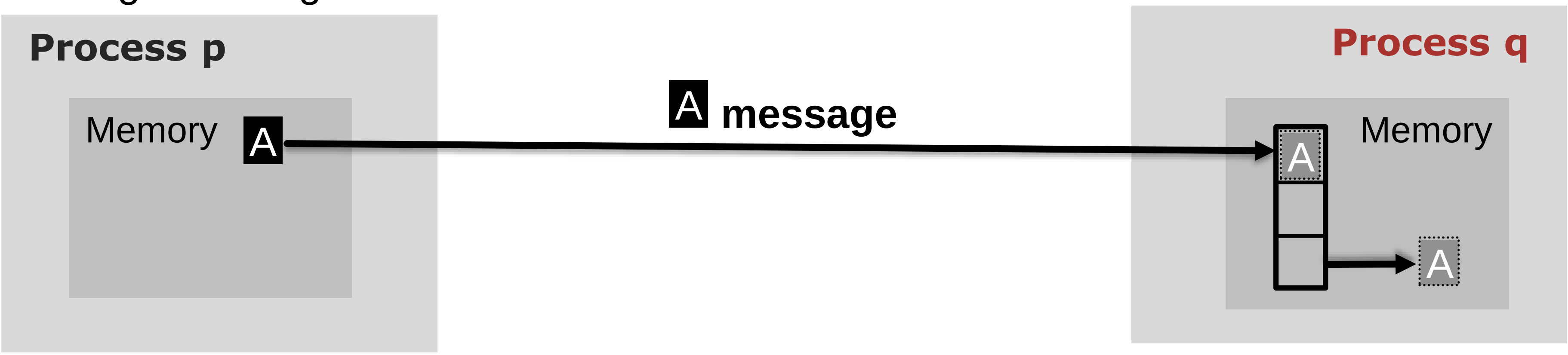

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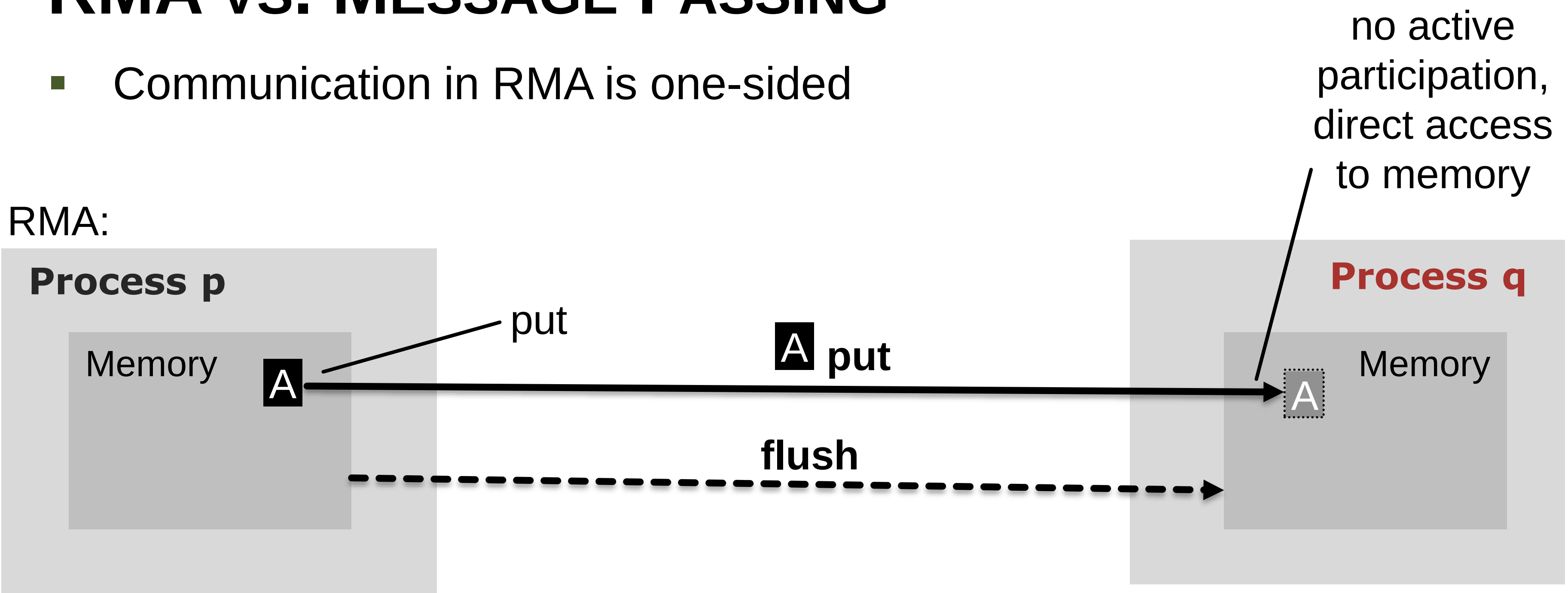


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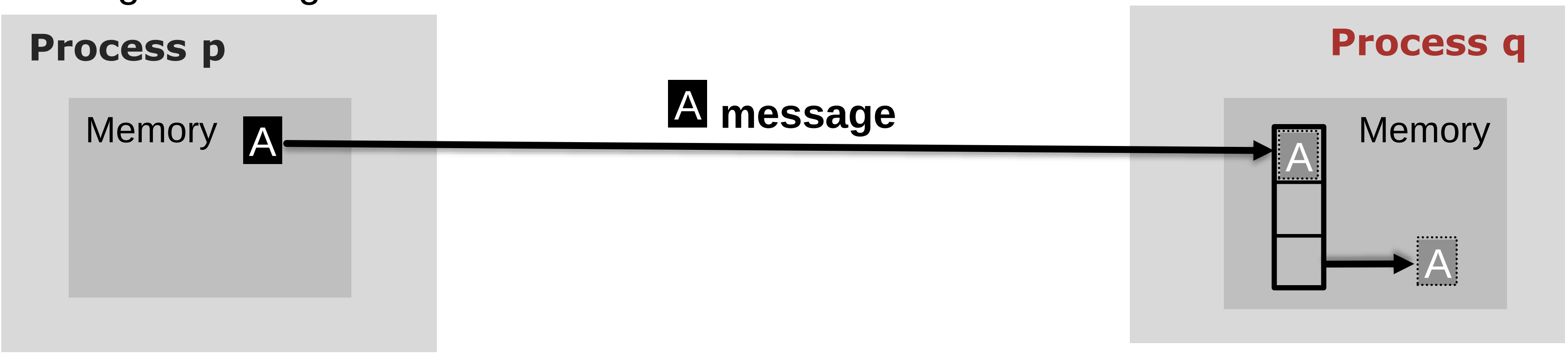

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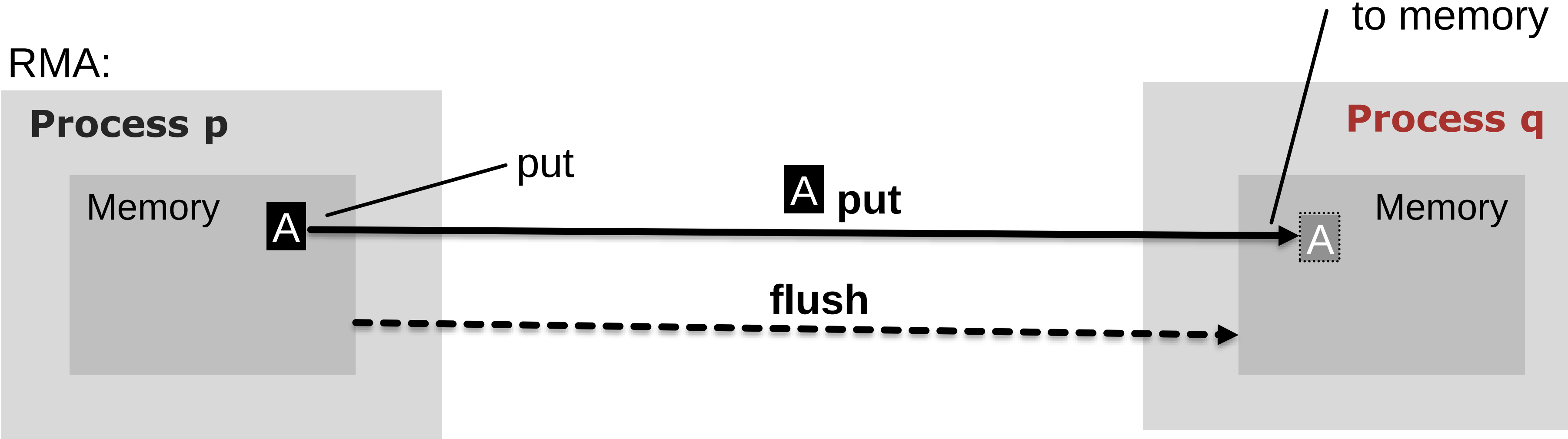


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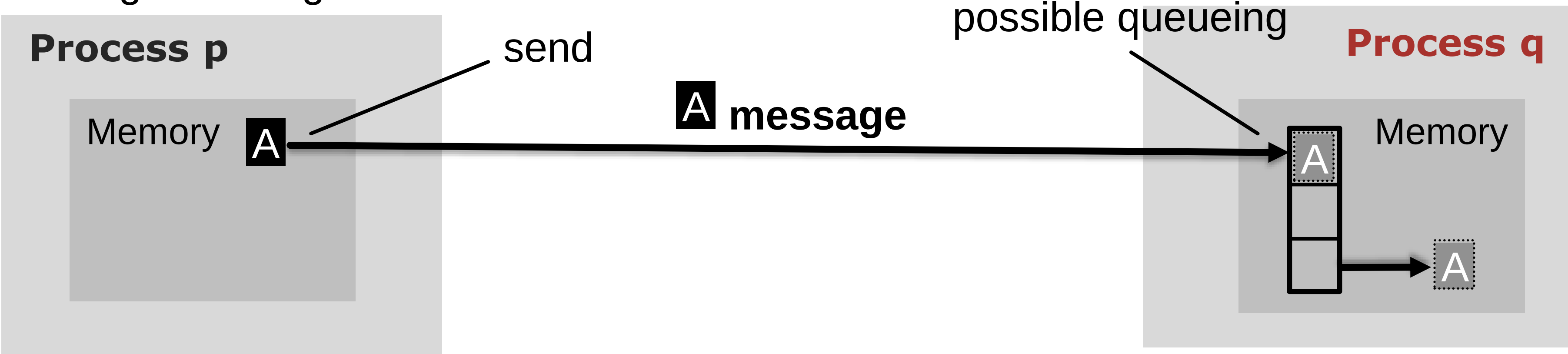

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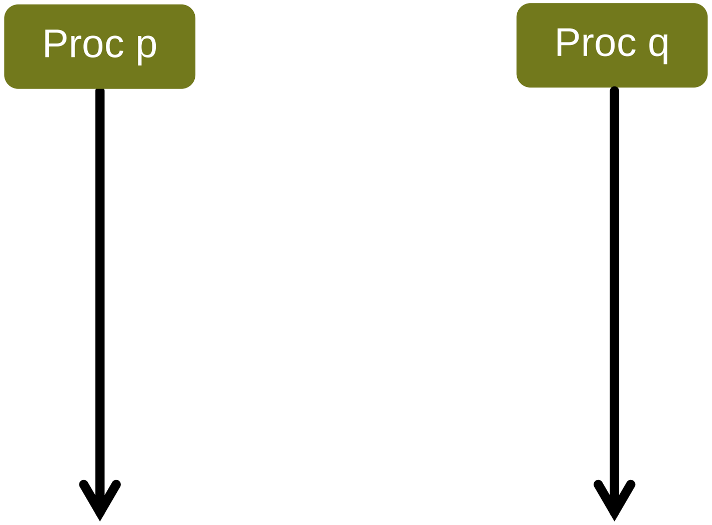


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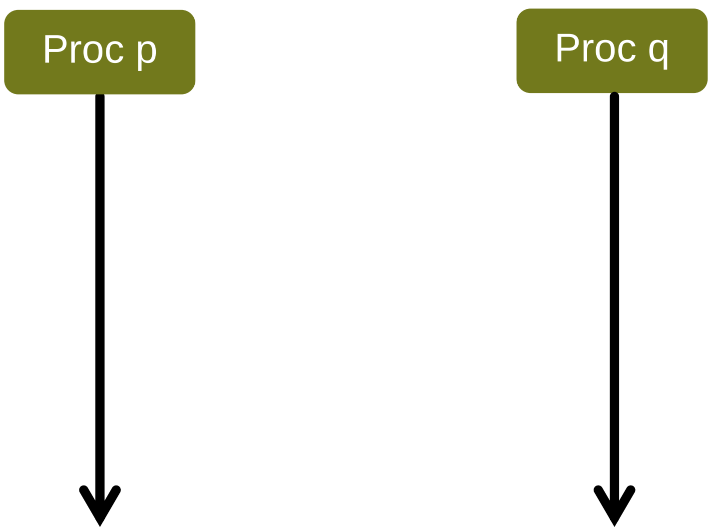


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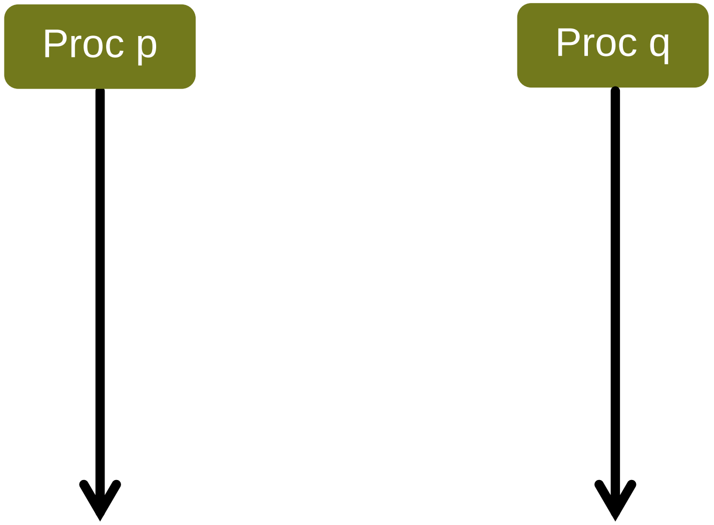


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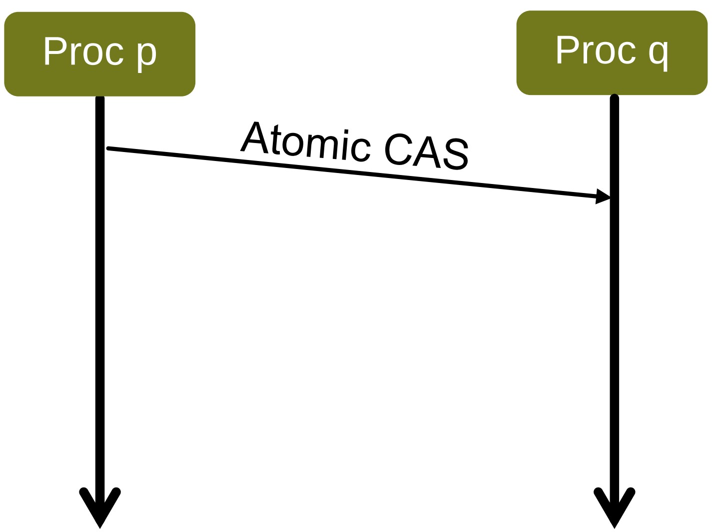


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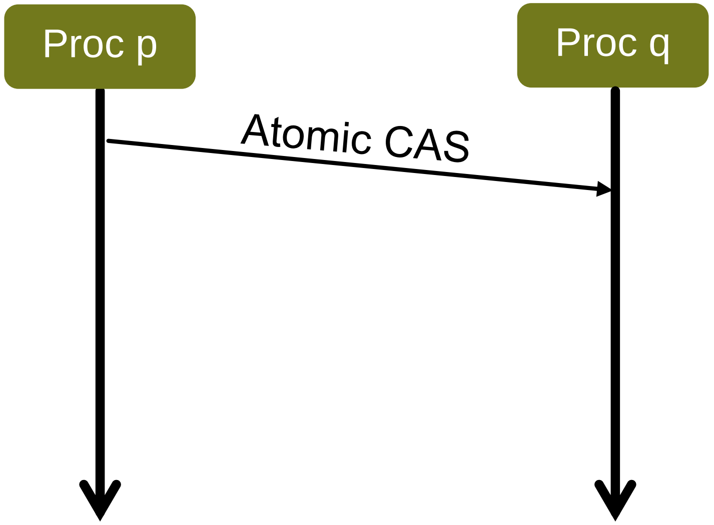


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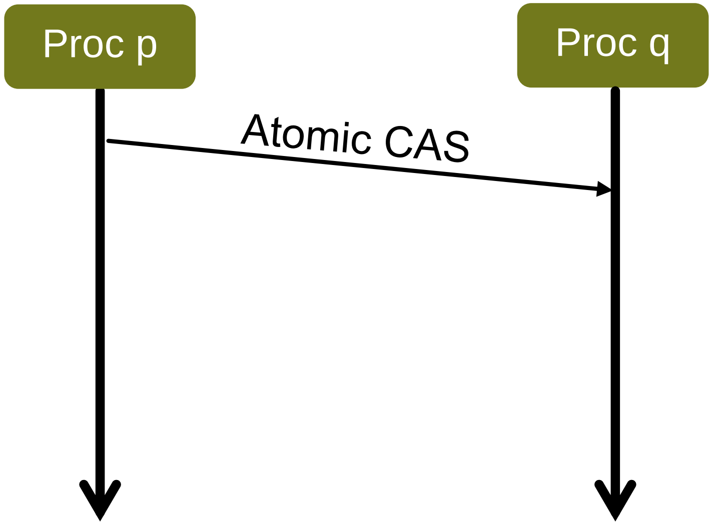


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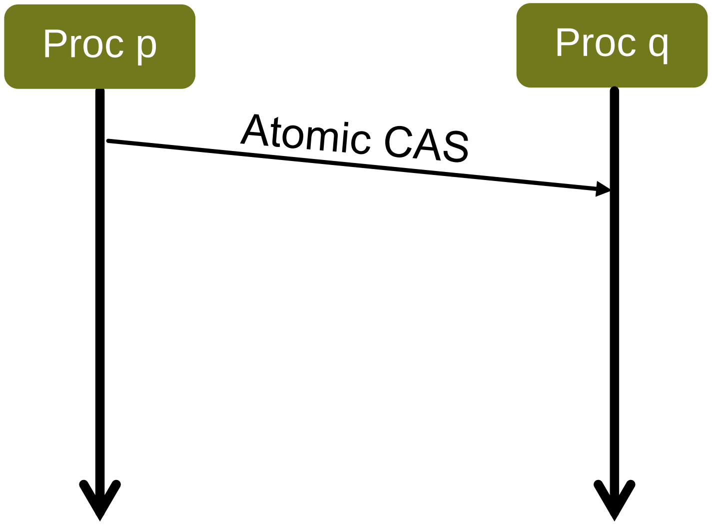


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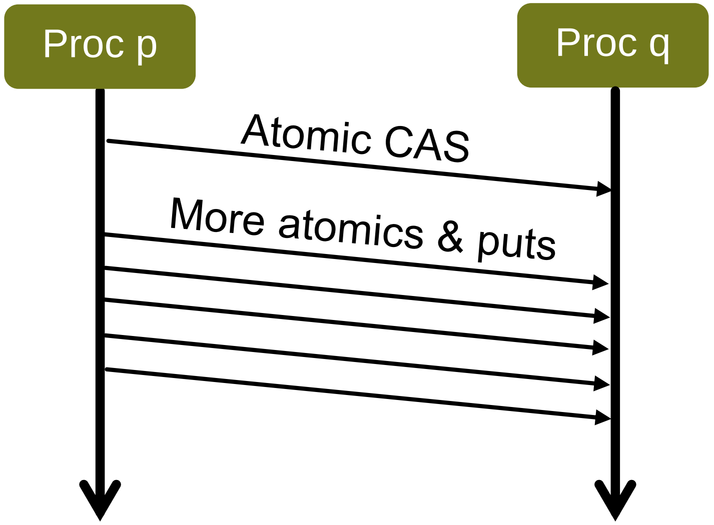


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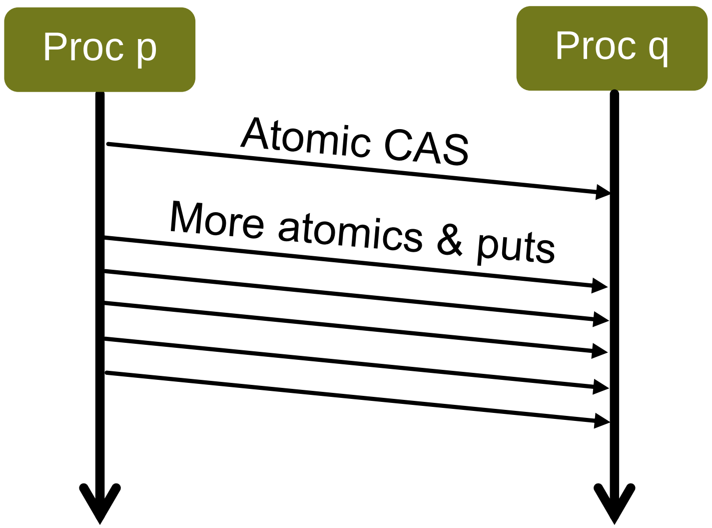


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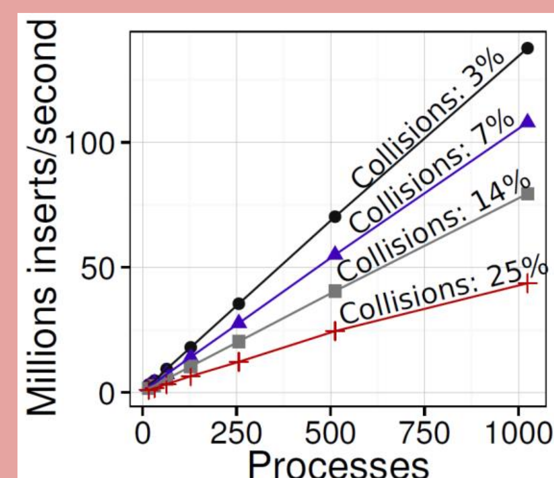


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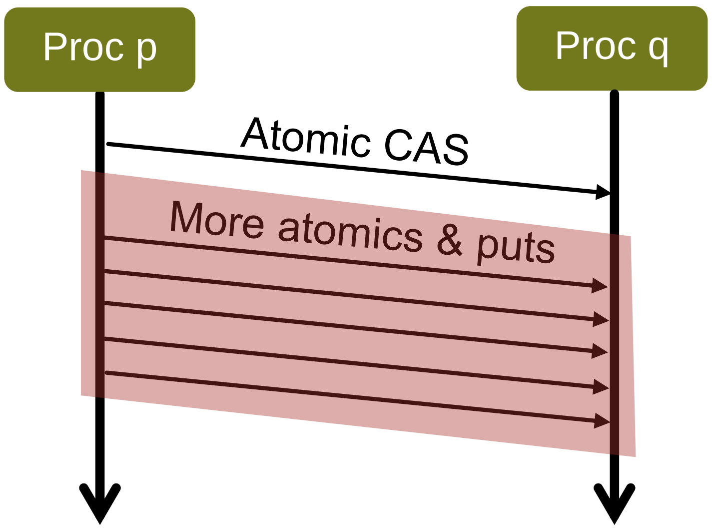


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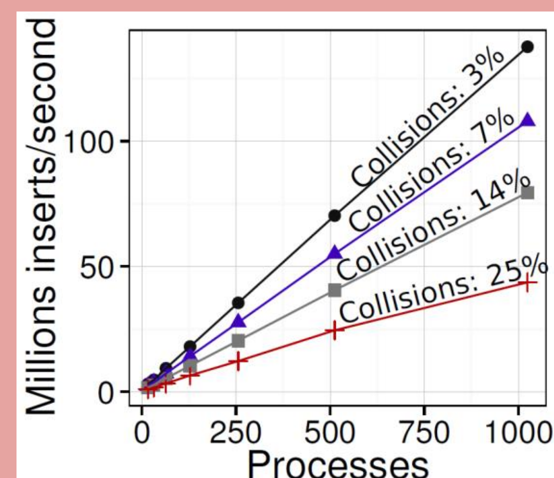


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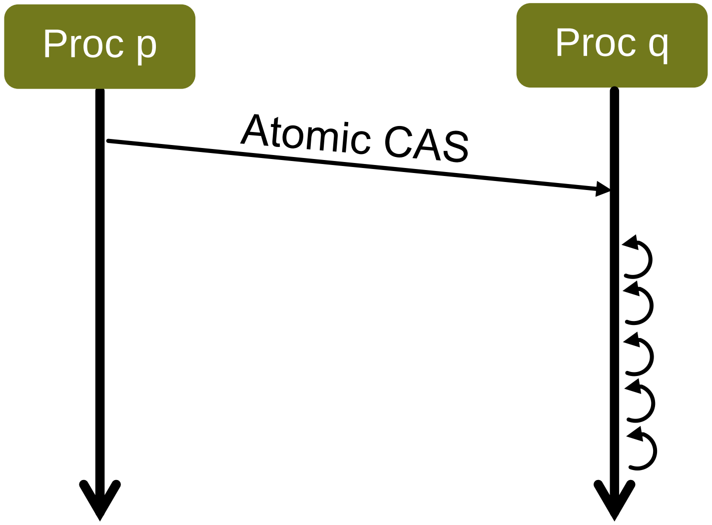


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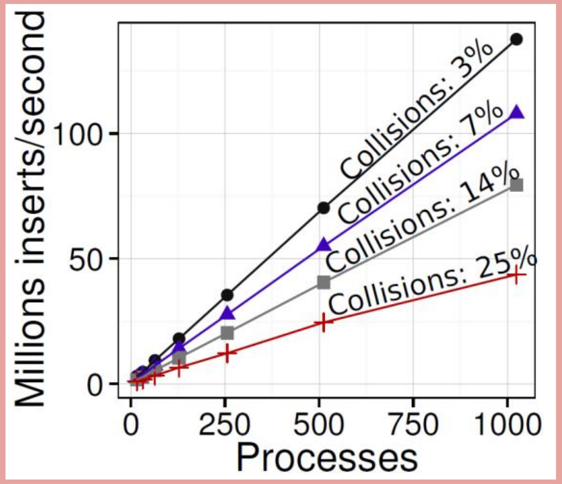


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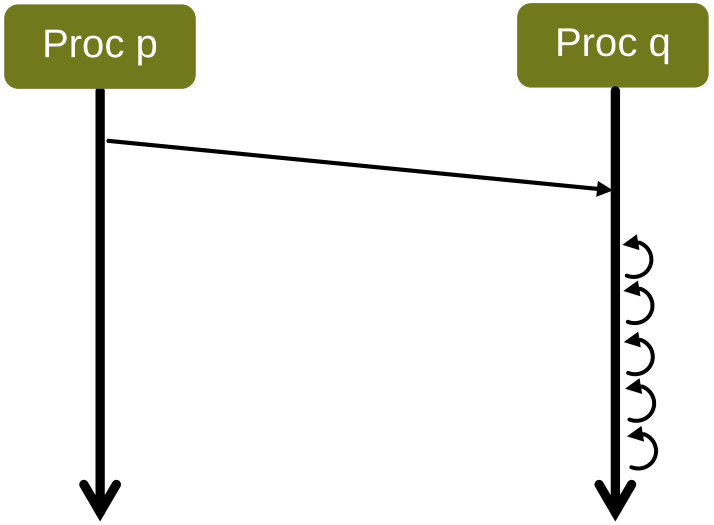


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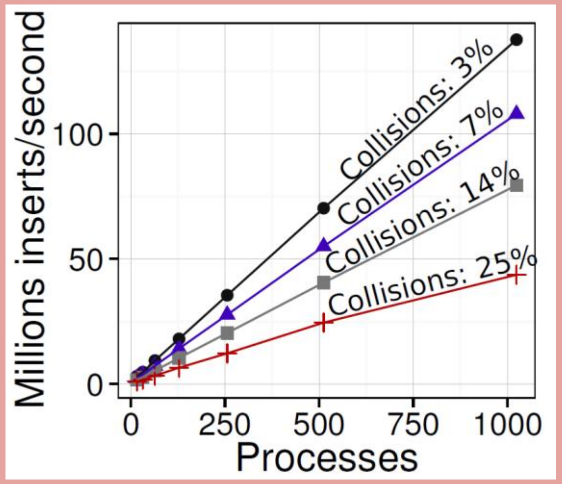


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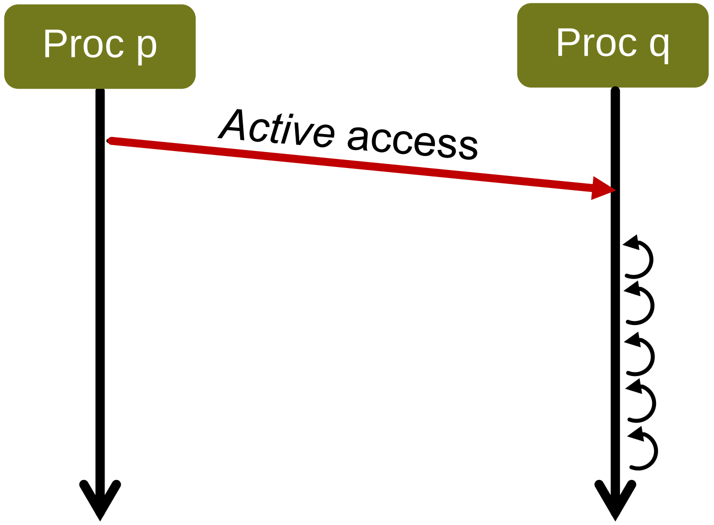


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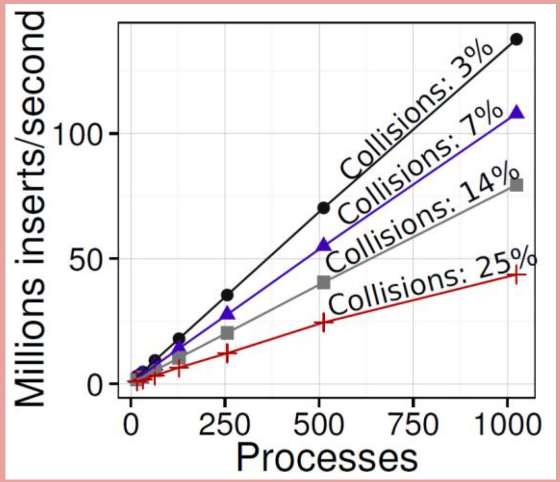


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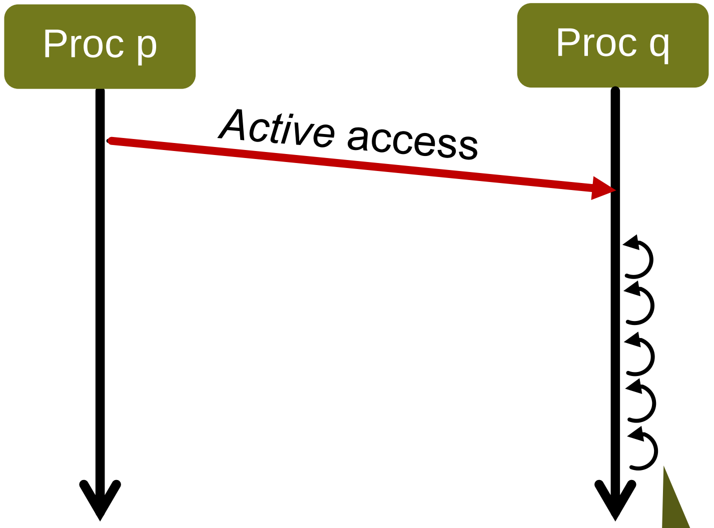


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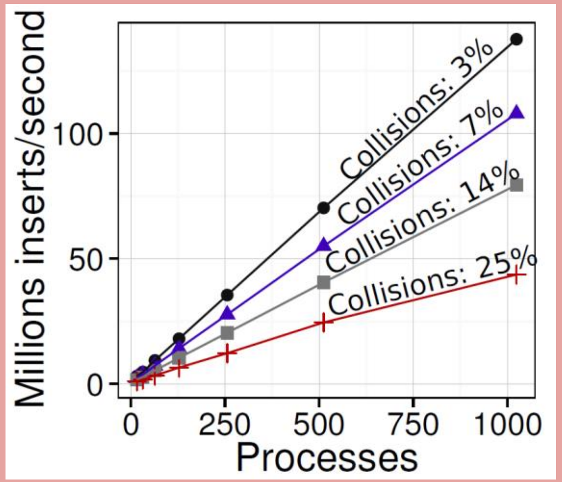


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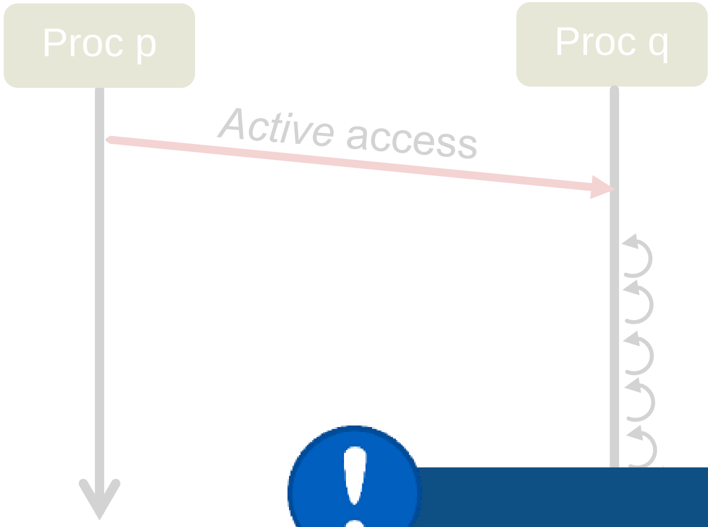


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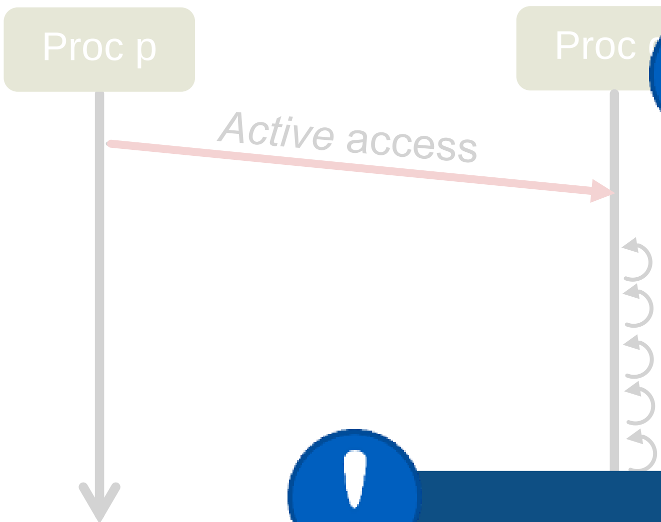


Use and extend I/O MMUs and their paging capabilities

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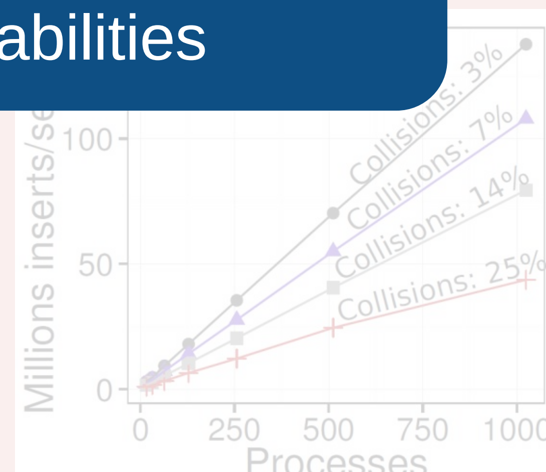


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# USE SEMANTICS FROM ACTIVE MESSAGES (AM) [1]

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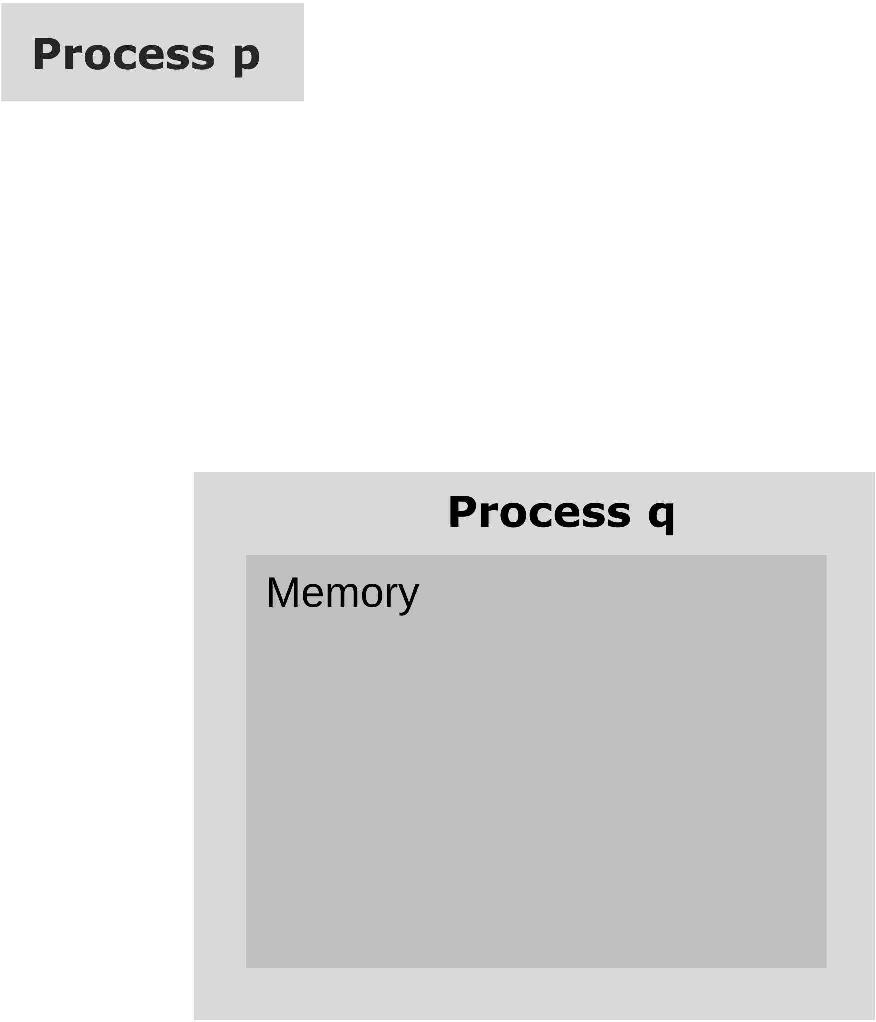
# USE SEMANTICS FROM ACTIVE MESSAGES (AM) [1]

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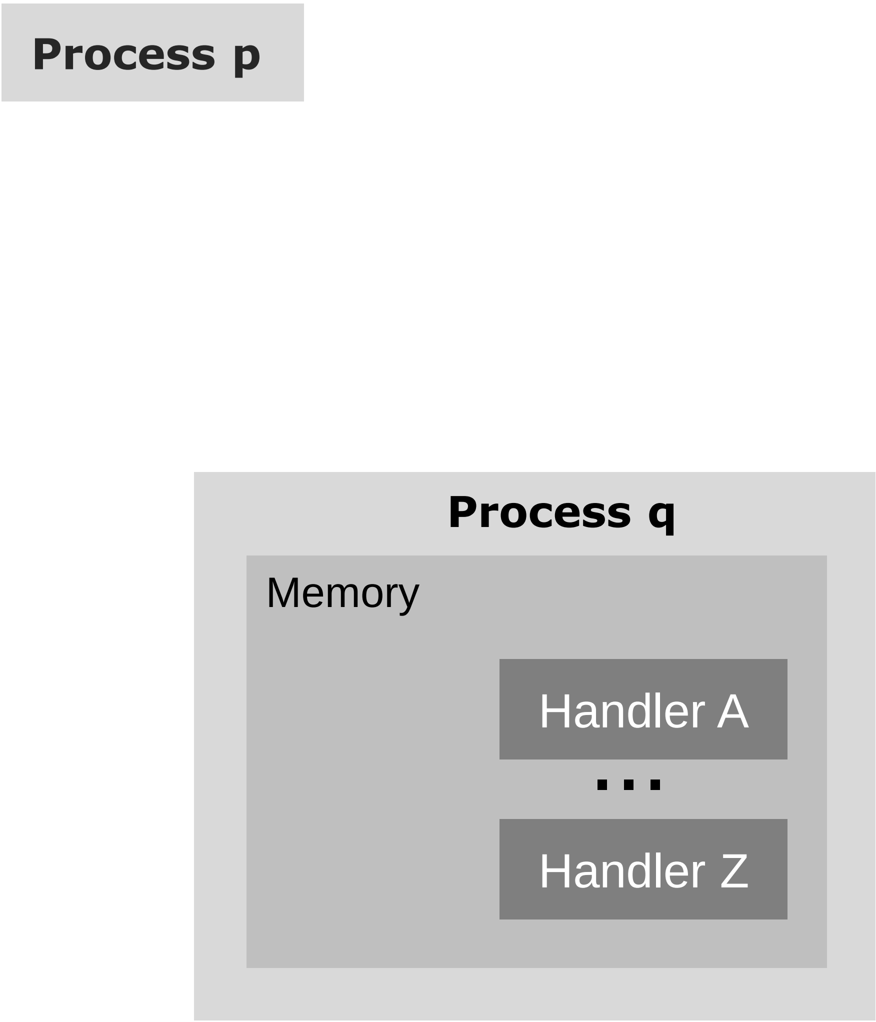


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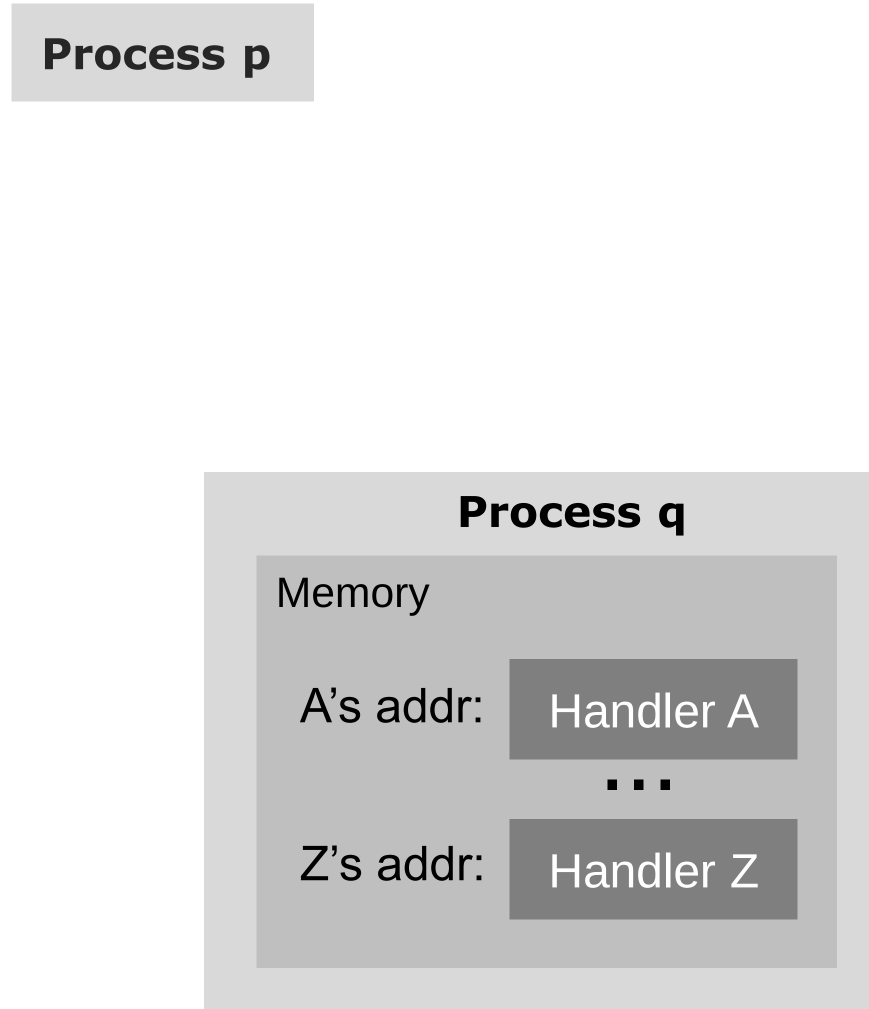


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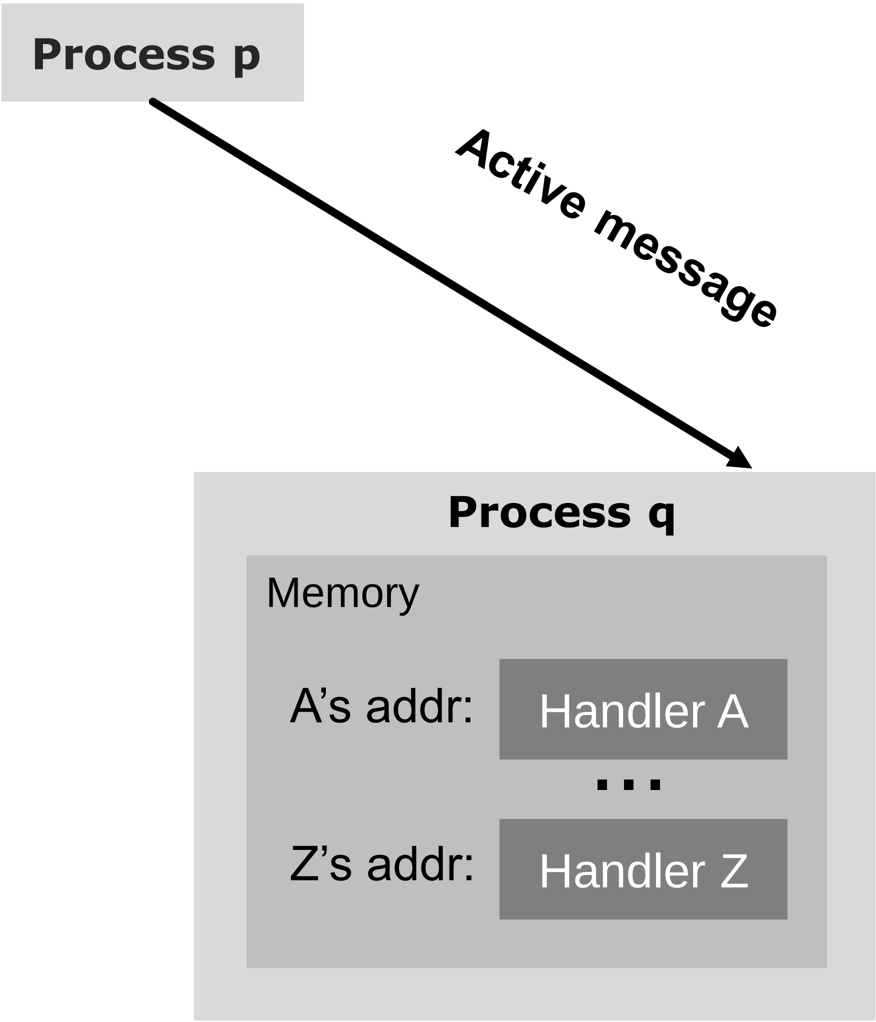


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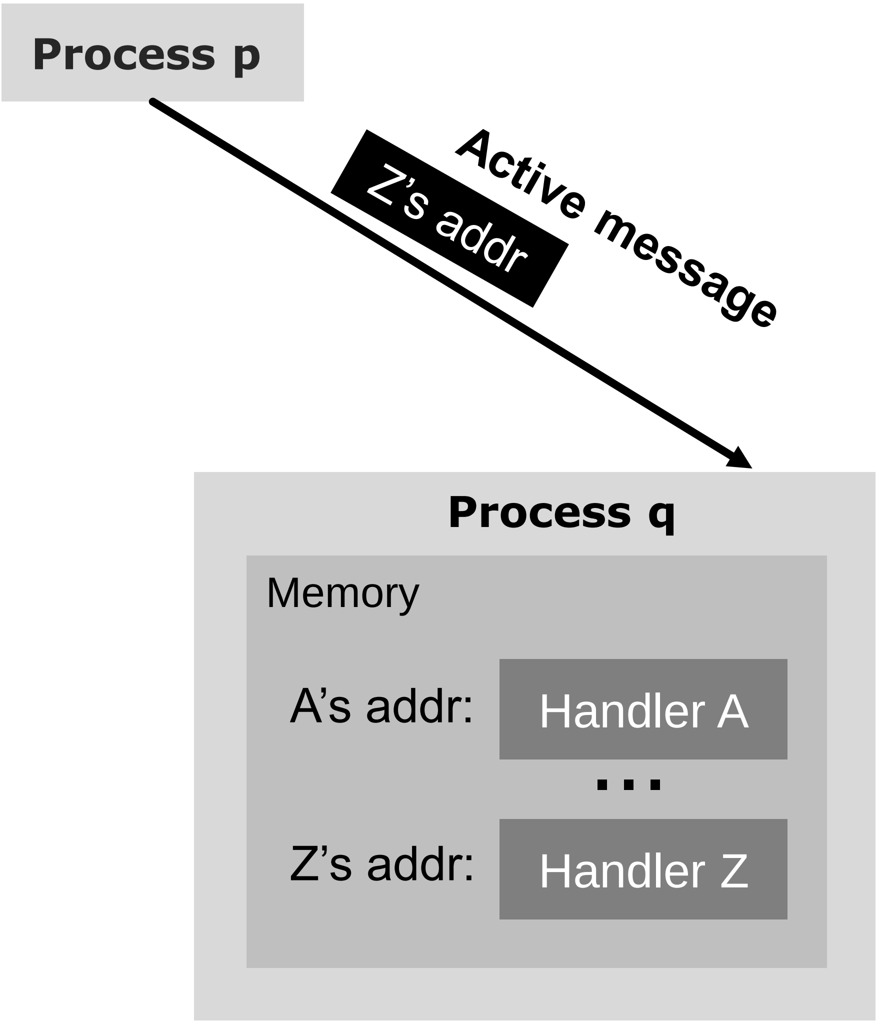


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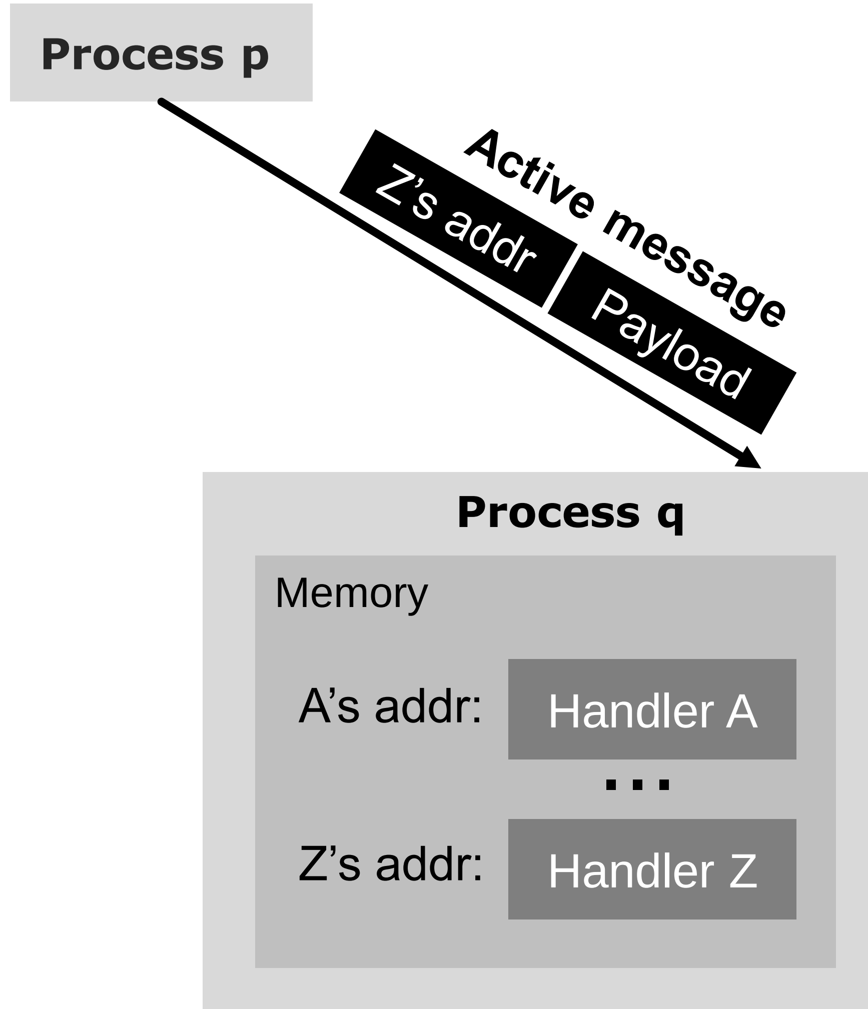


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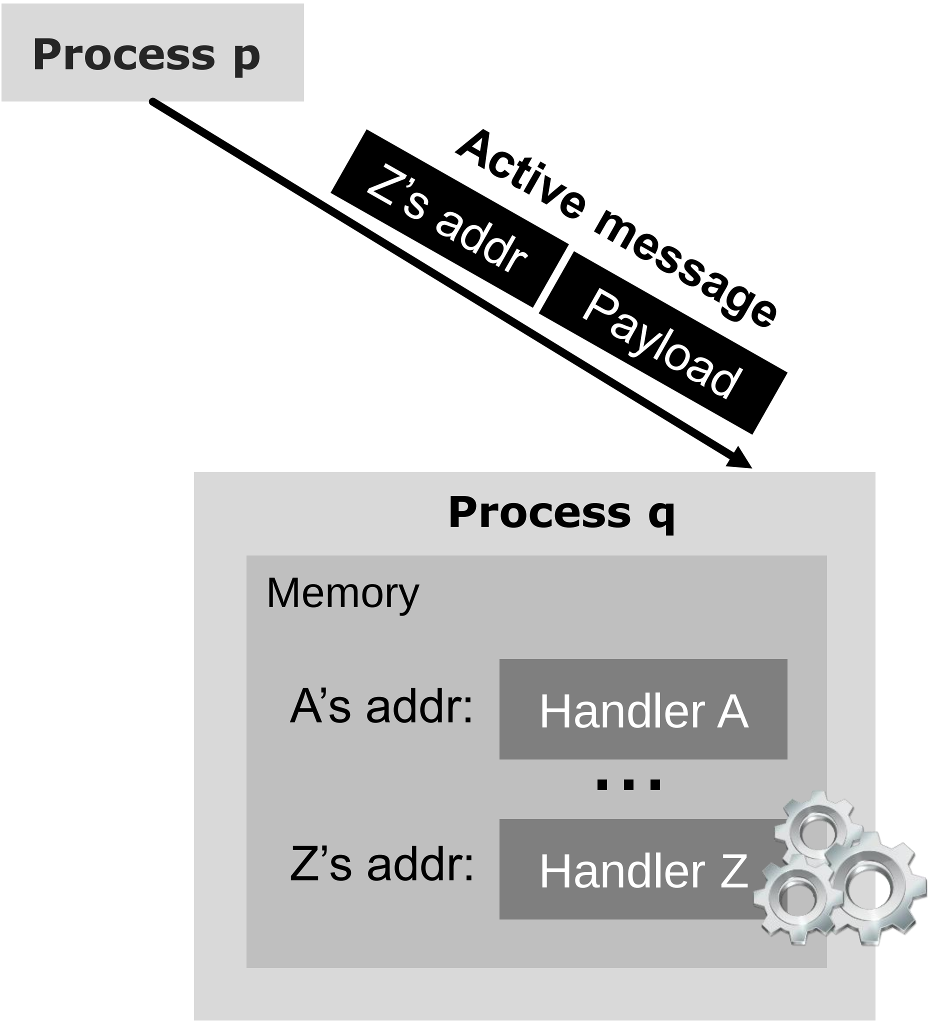


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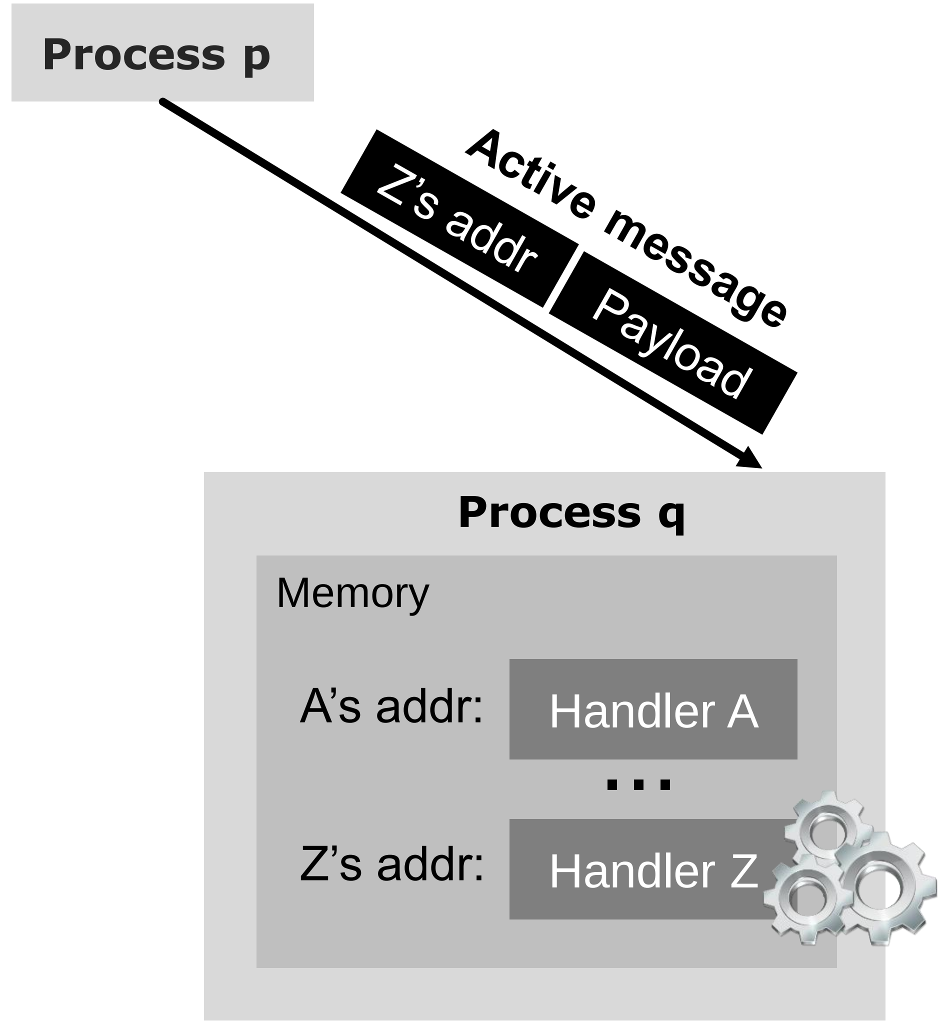


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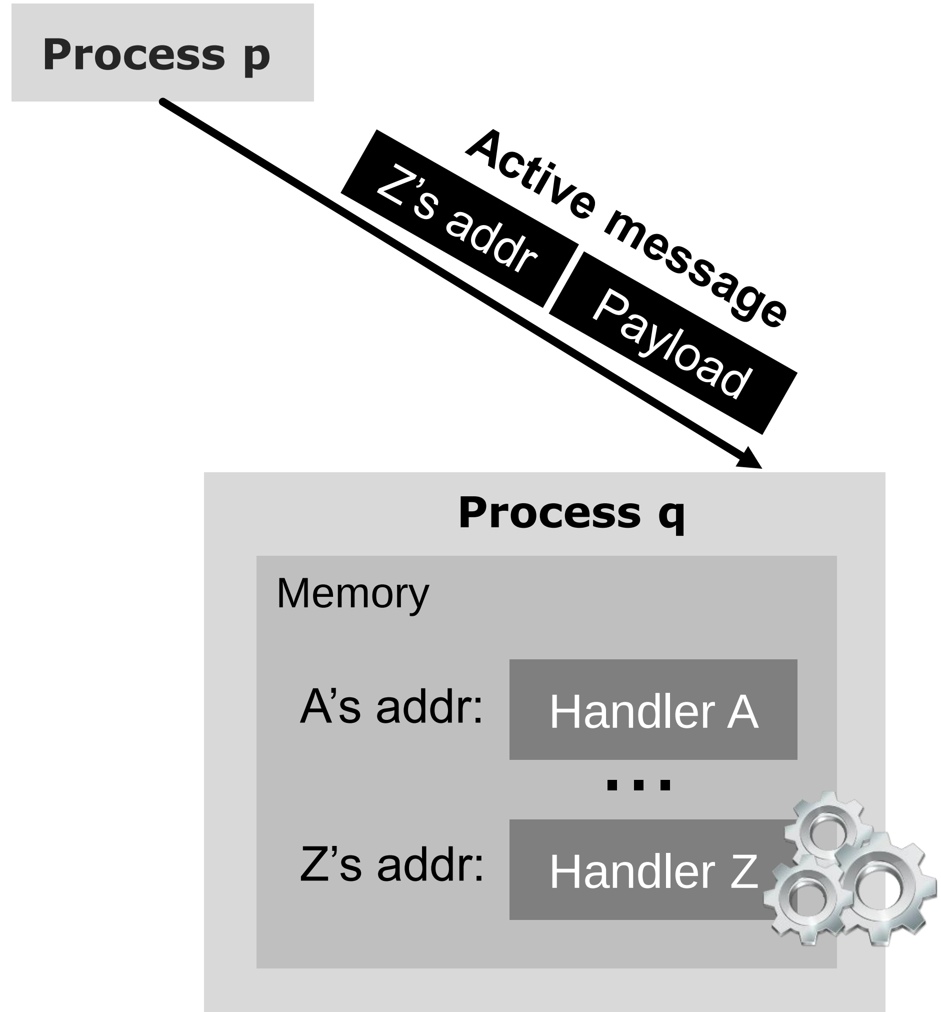


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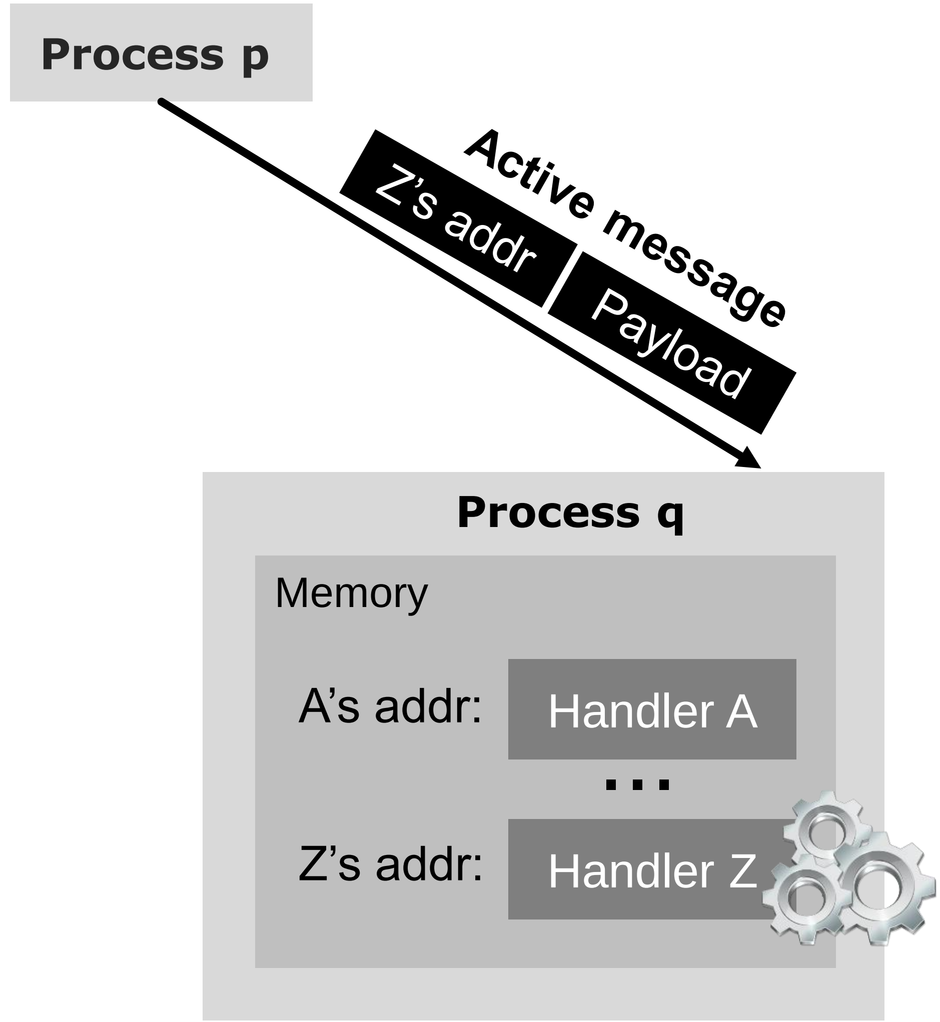
# USE SEMANTICS FROM ACTIVE MESSAGES (AM) [1]


AM++[2]
GASNet [3]

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# USE SEMANTICS FROM ACTIVE MESSAGES (AM) [1]

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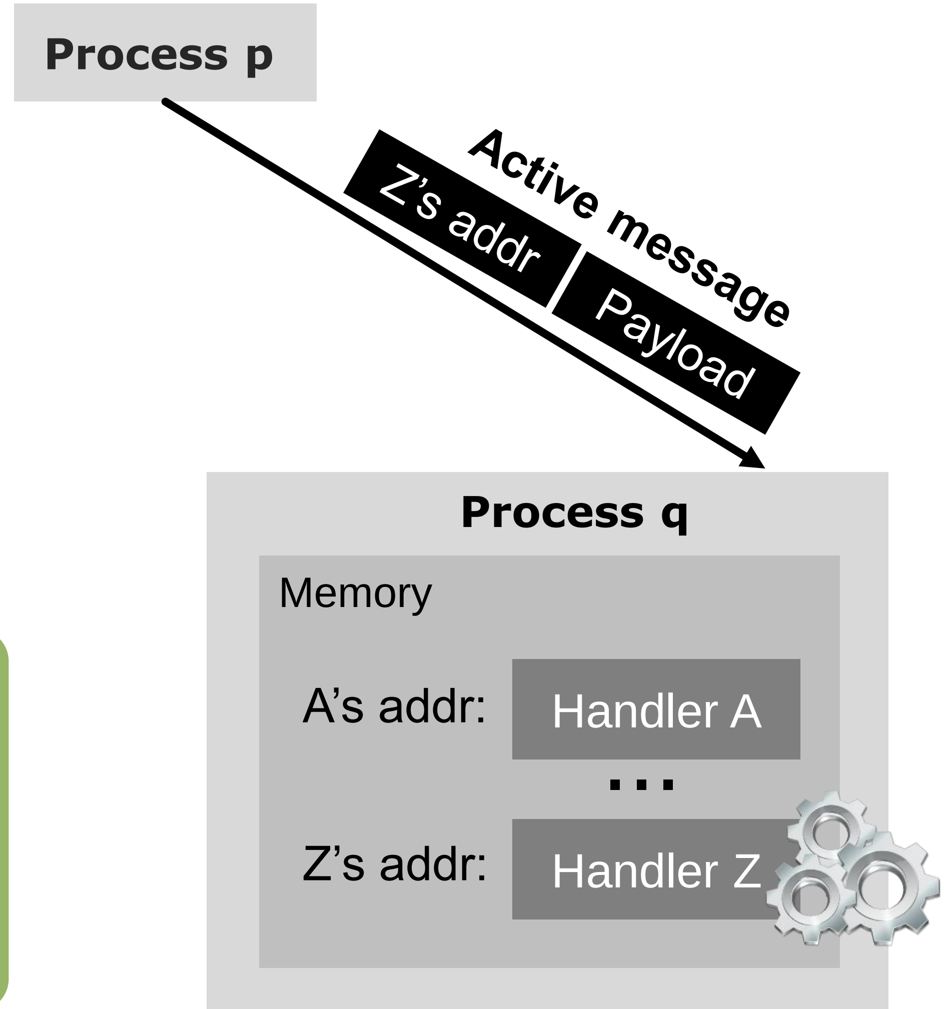
We need *active* puts/gets:

- Invoke a handler upon accessing a given page
- Preserve one-sided RMA behavior

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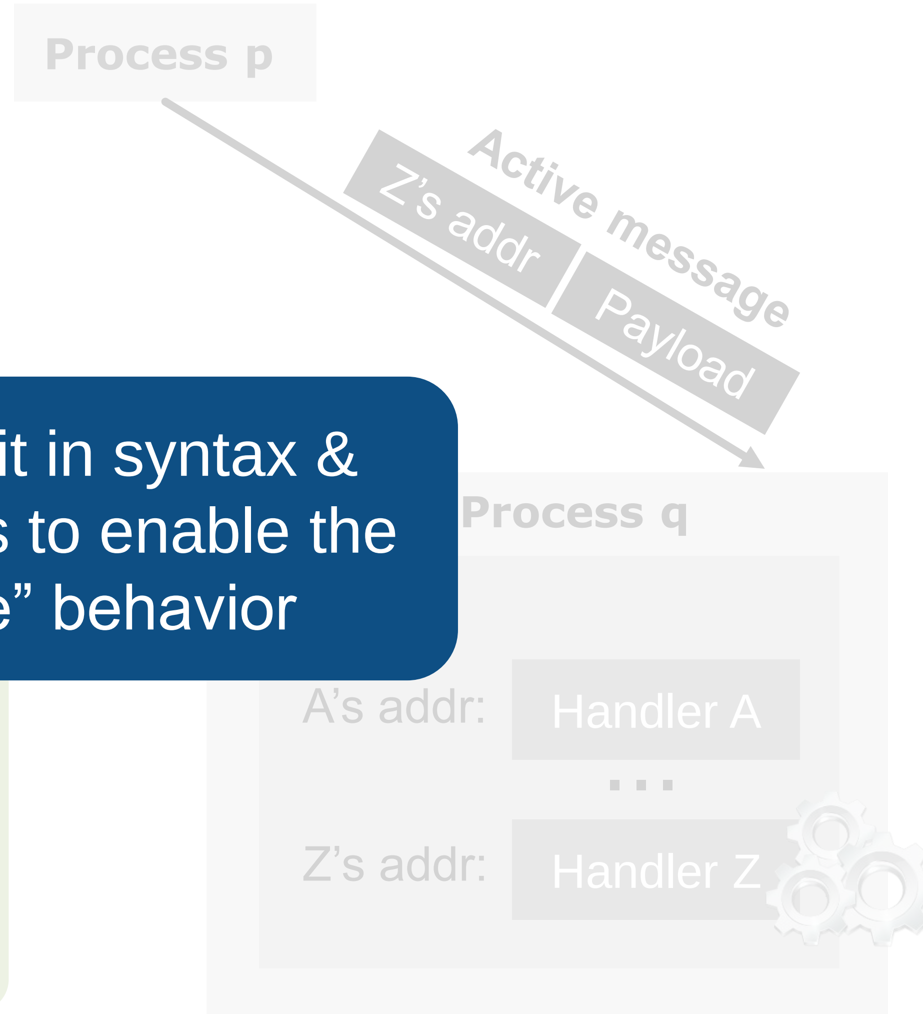


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**We use it in syntax & semantics to enable the "active" behavior**

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# Use Input/Output Memory Management Units

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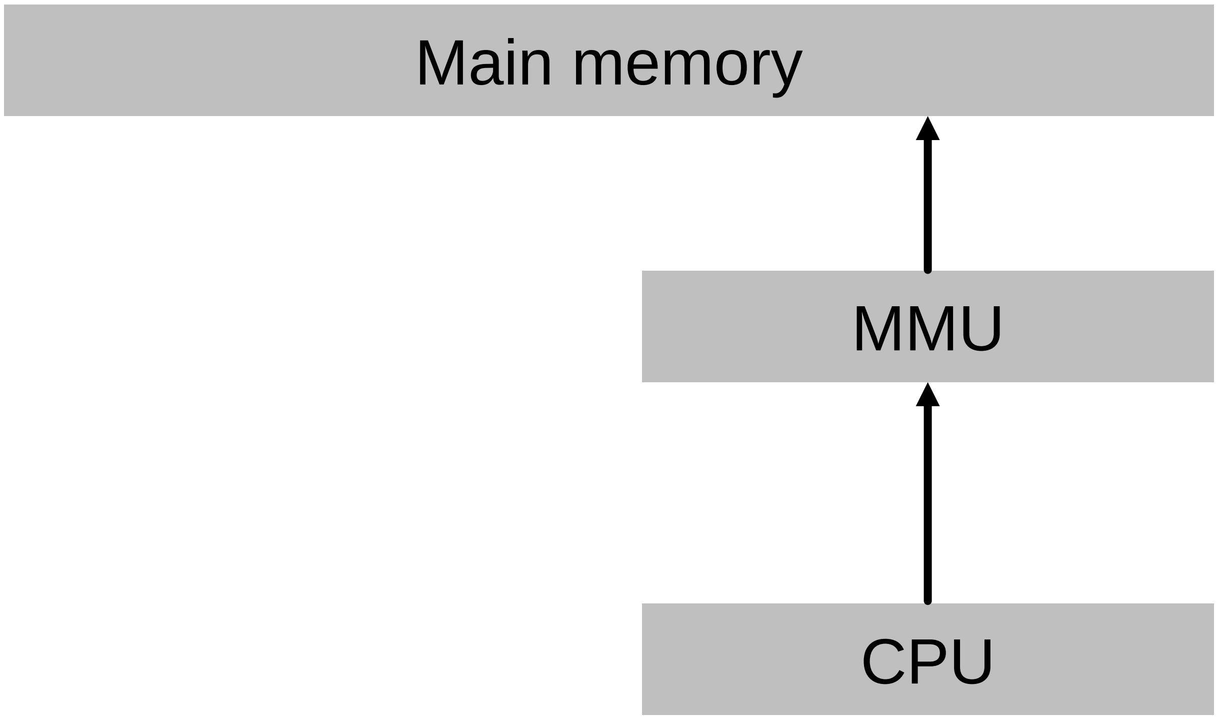

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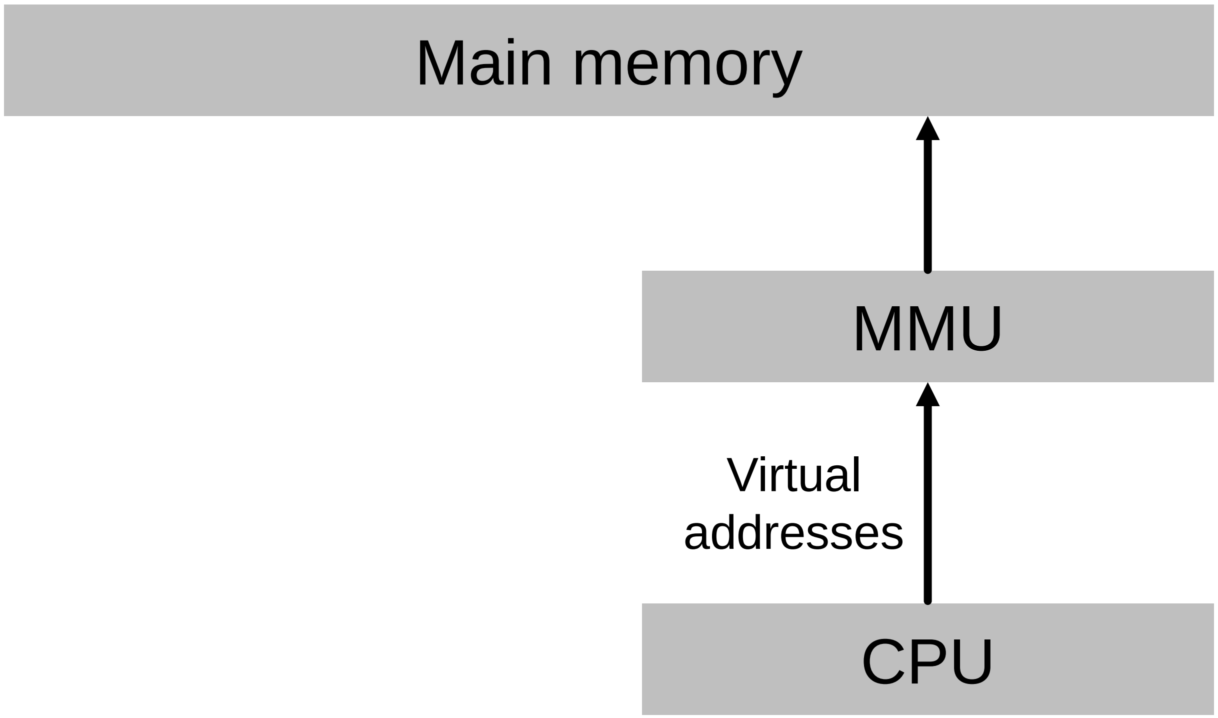

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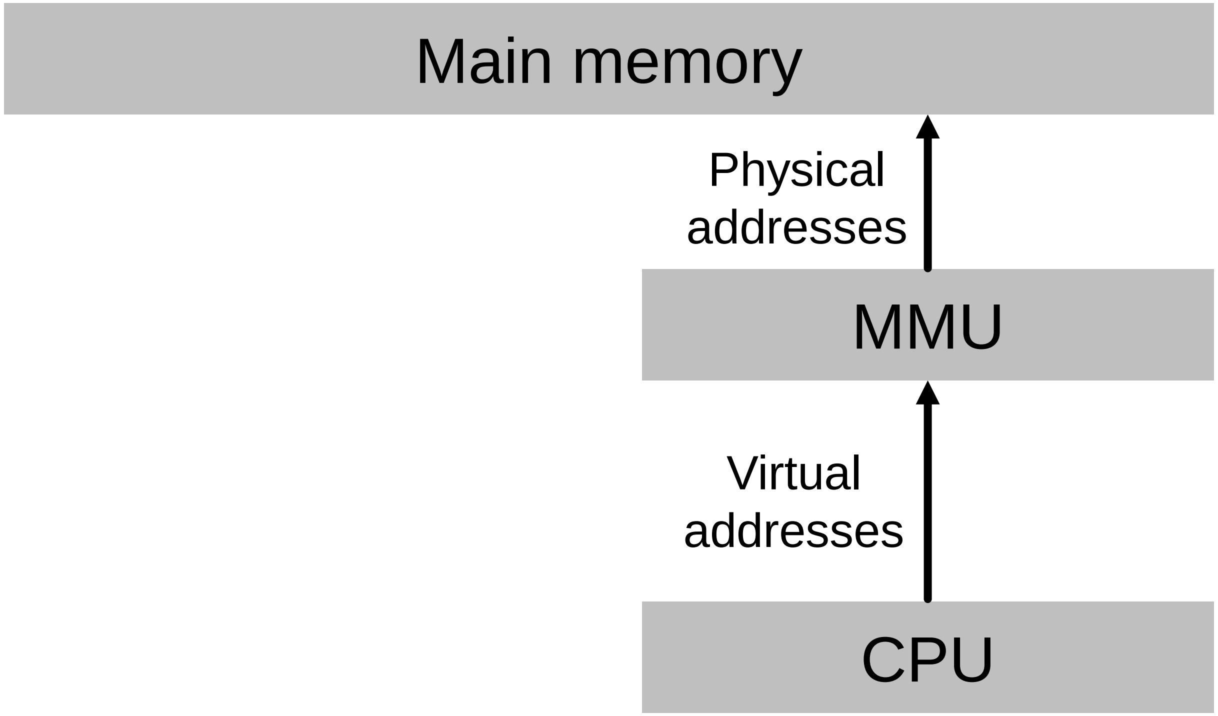

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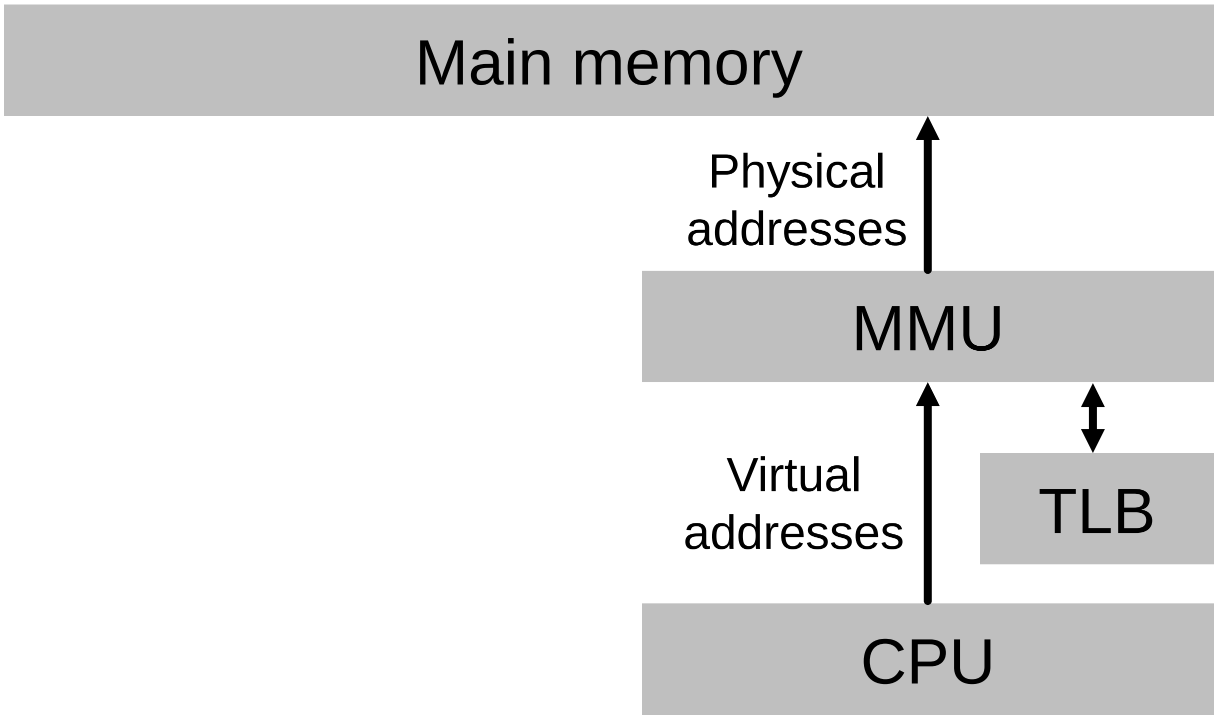

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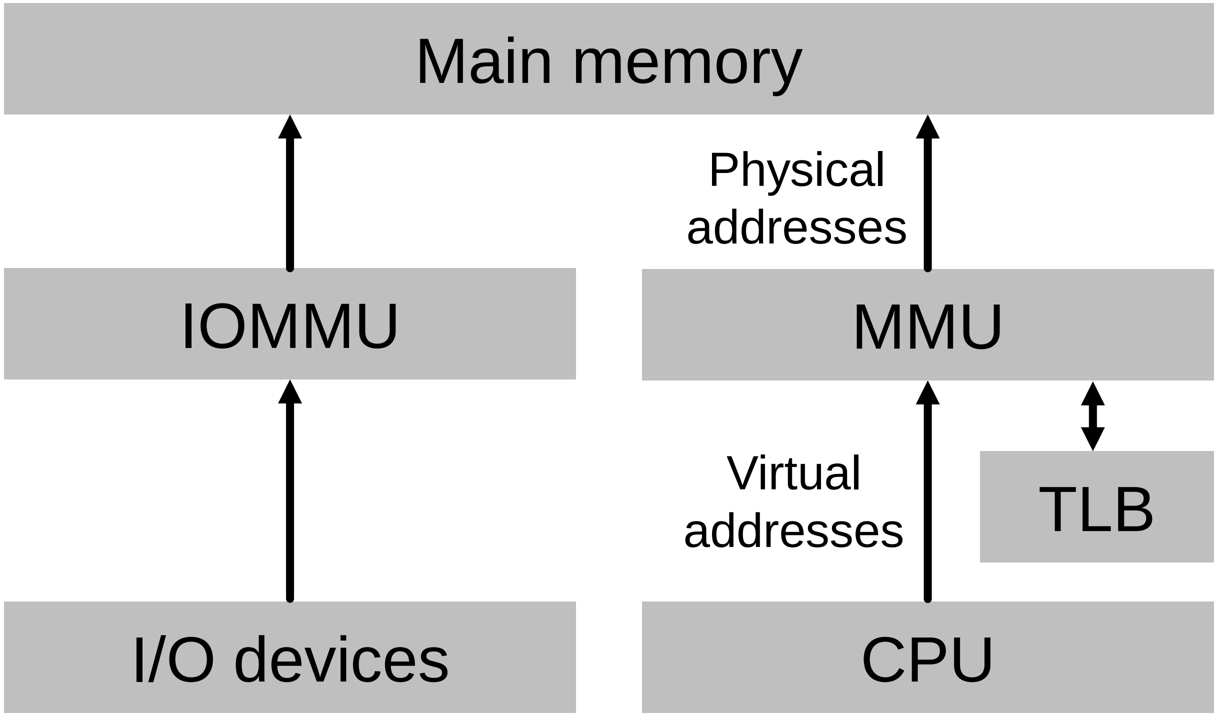

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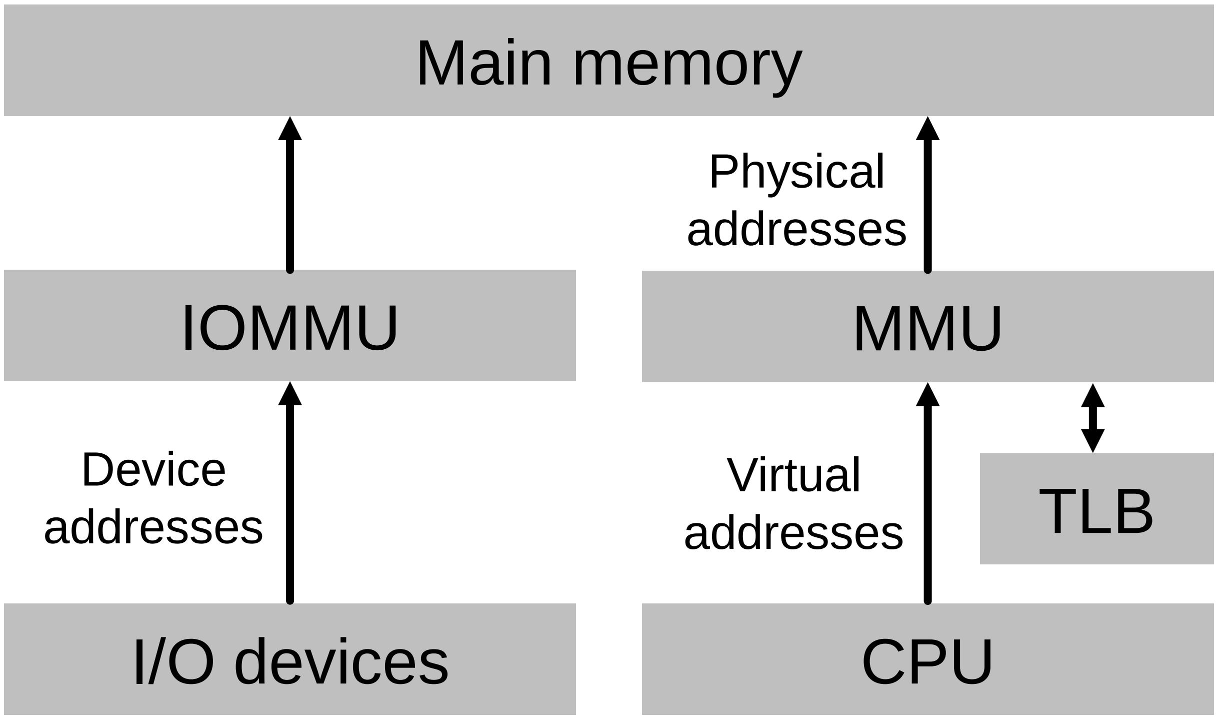

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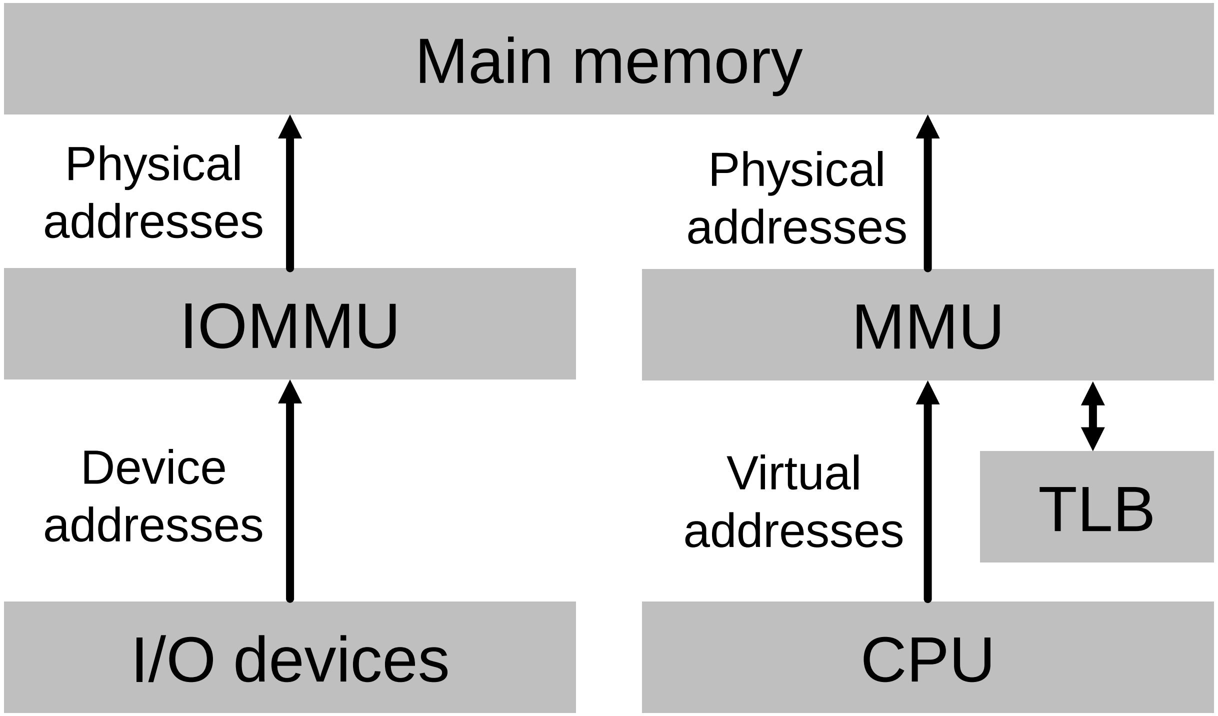

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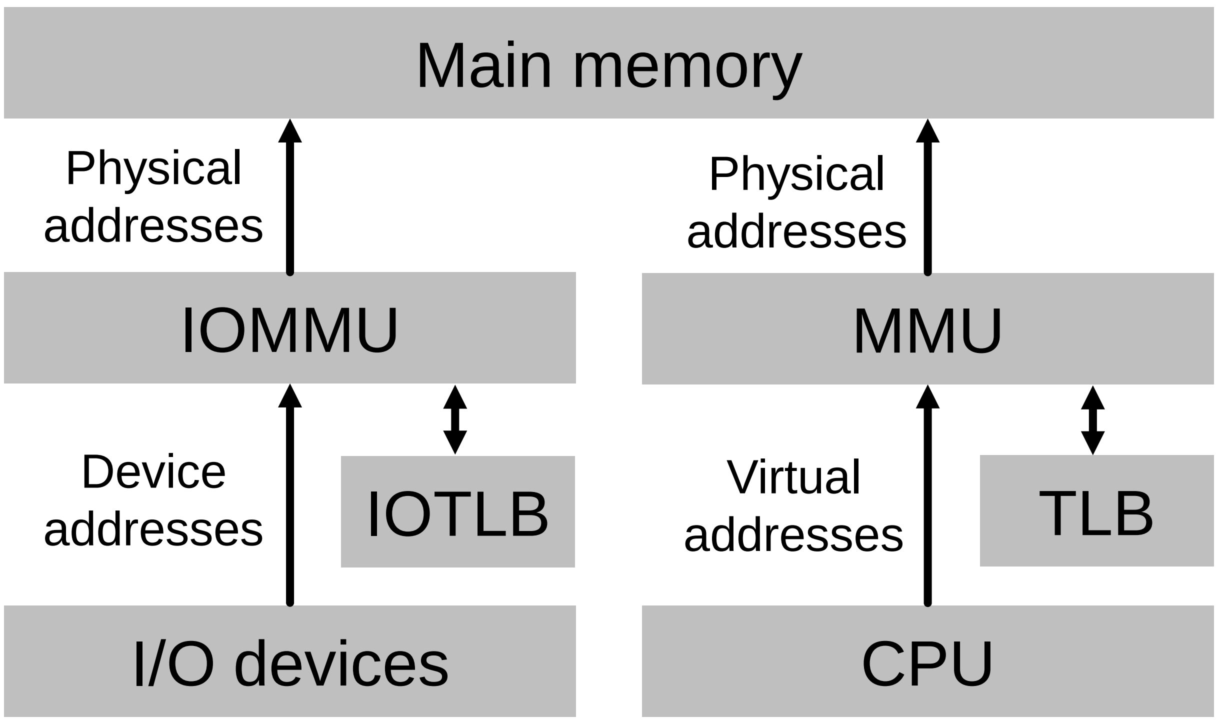

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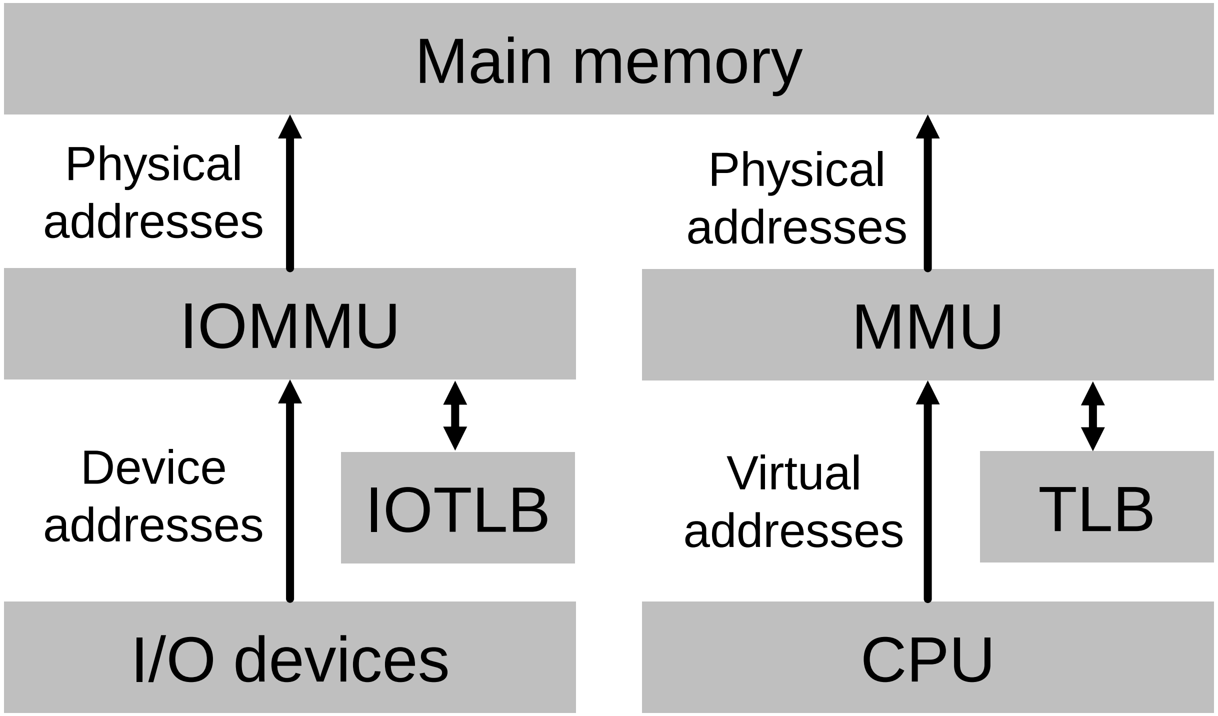

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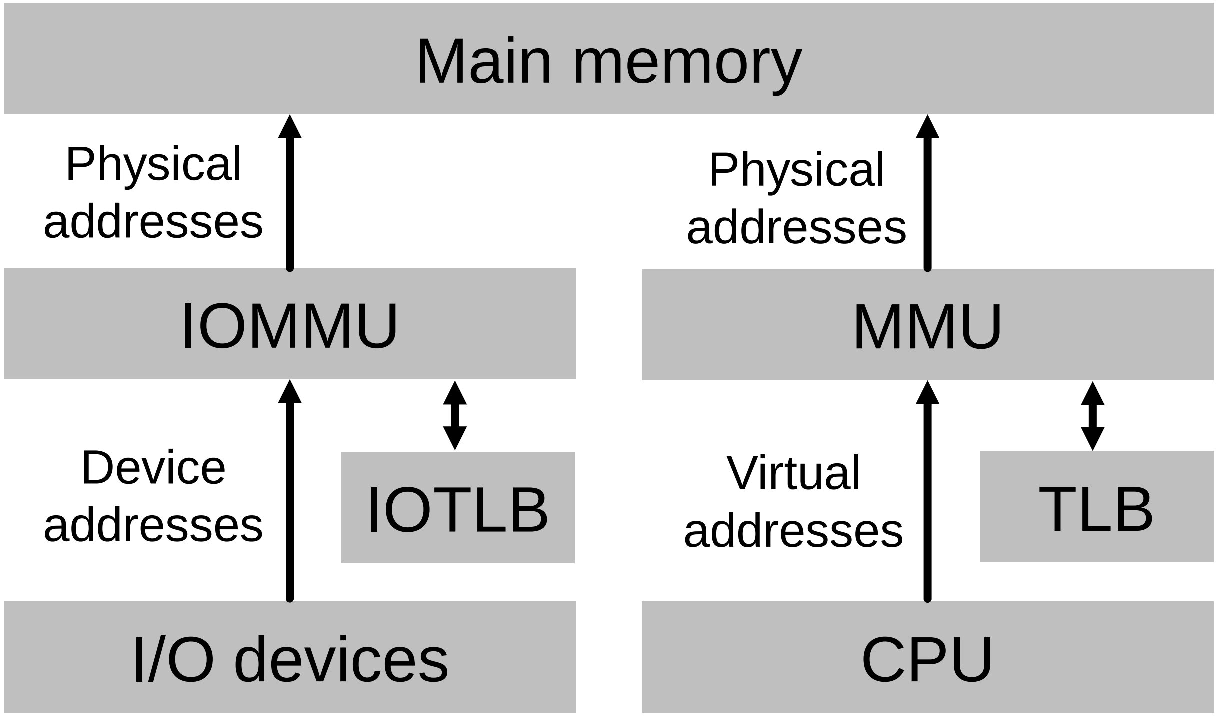

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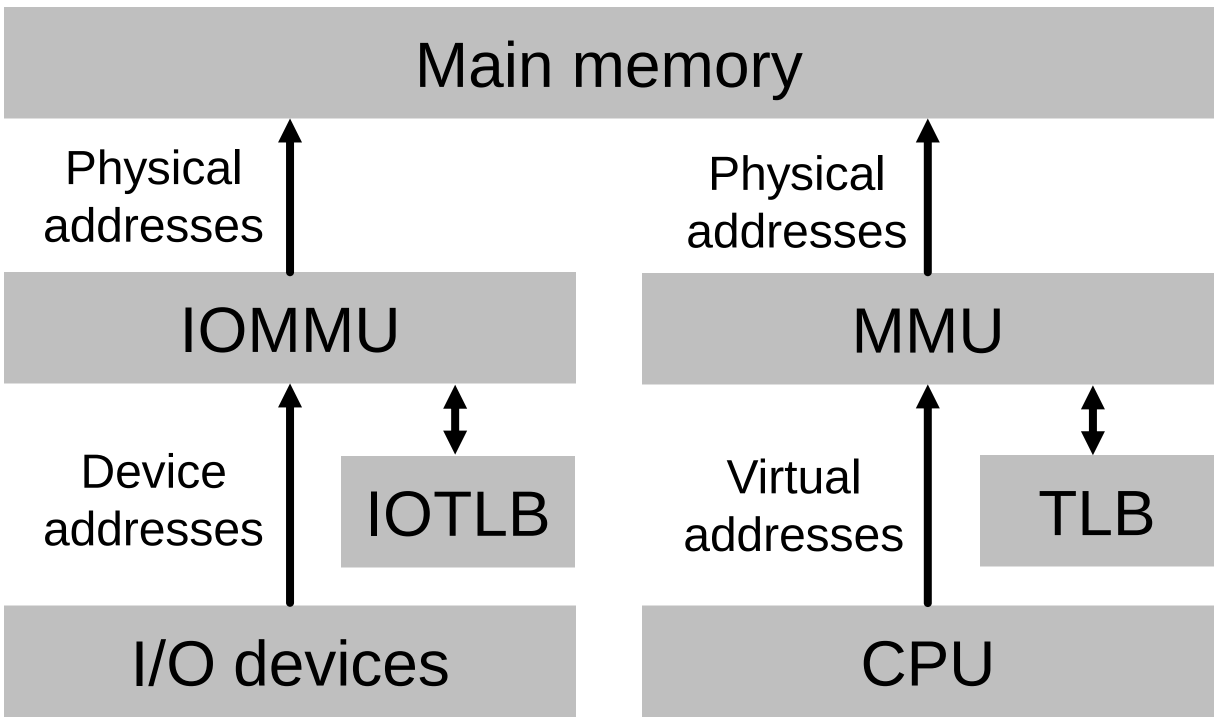


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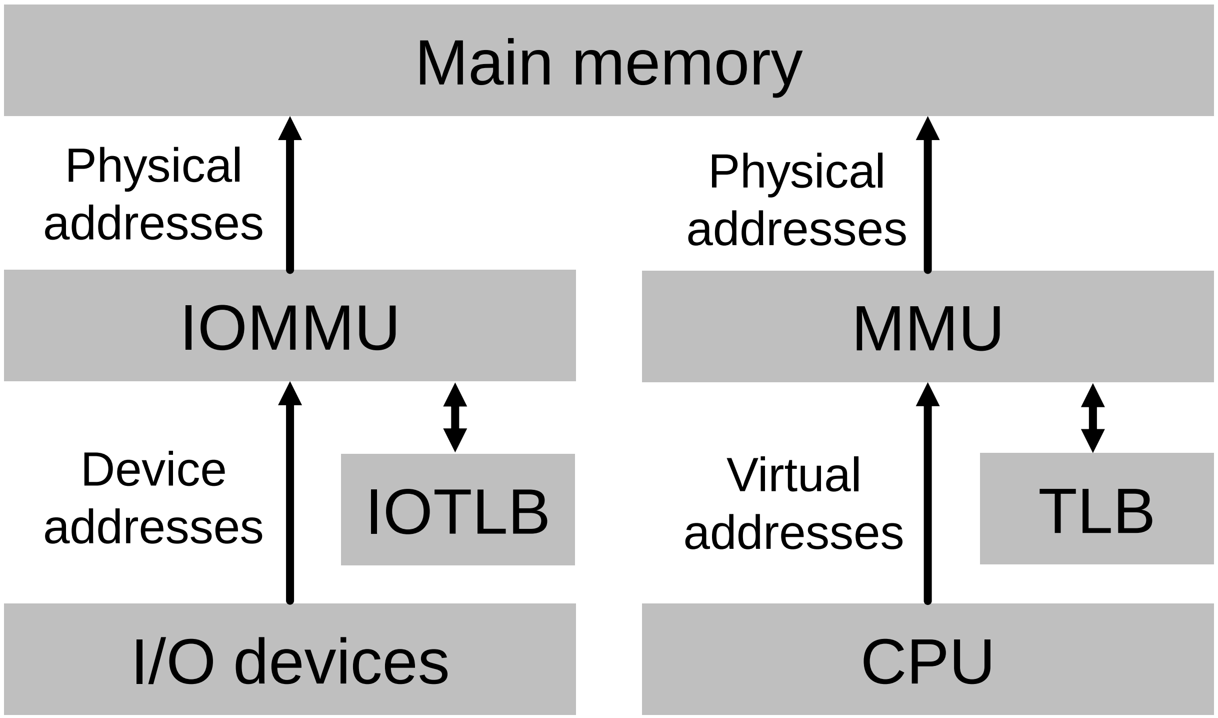


AMD
IBM
ARM
Sun microsystems
SOLARFLARE
intel + PCI EXPRESS

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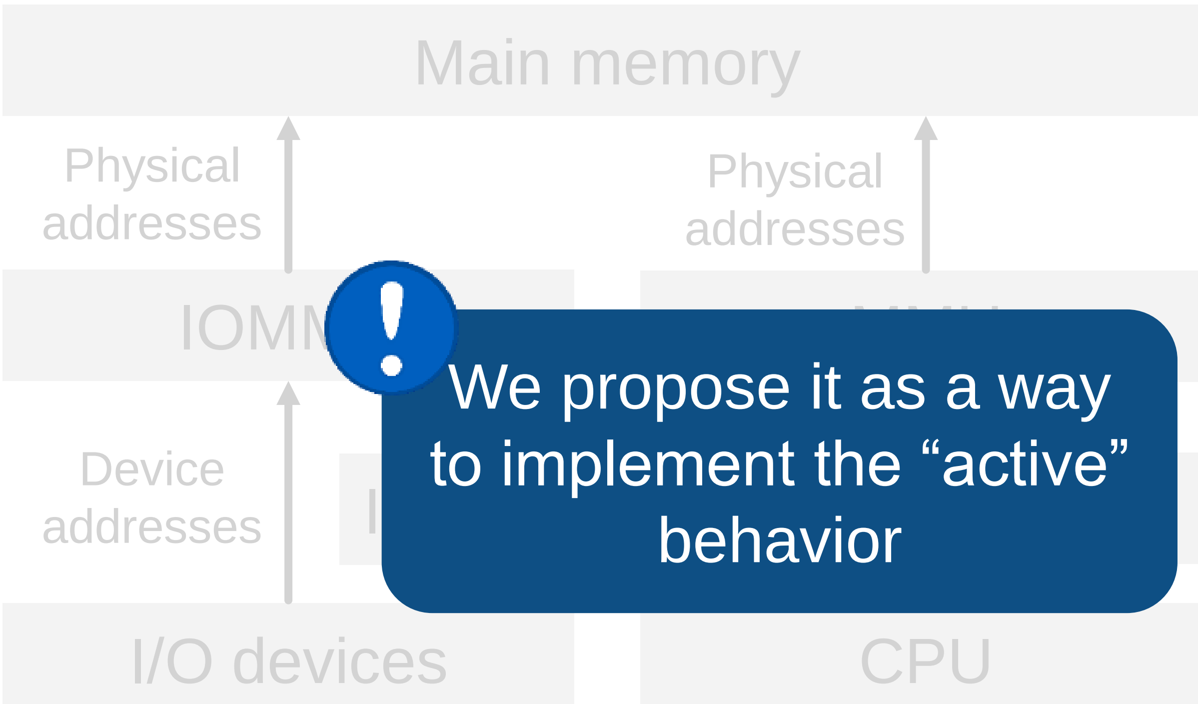


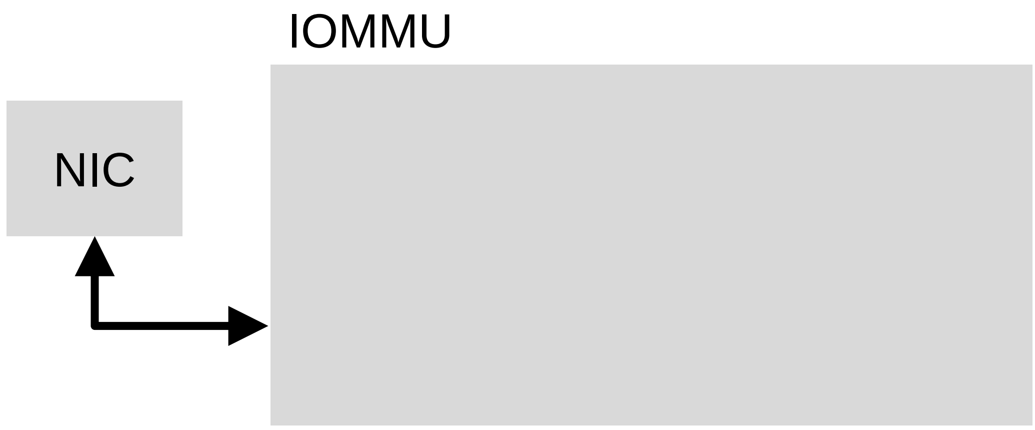

We propose it as a way to implement the “active” behavior

# IOMMUS AND RMA

# IOMMUs and RMA

NIC

# IOMMUs and RMA



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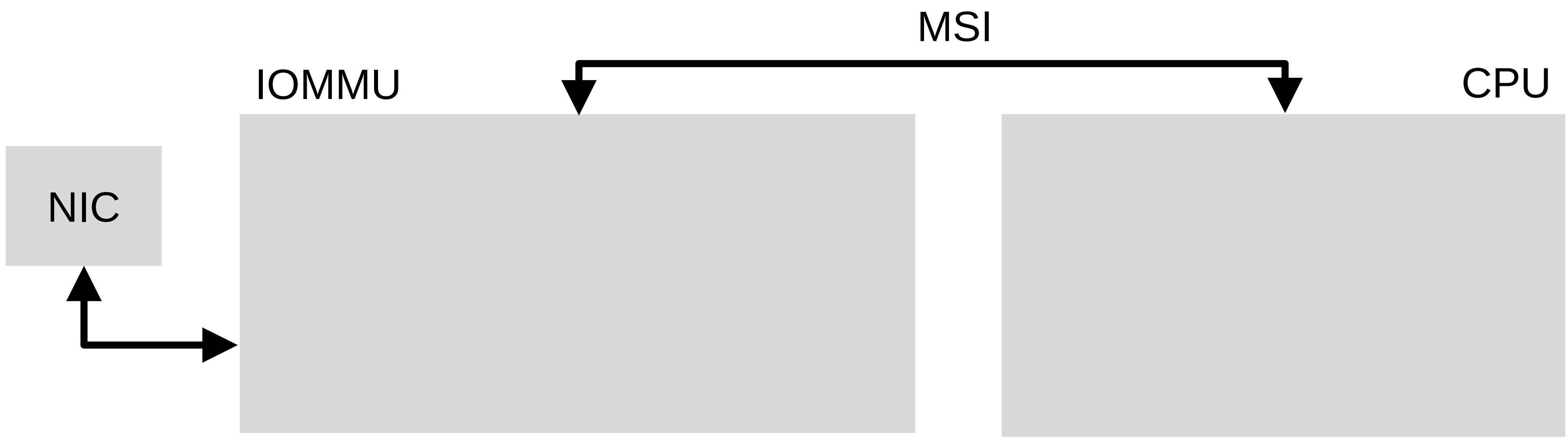

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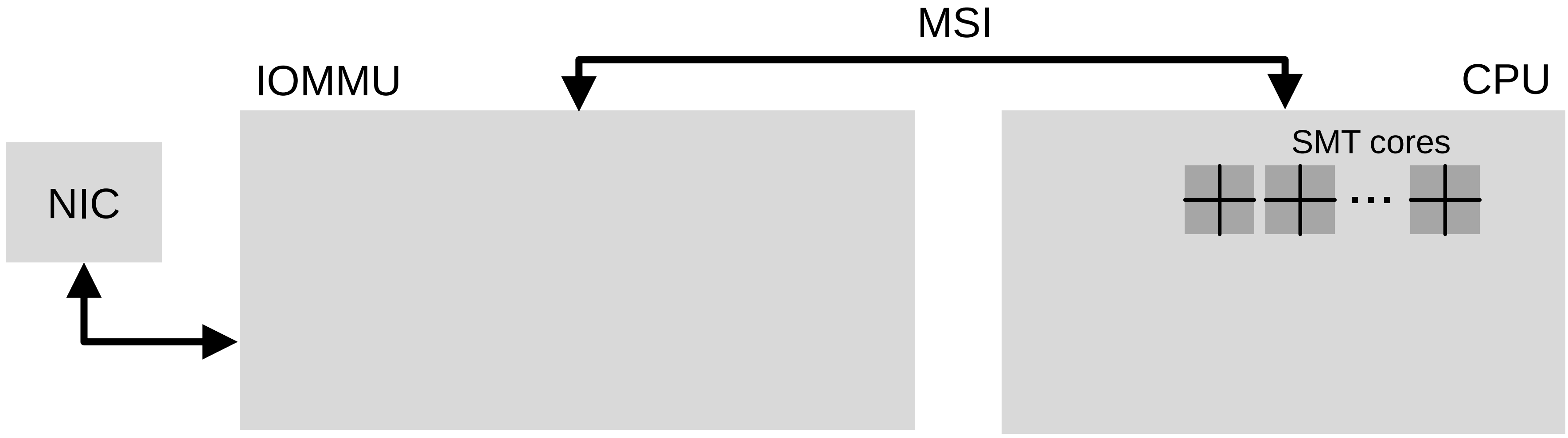

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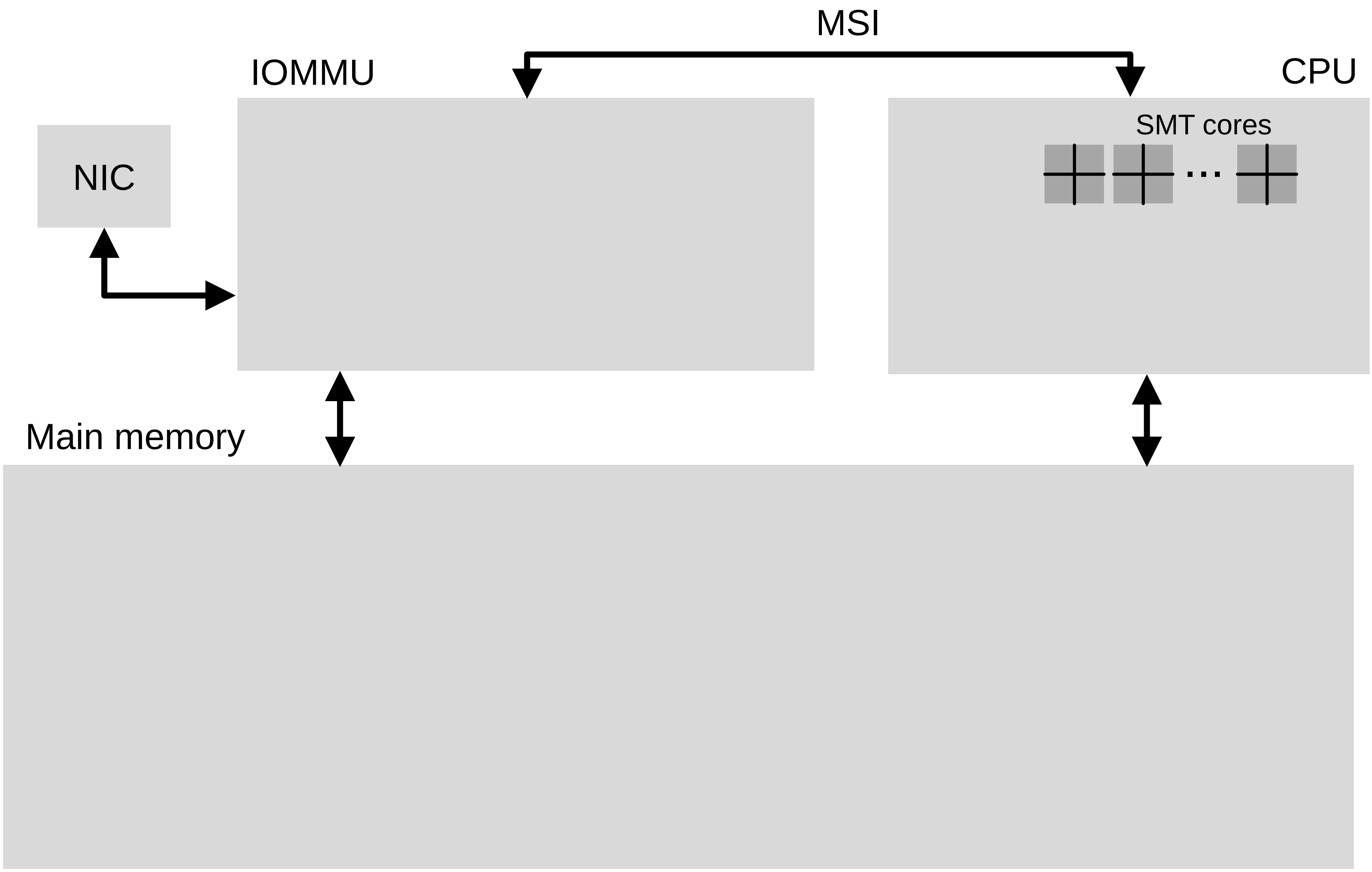

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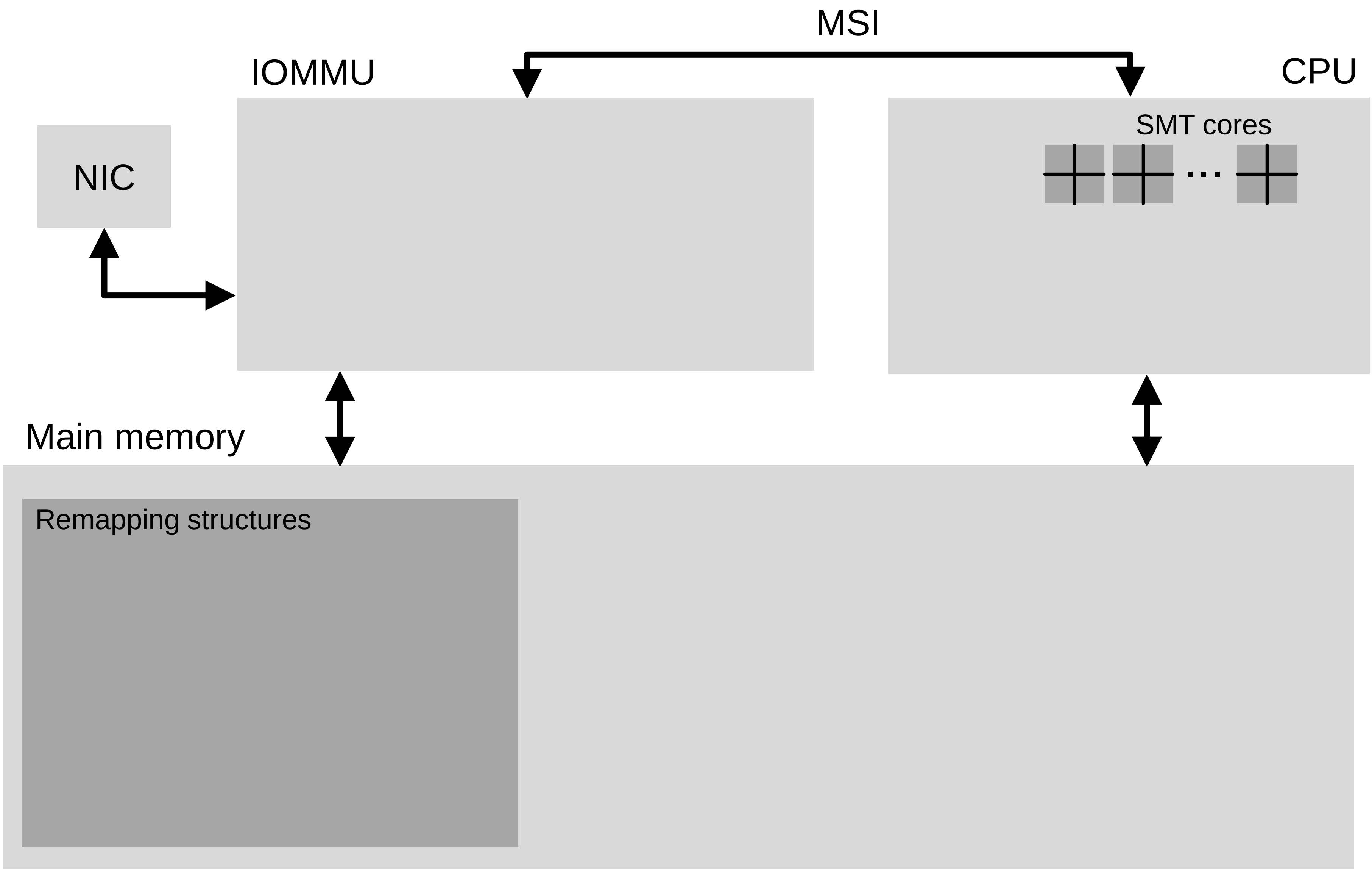

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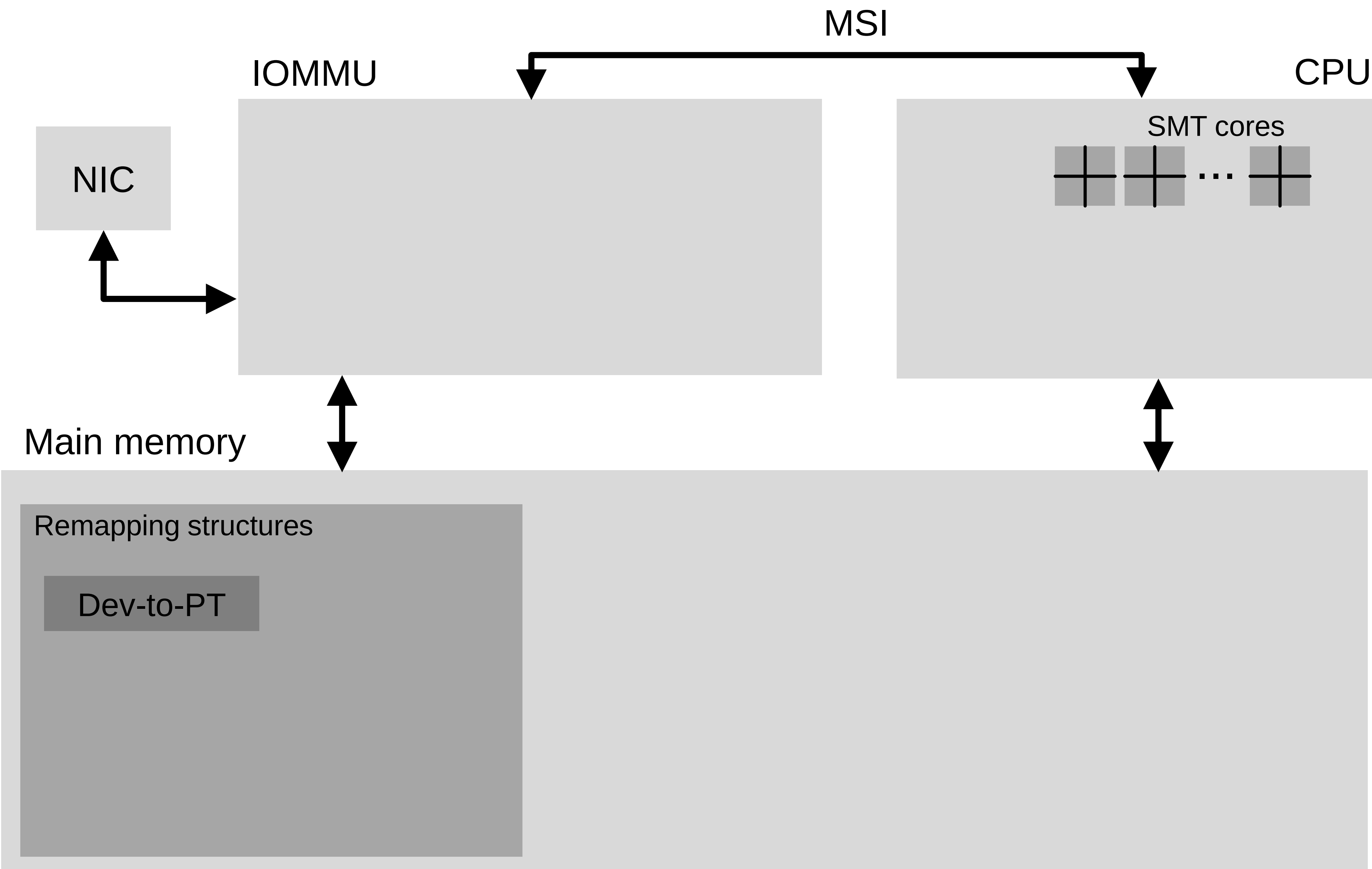

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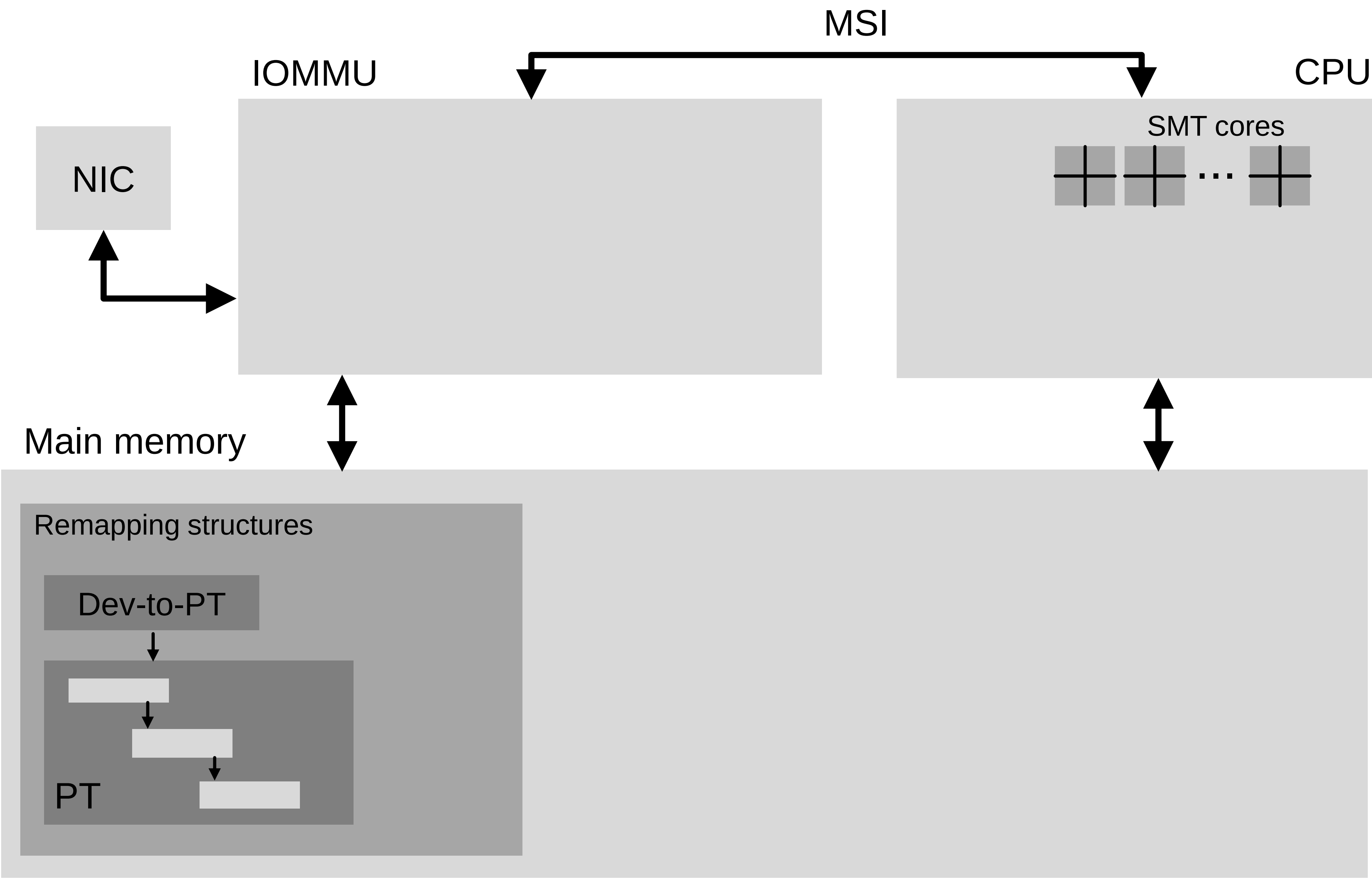

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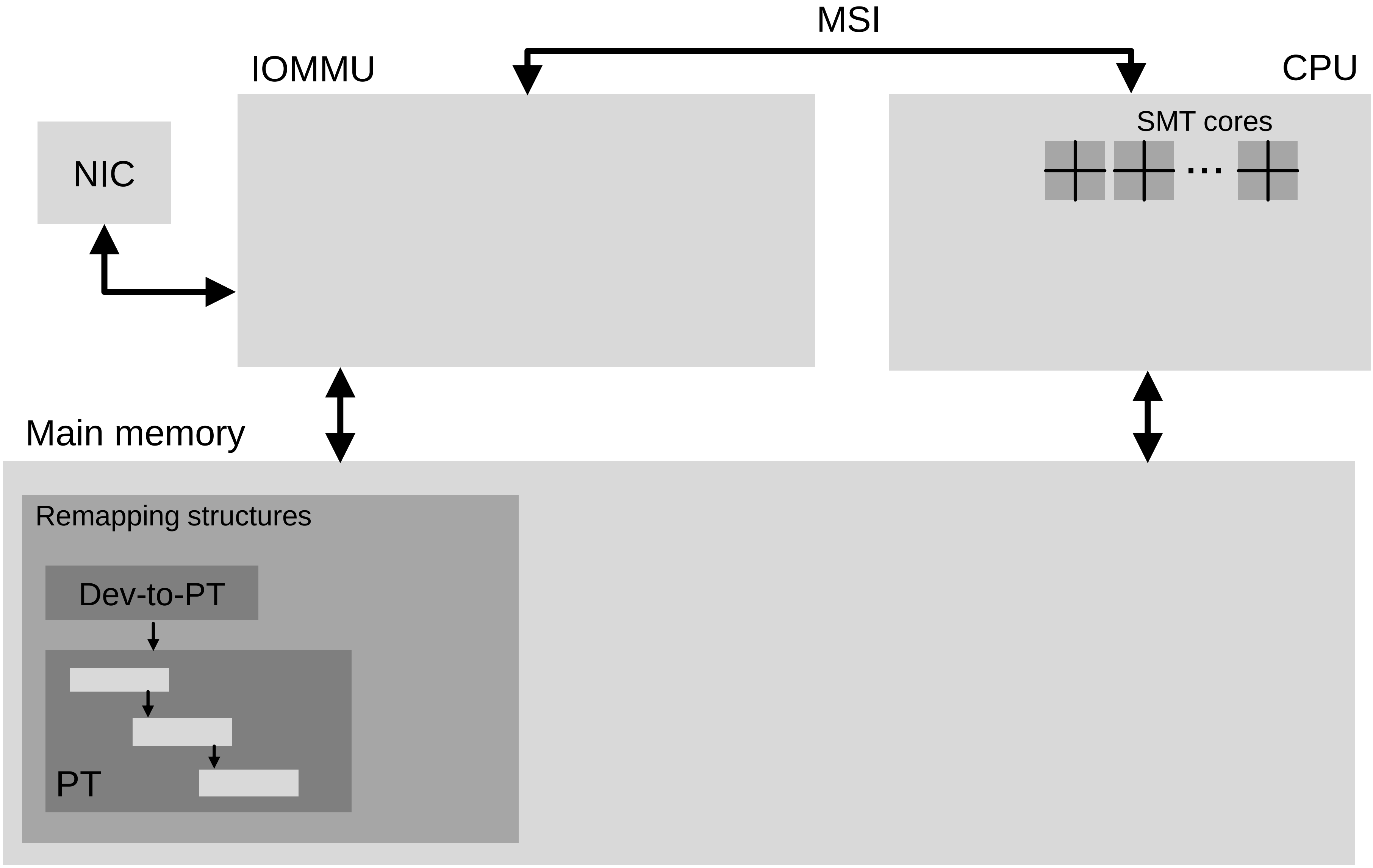

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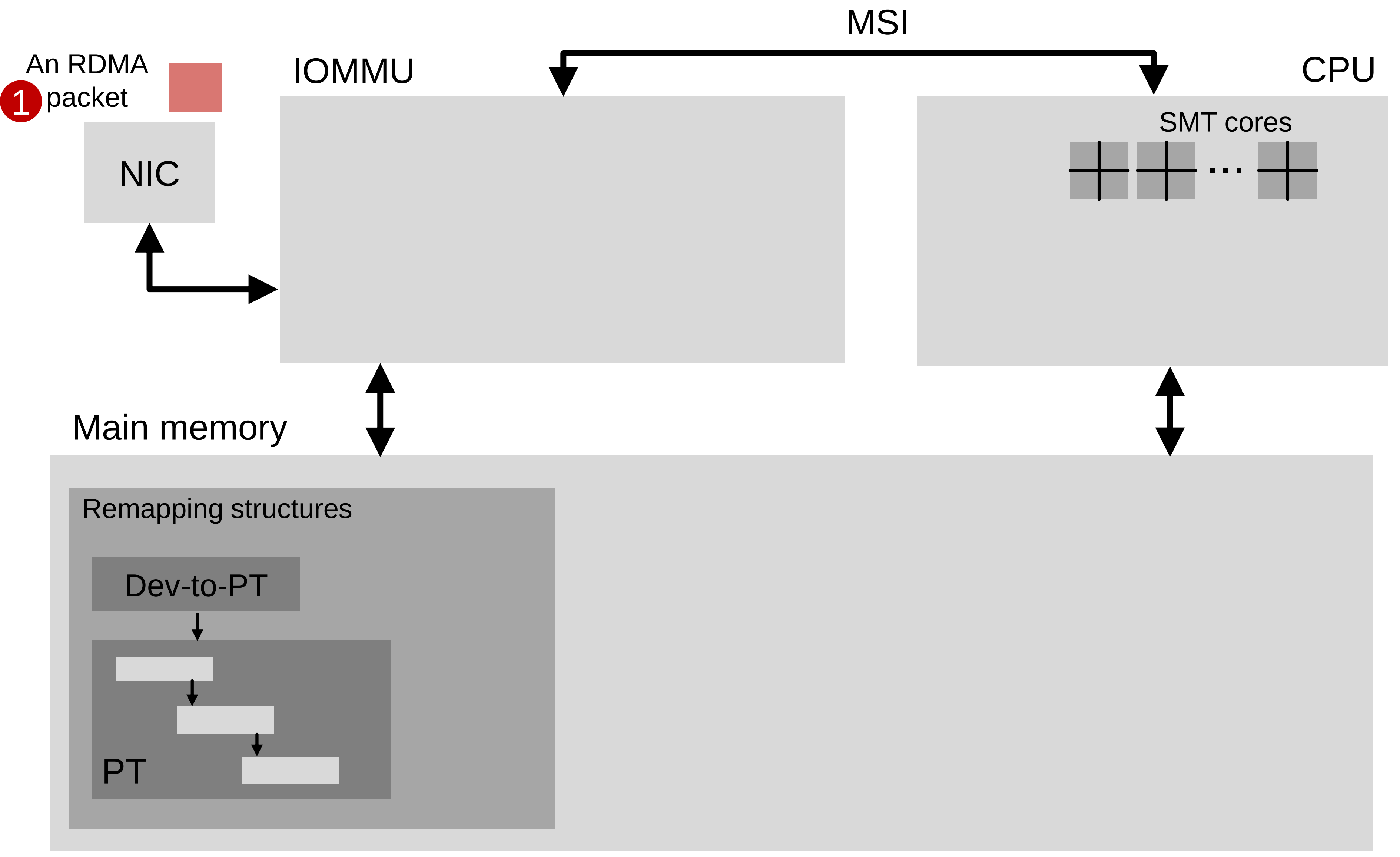

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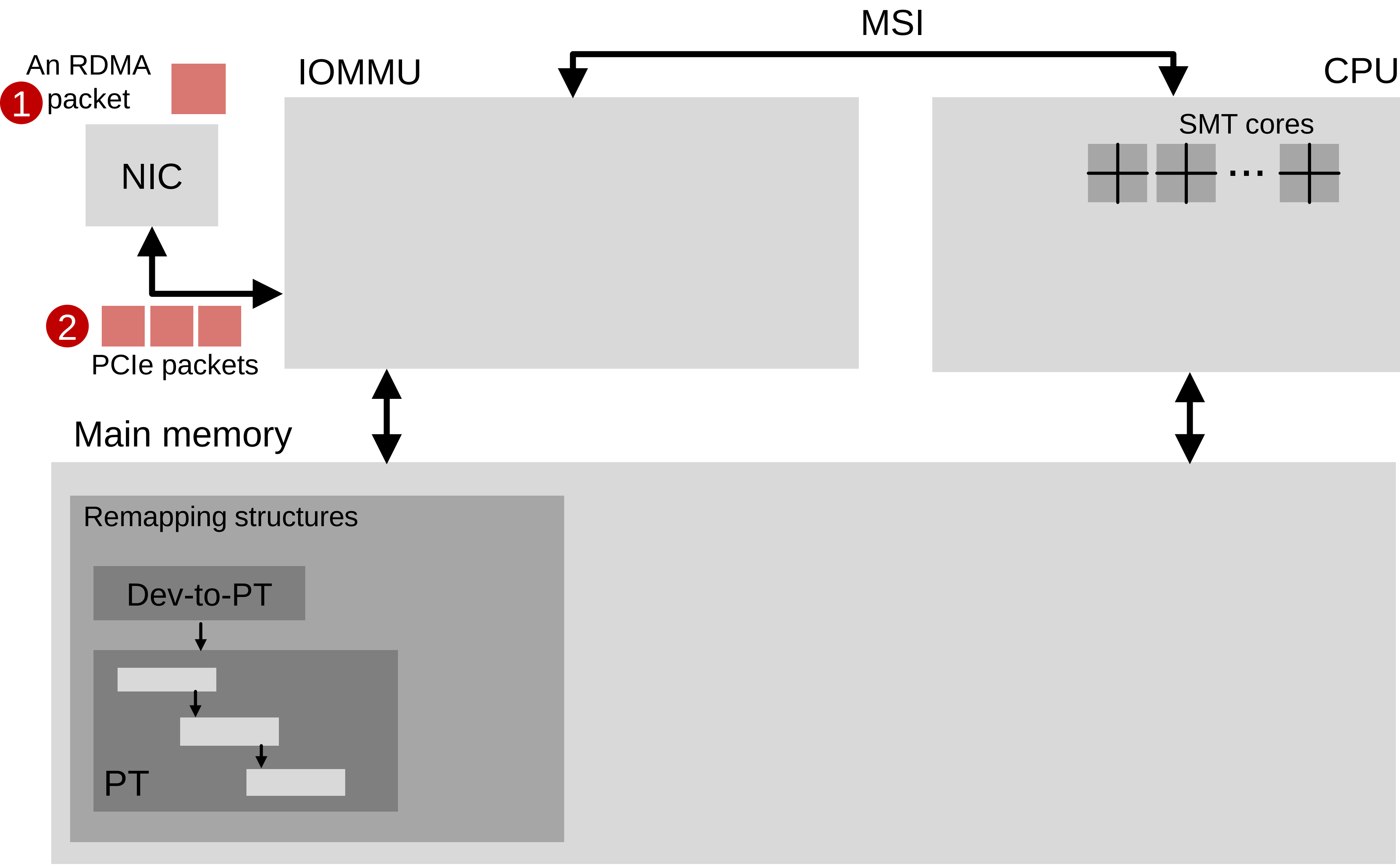
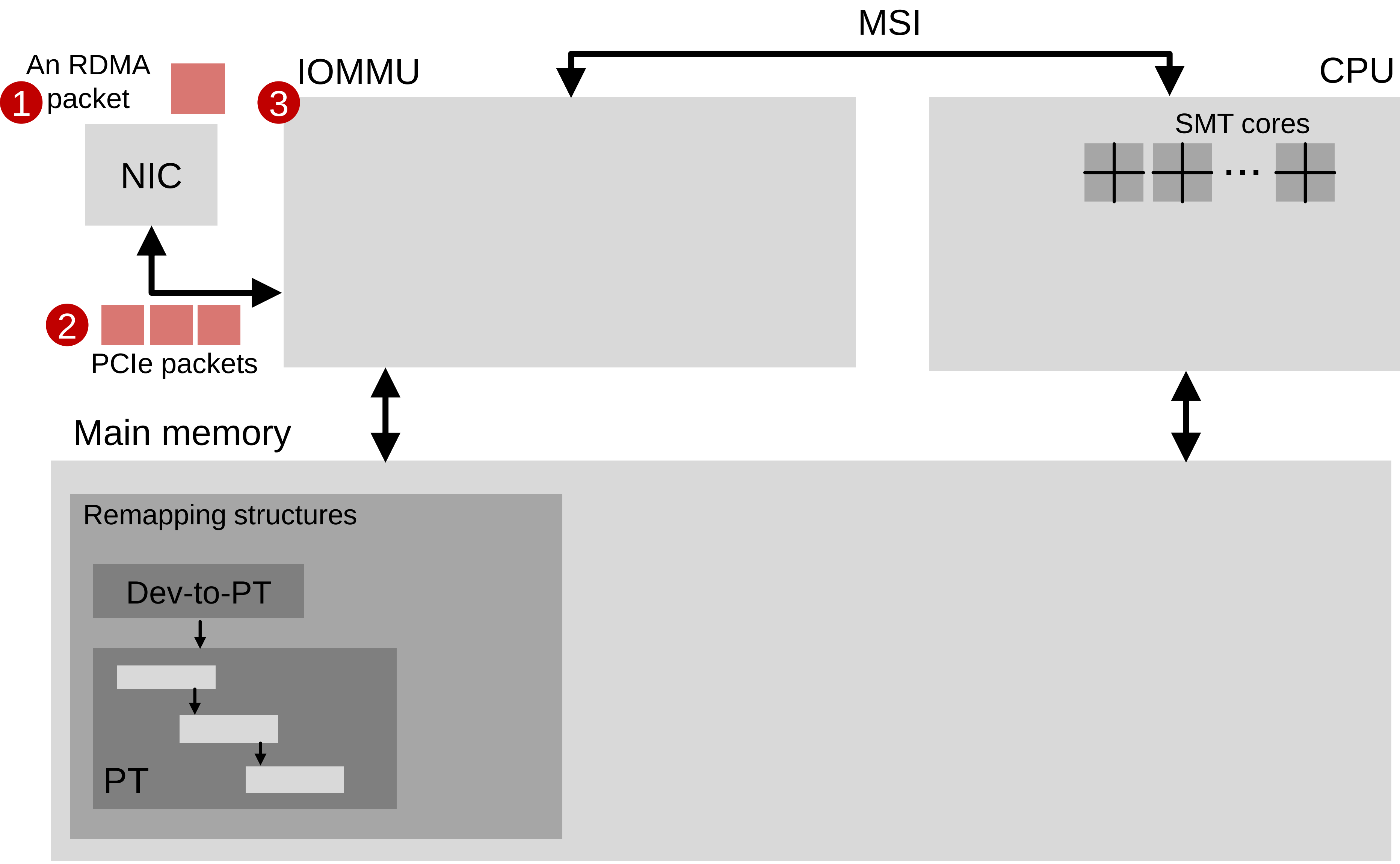


# IOMMUs and RMA



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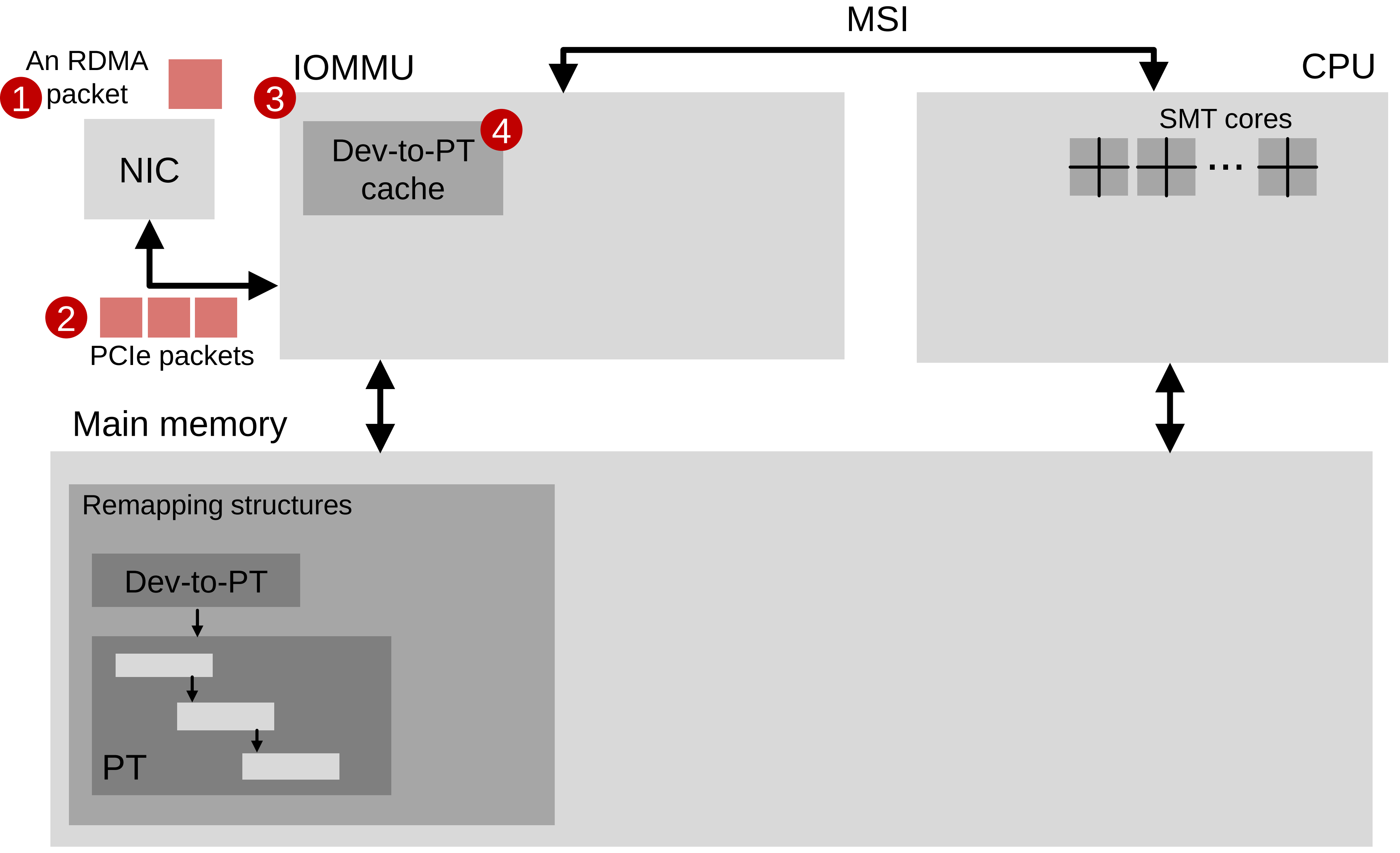

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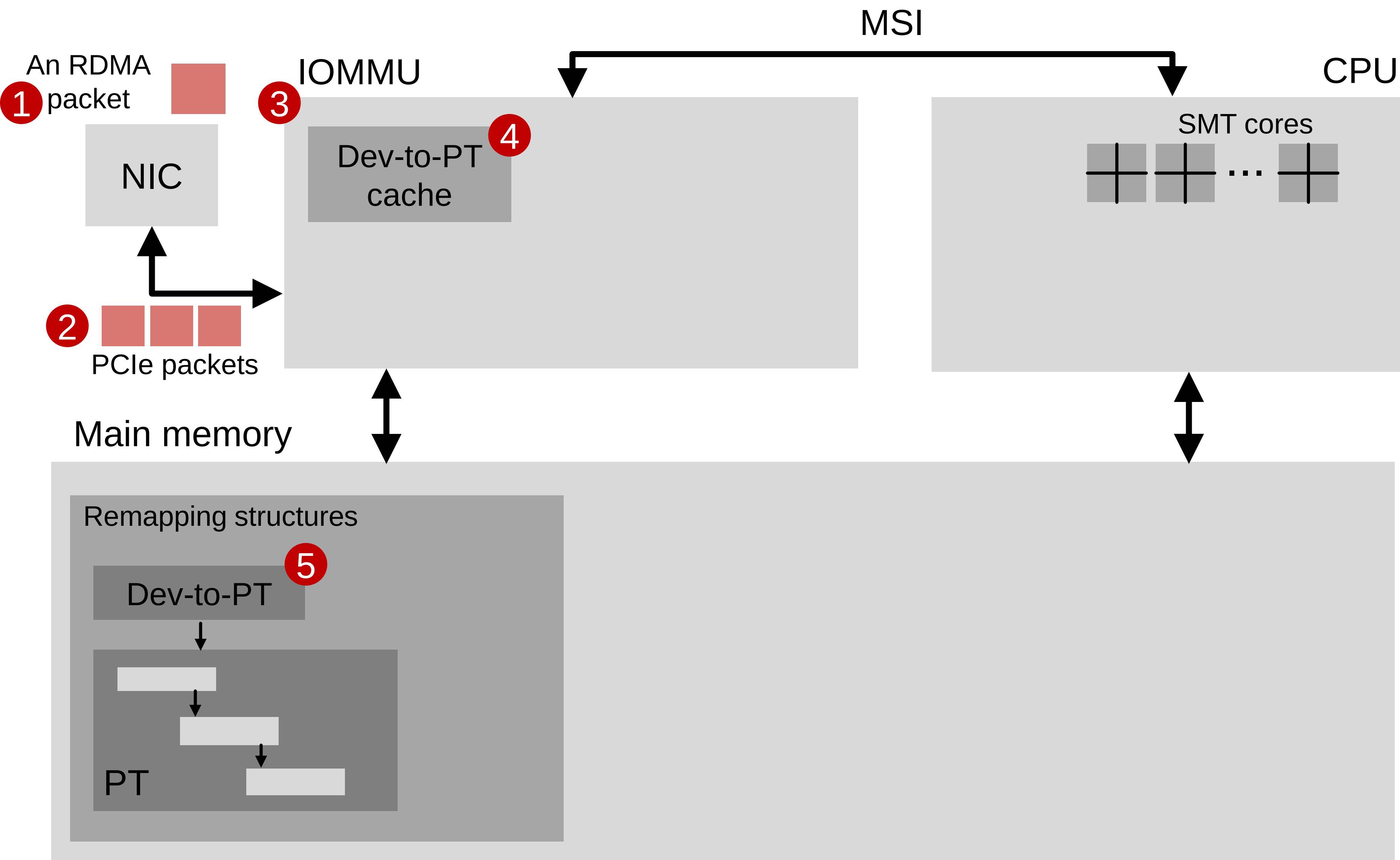

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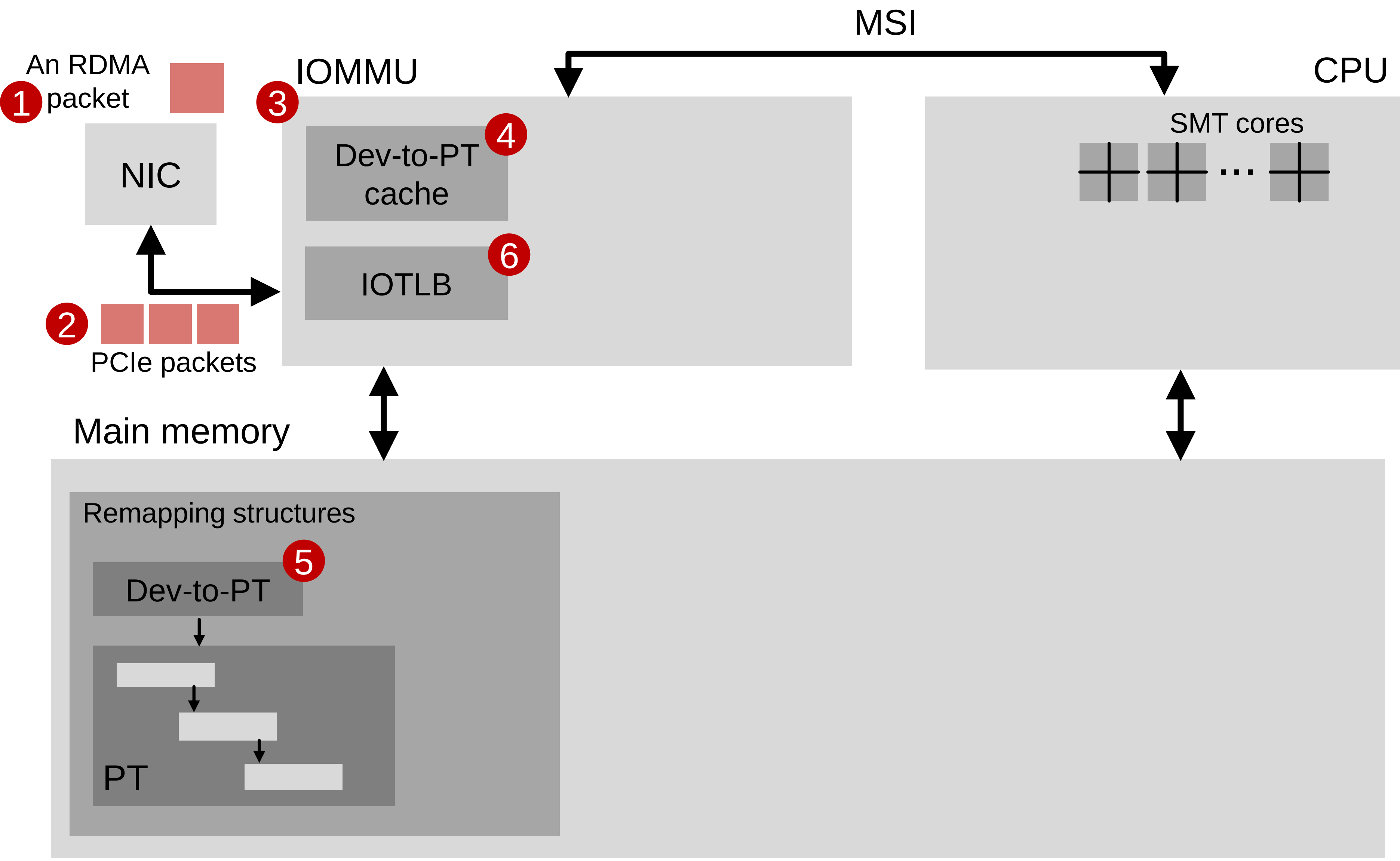

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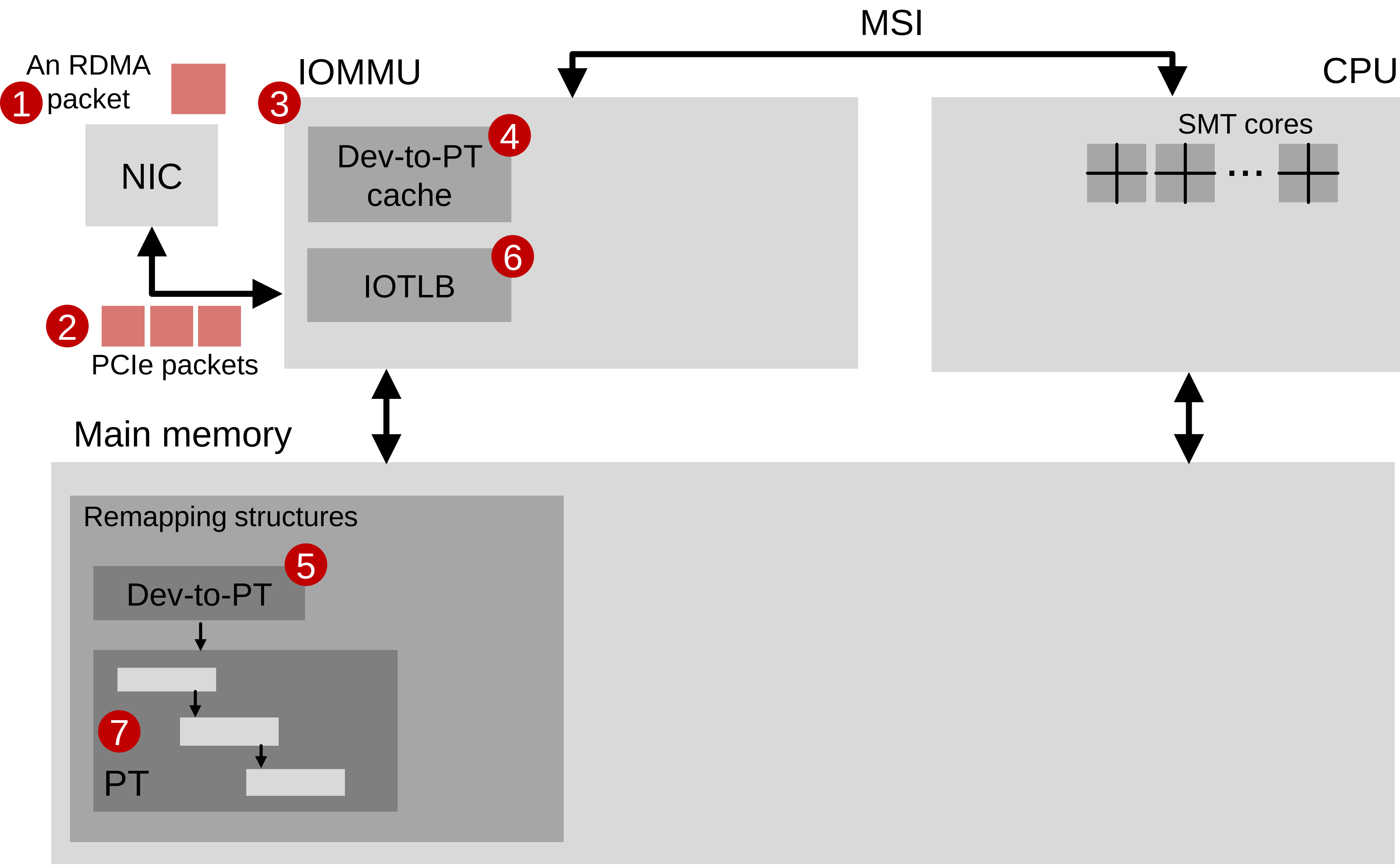

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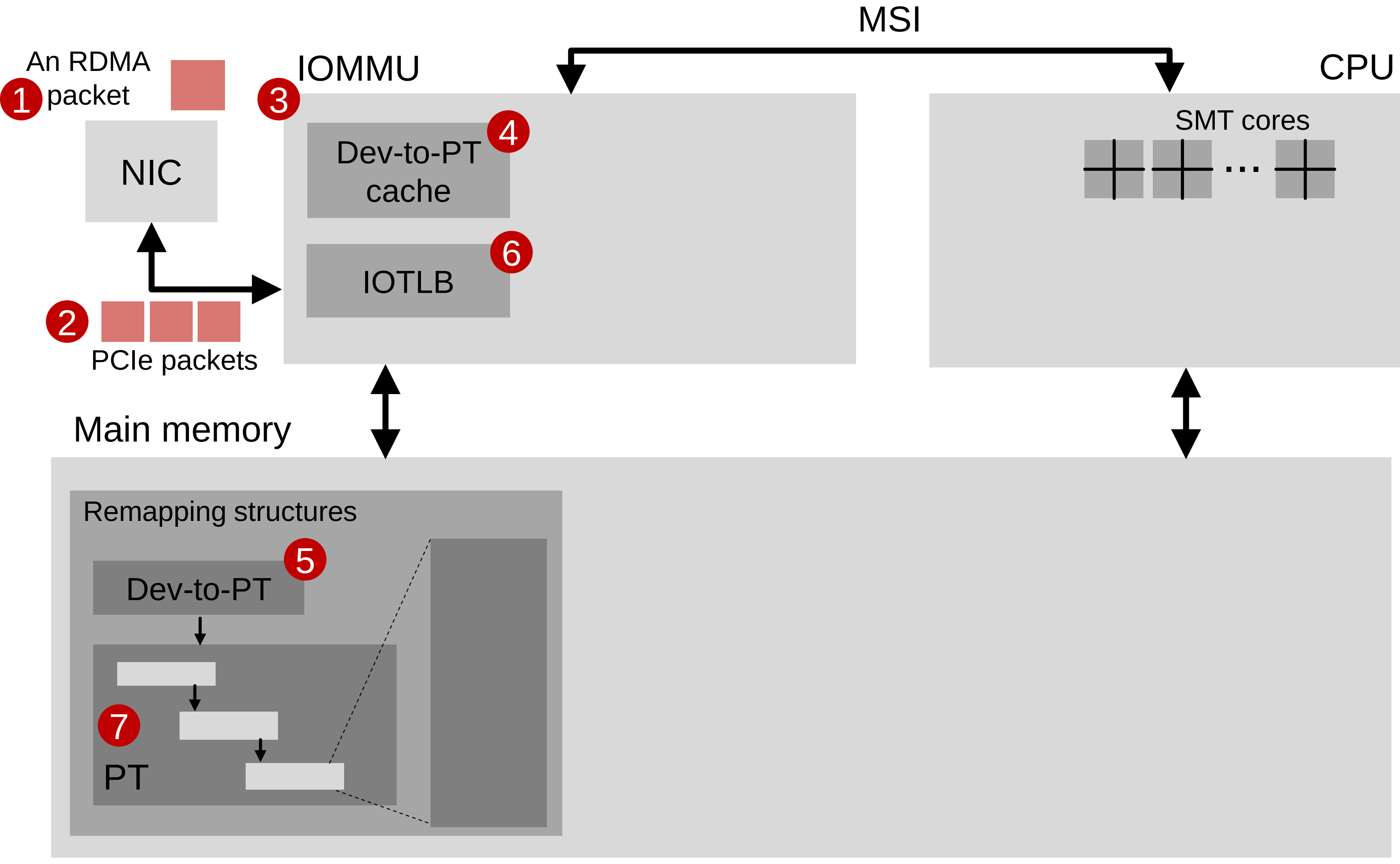

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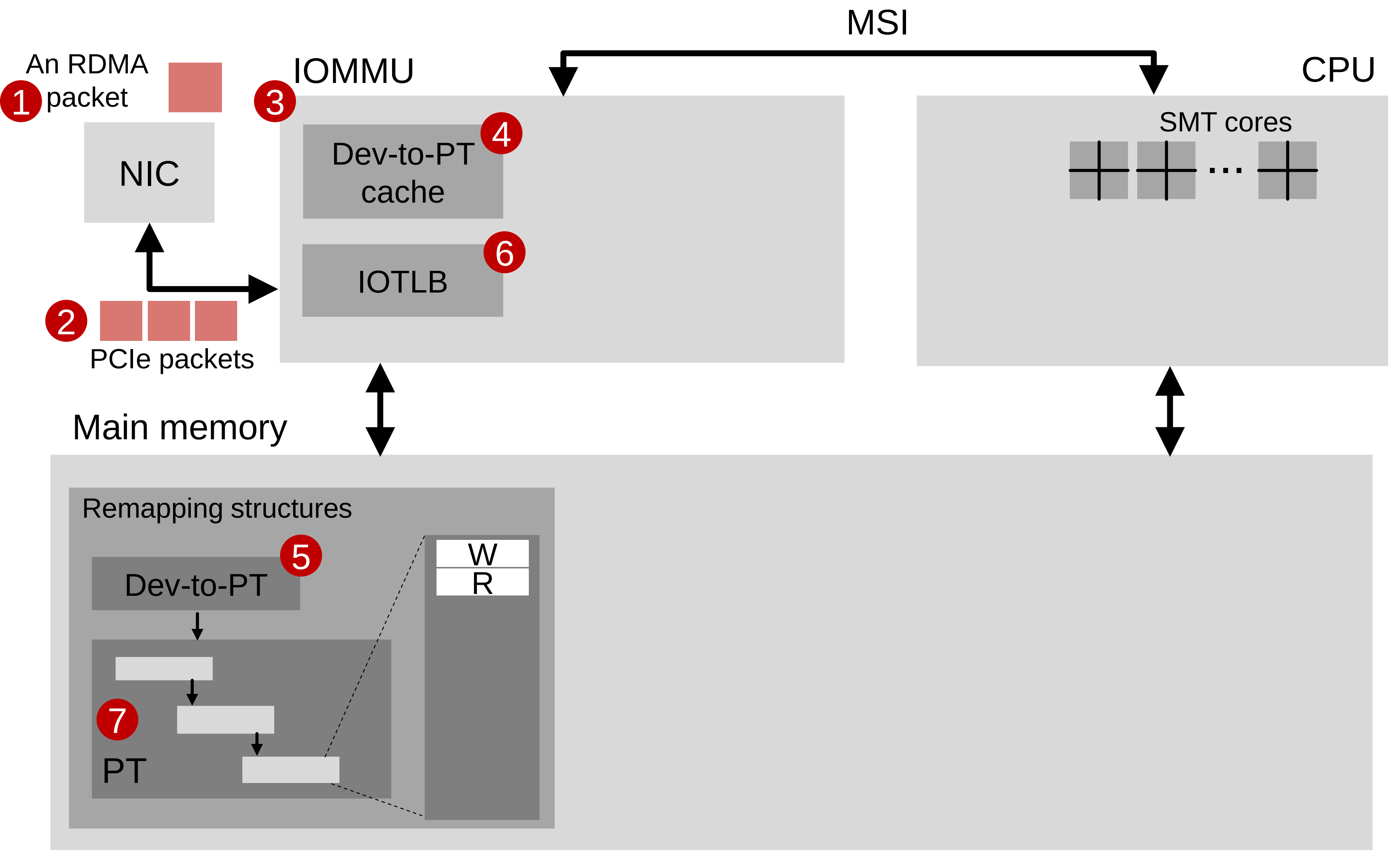

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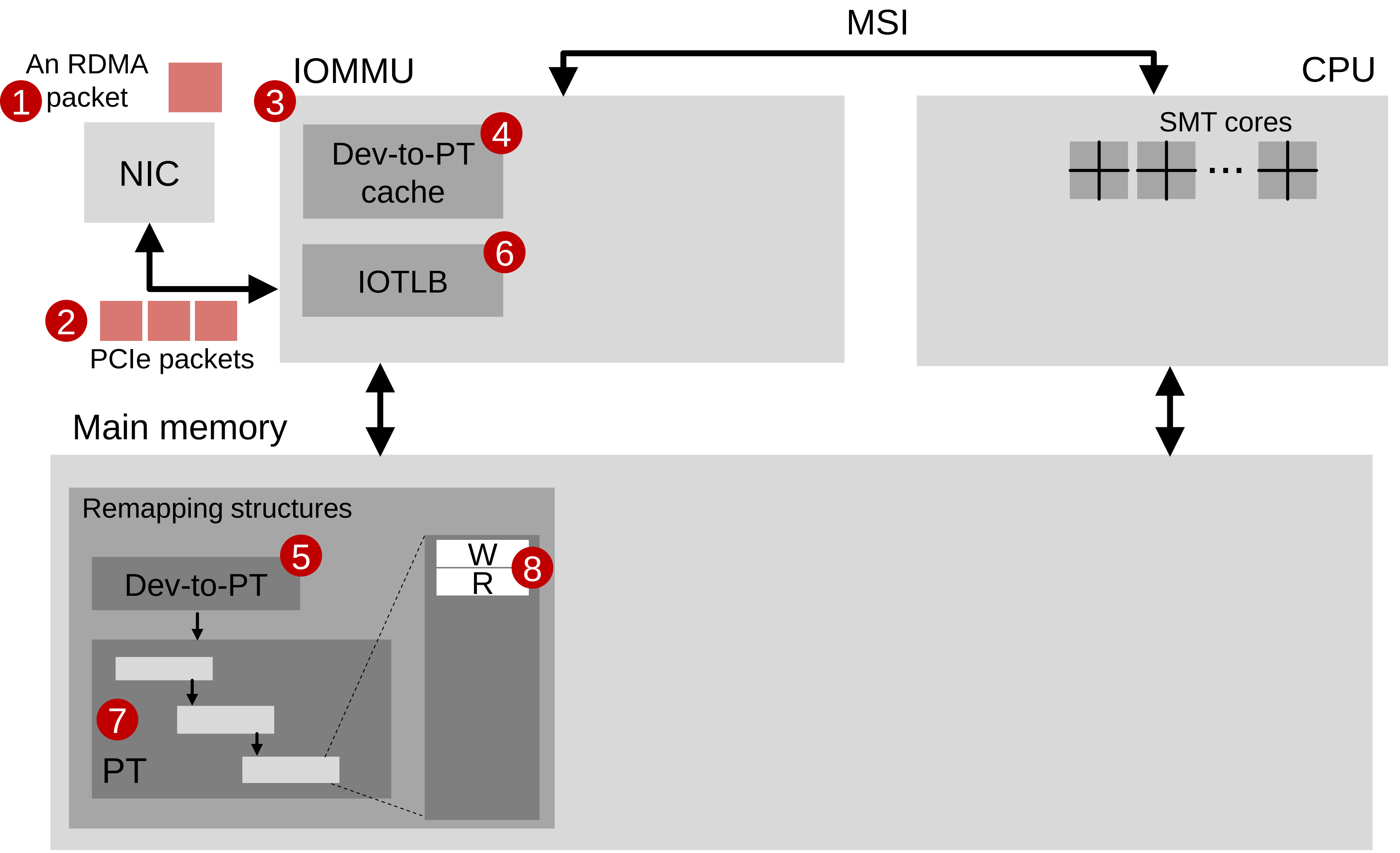

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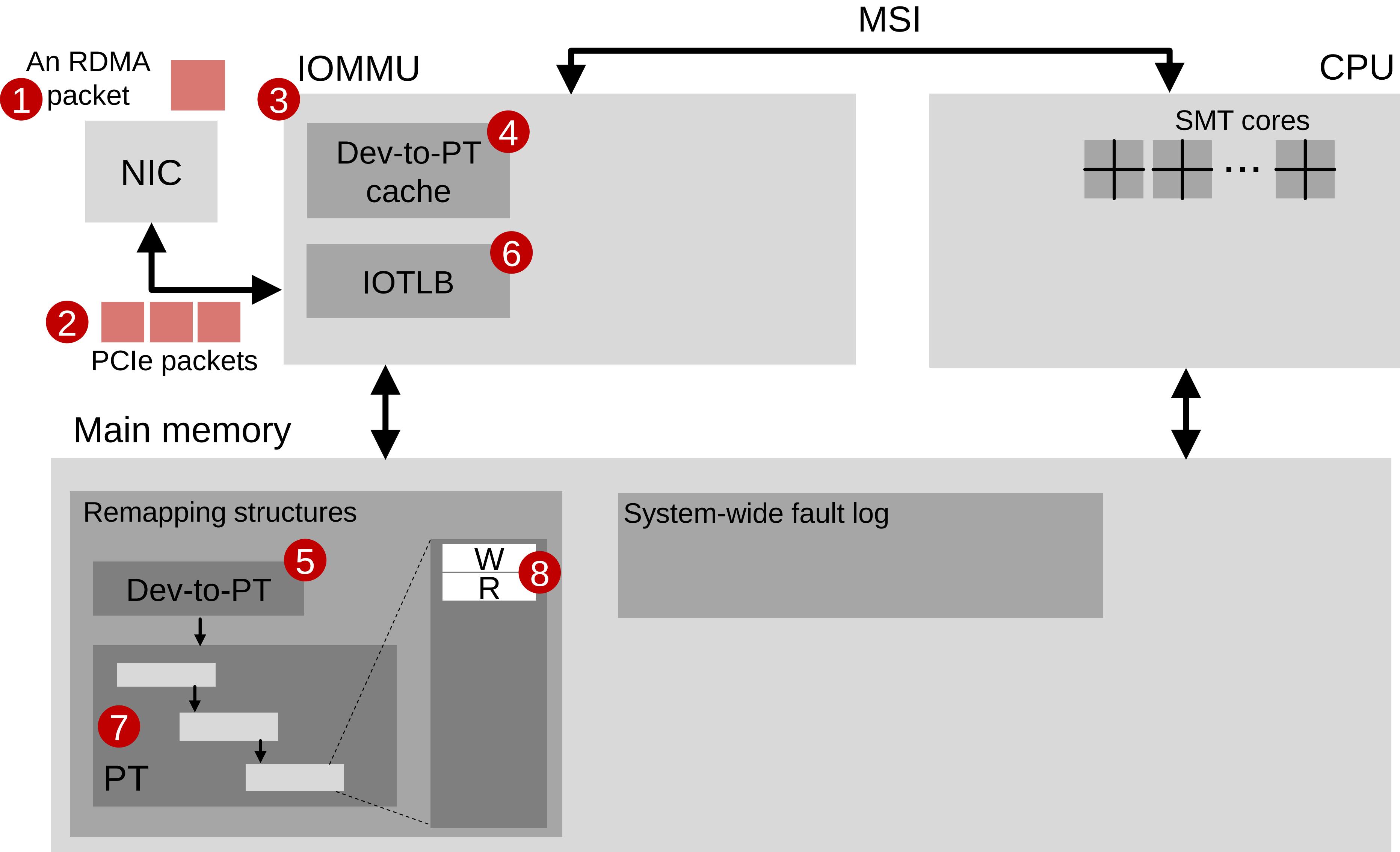

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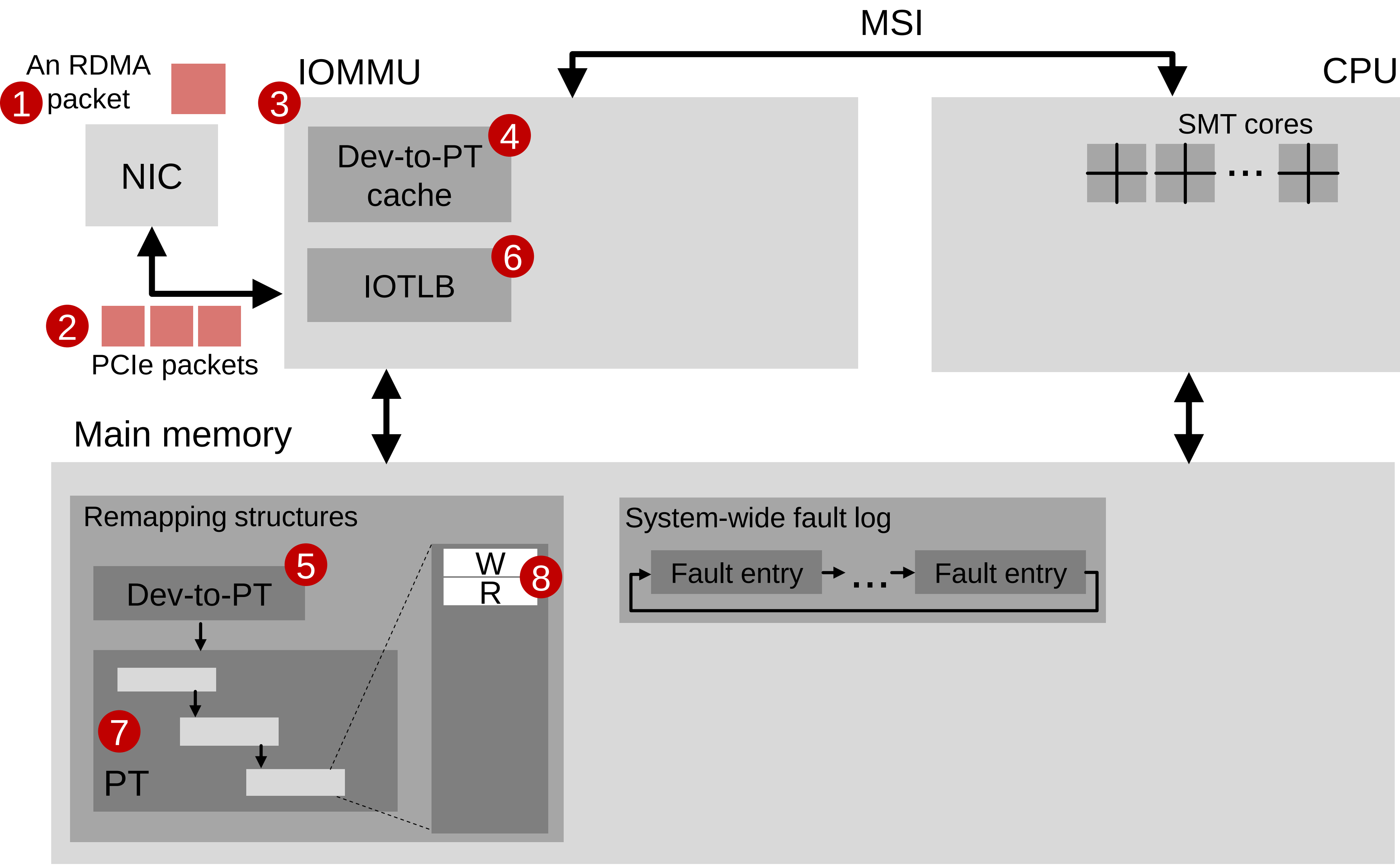

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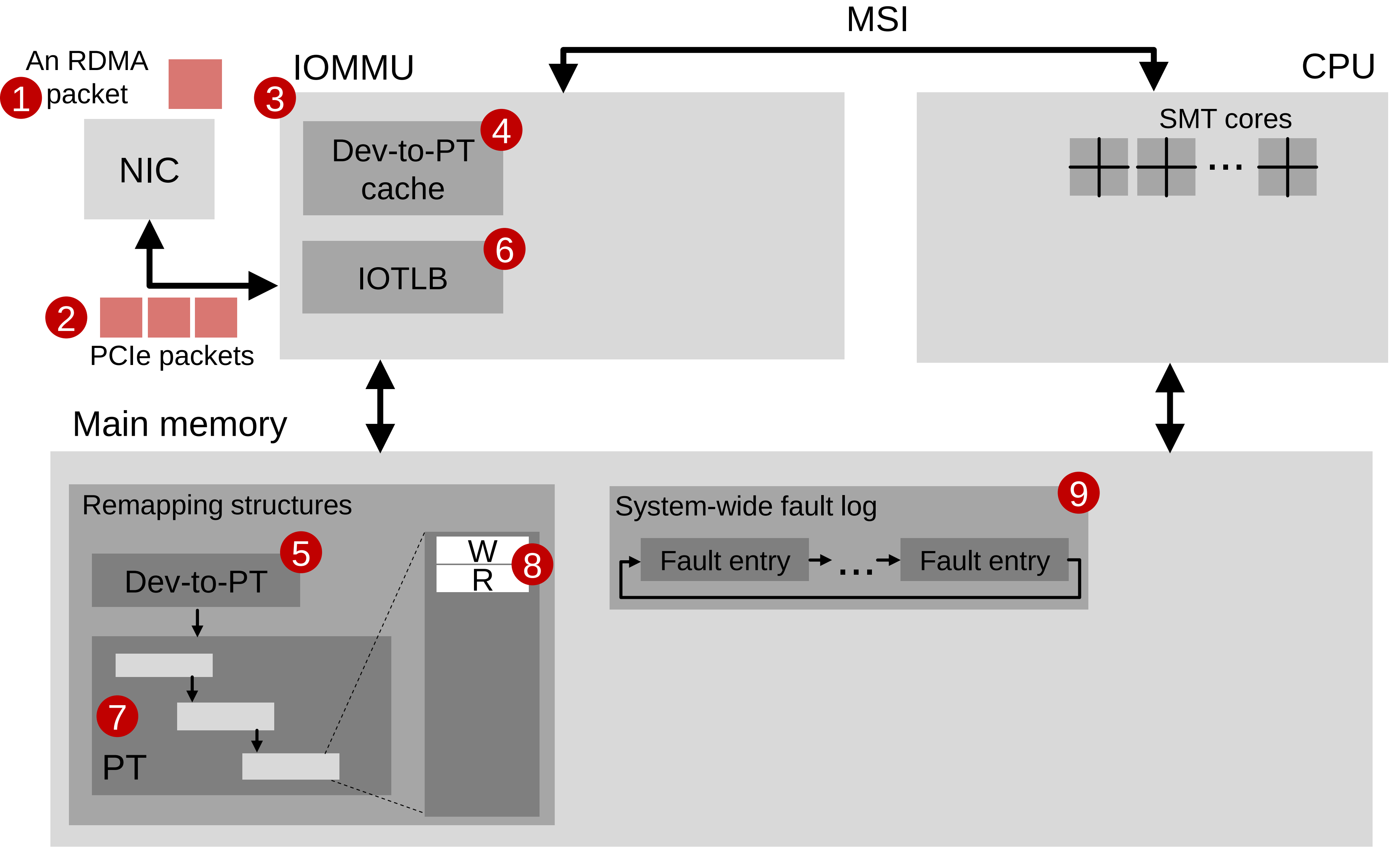

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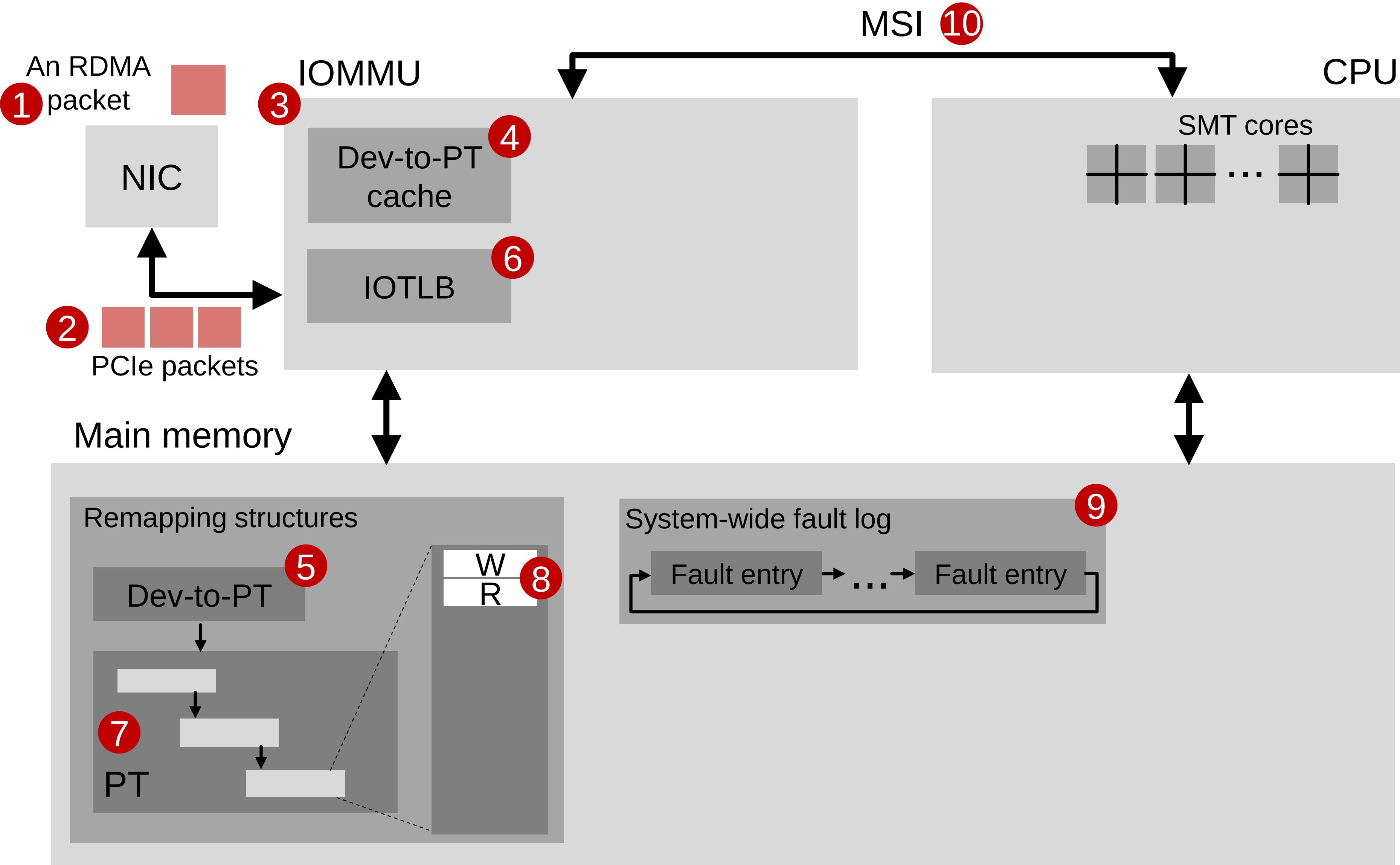

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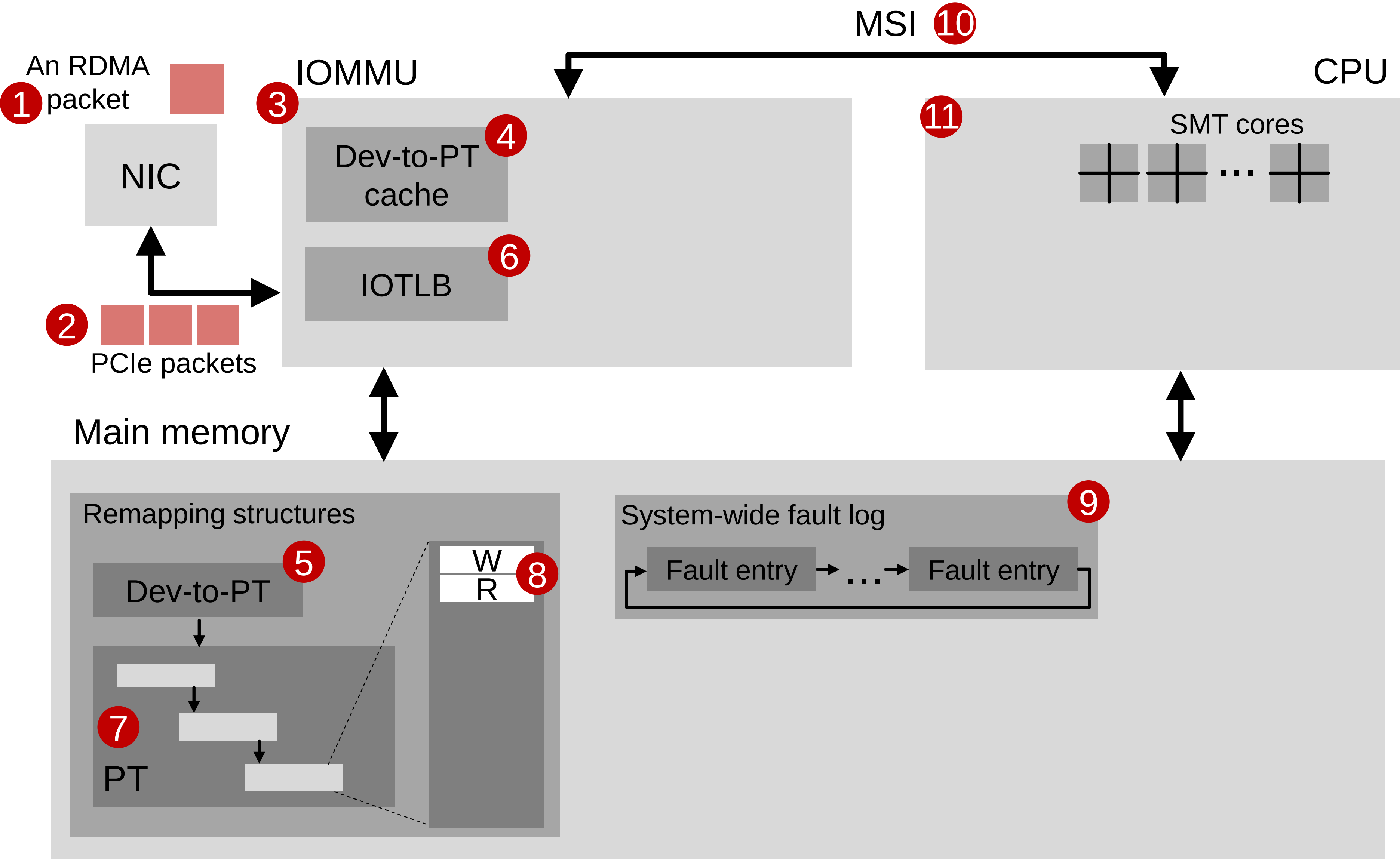

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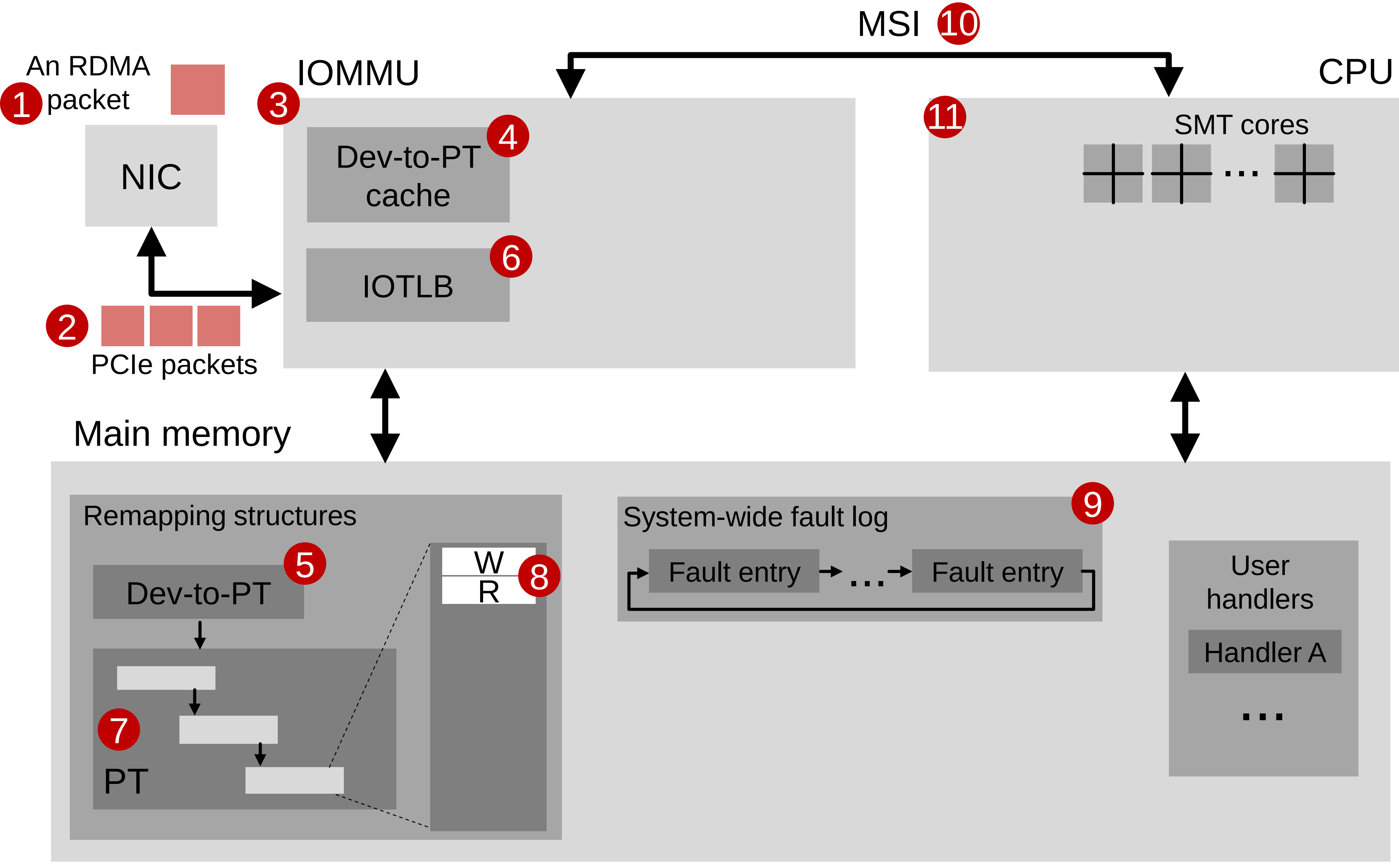

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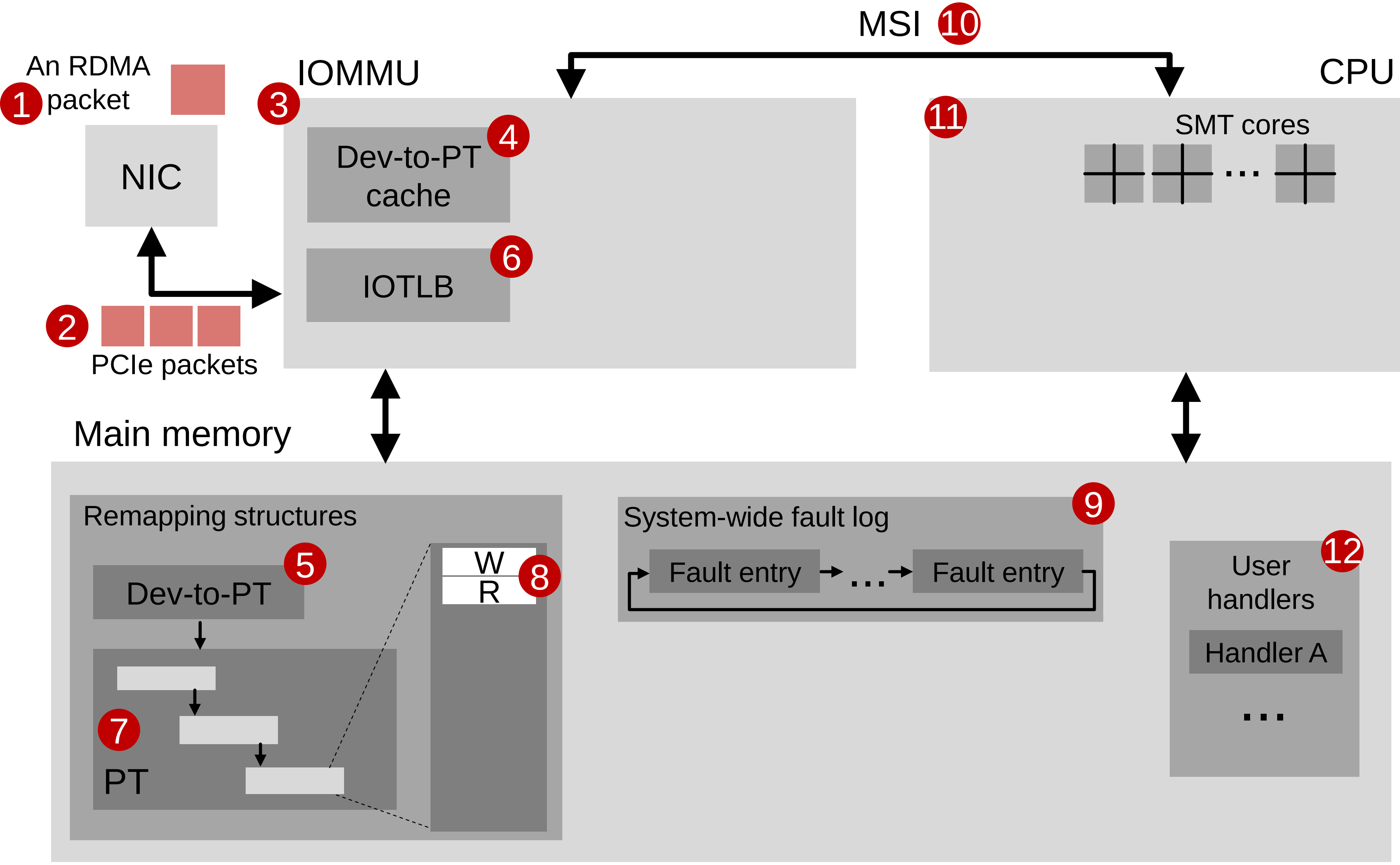

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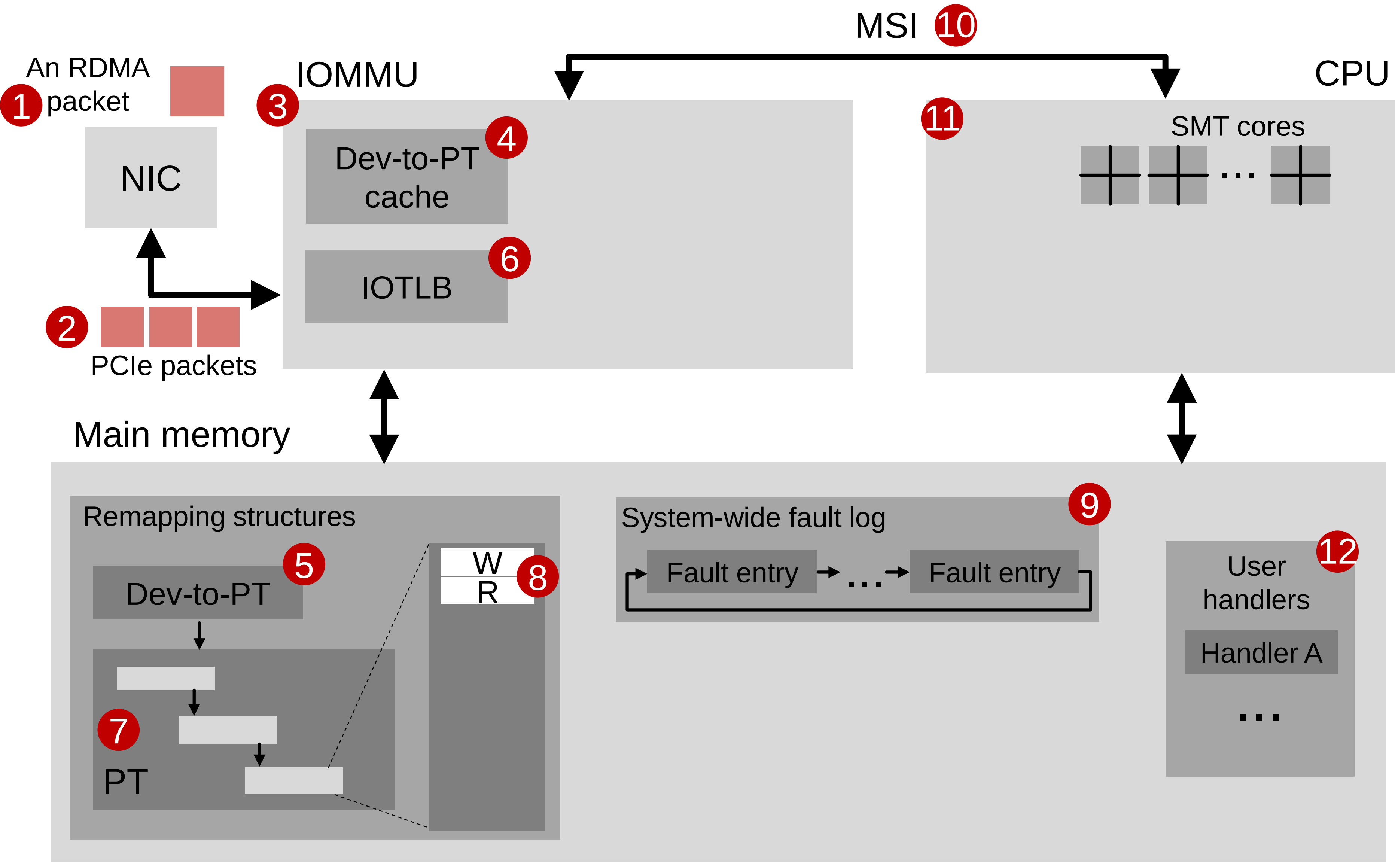

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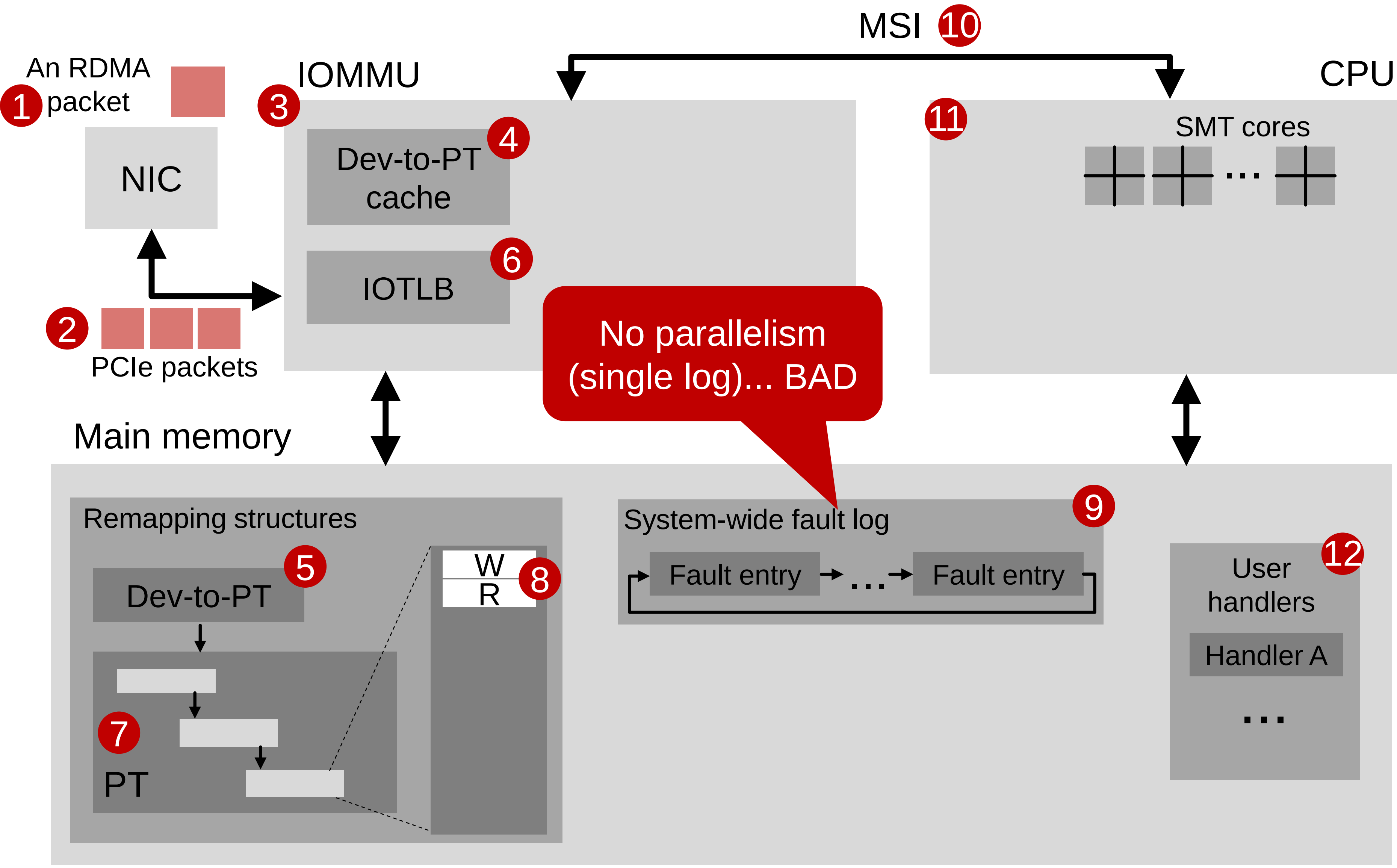

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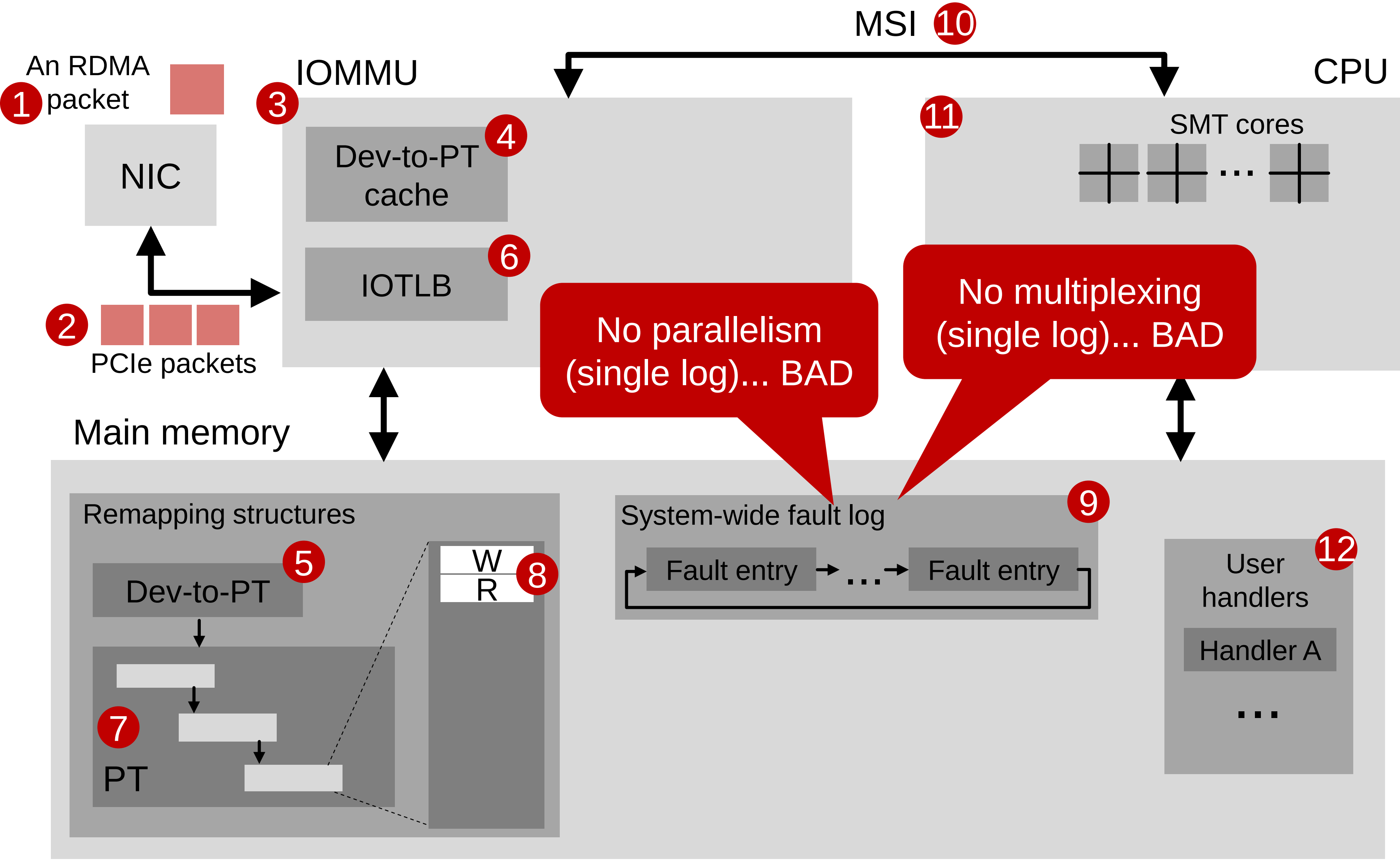

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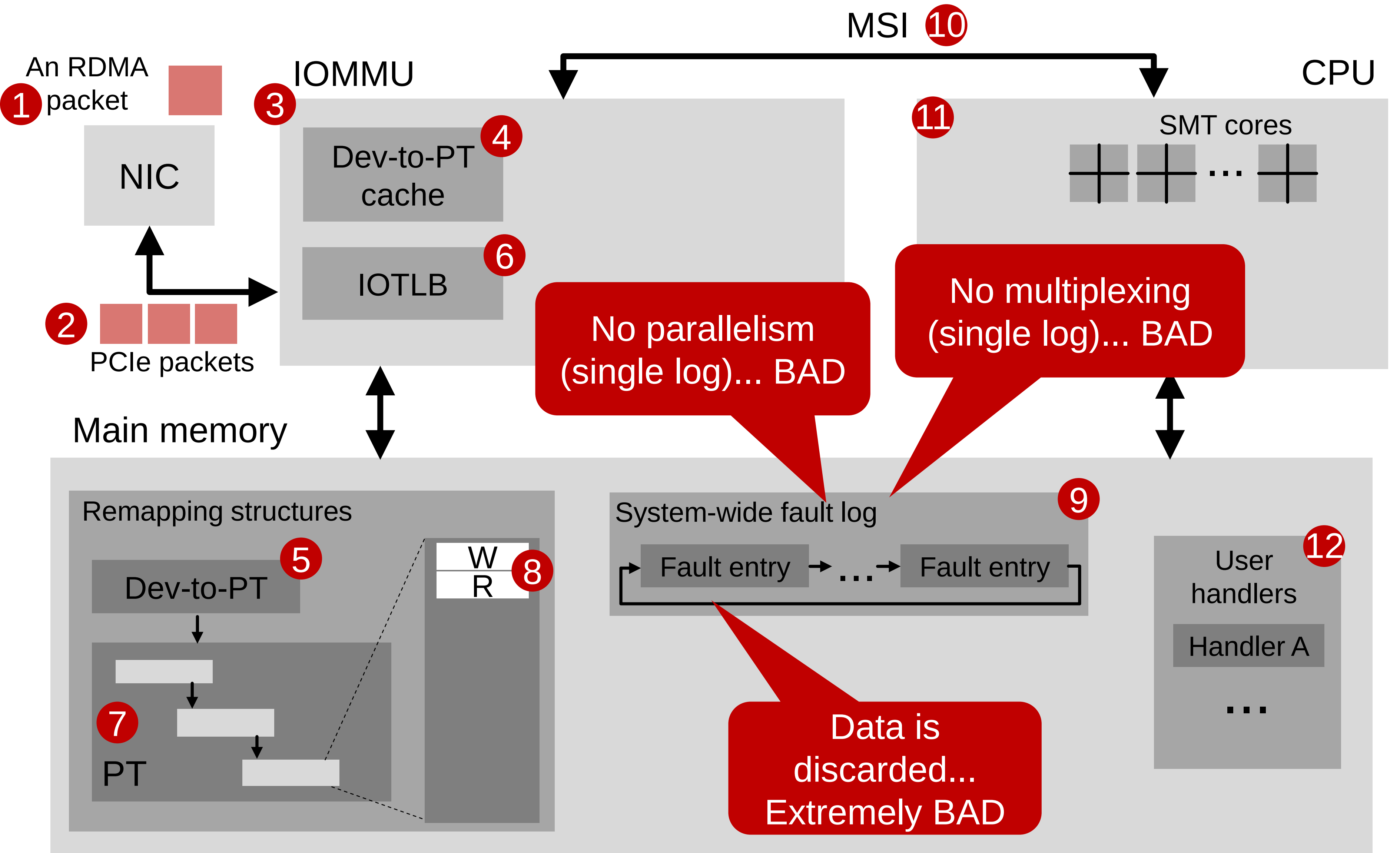
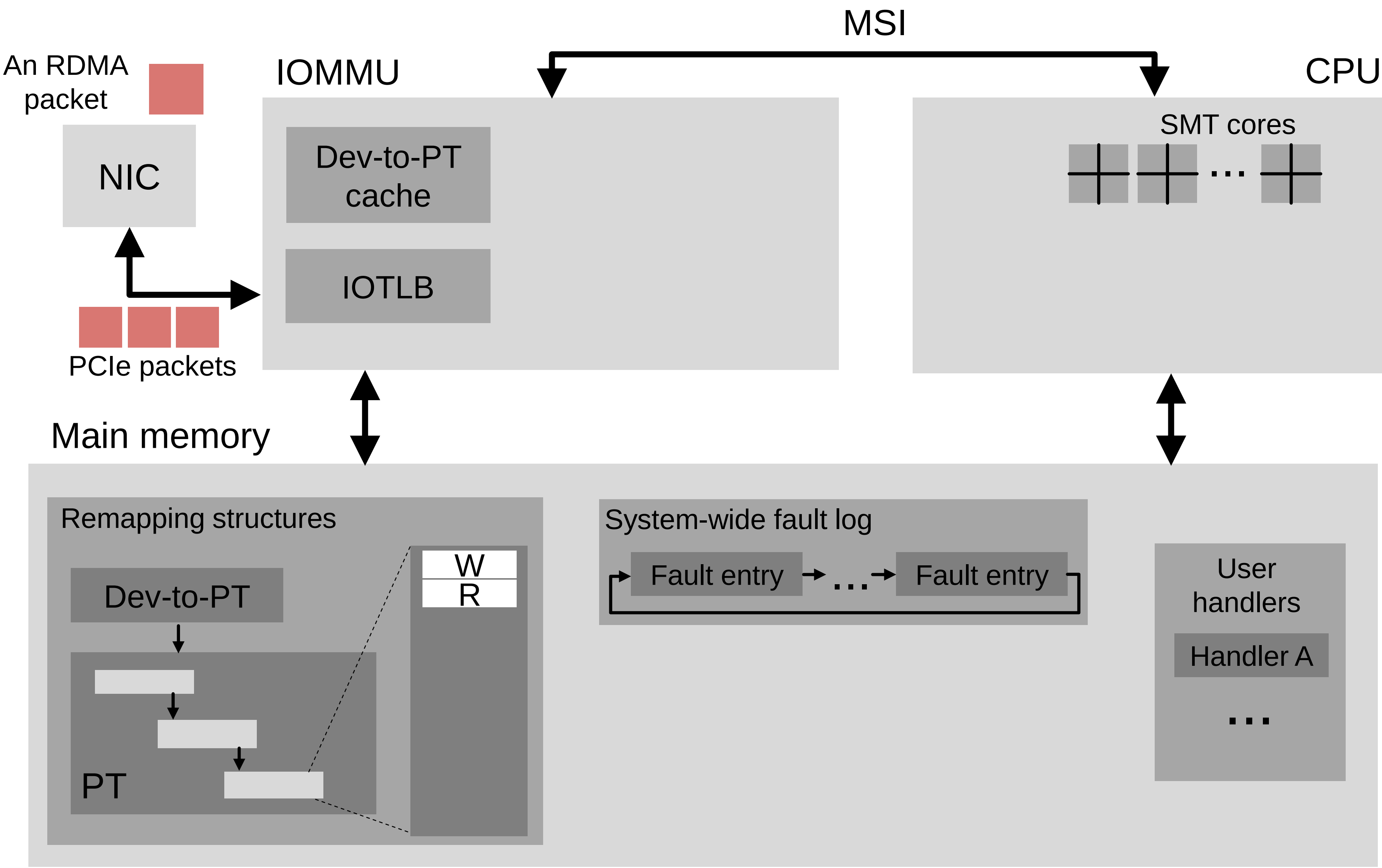


# Active Puts


MSI
An RDMA packet
IOMMU
CPU
NIC
Dev-to-PT cache
IOTLB
SMT cores
...
PCIe packets
Main memory
Remapping structures
W
R
Dev-to-PT
PT
System-wide fault log
Fault entry
...
Fault entry
User handlers
Handler A
...

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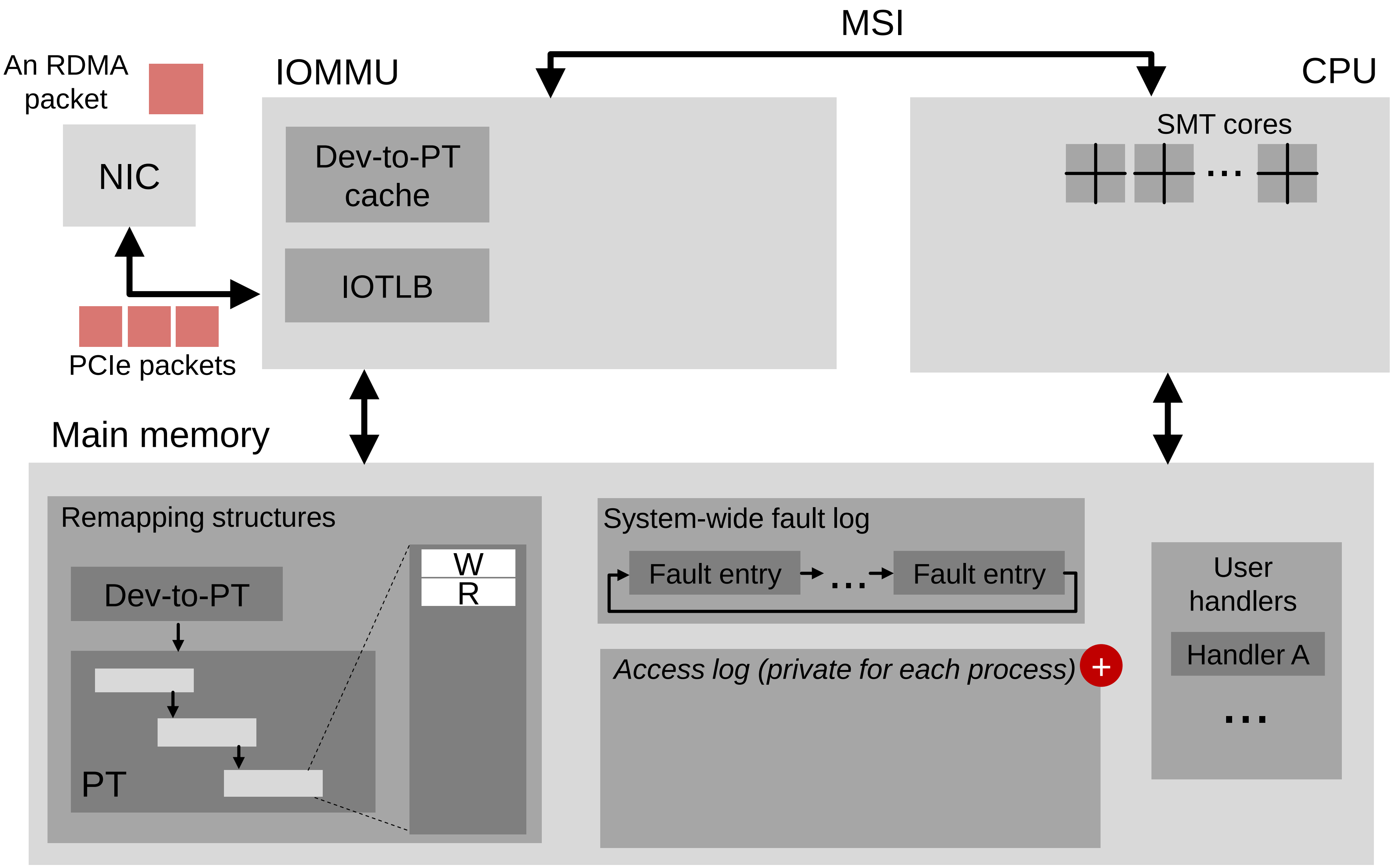
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Fault entry
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Fault entry
Access log (private for each process)
+
User handlers
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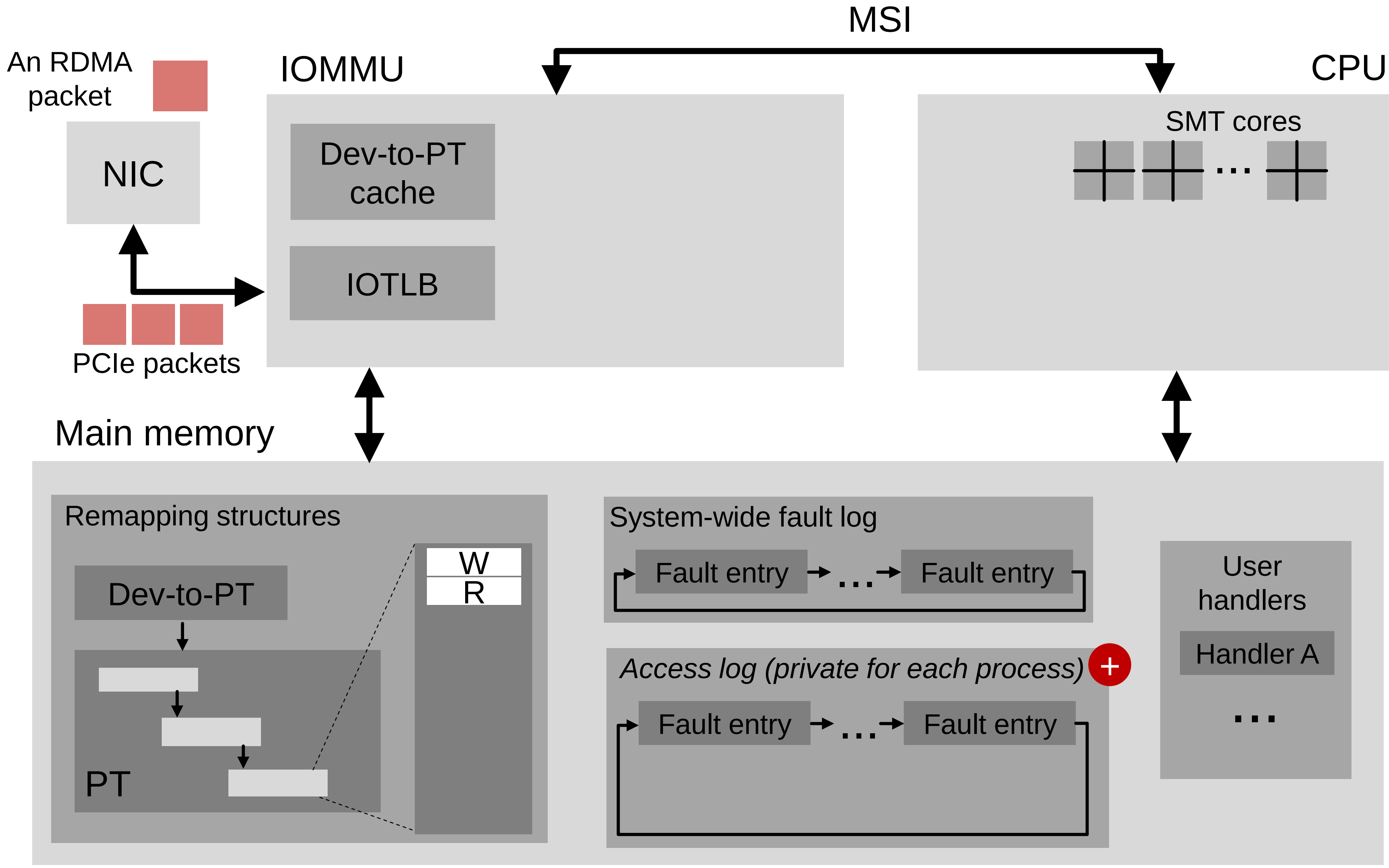
...

# ACTIVE PUTS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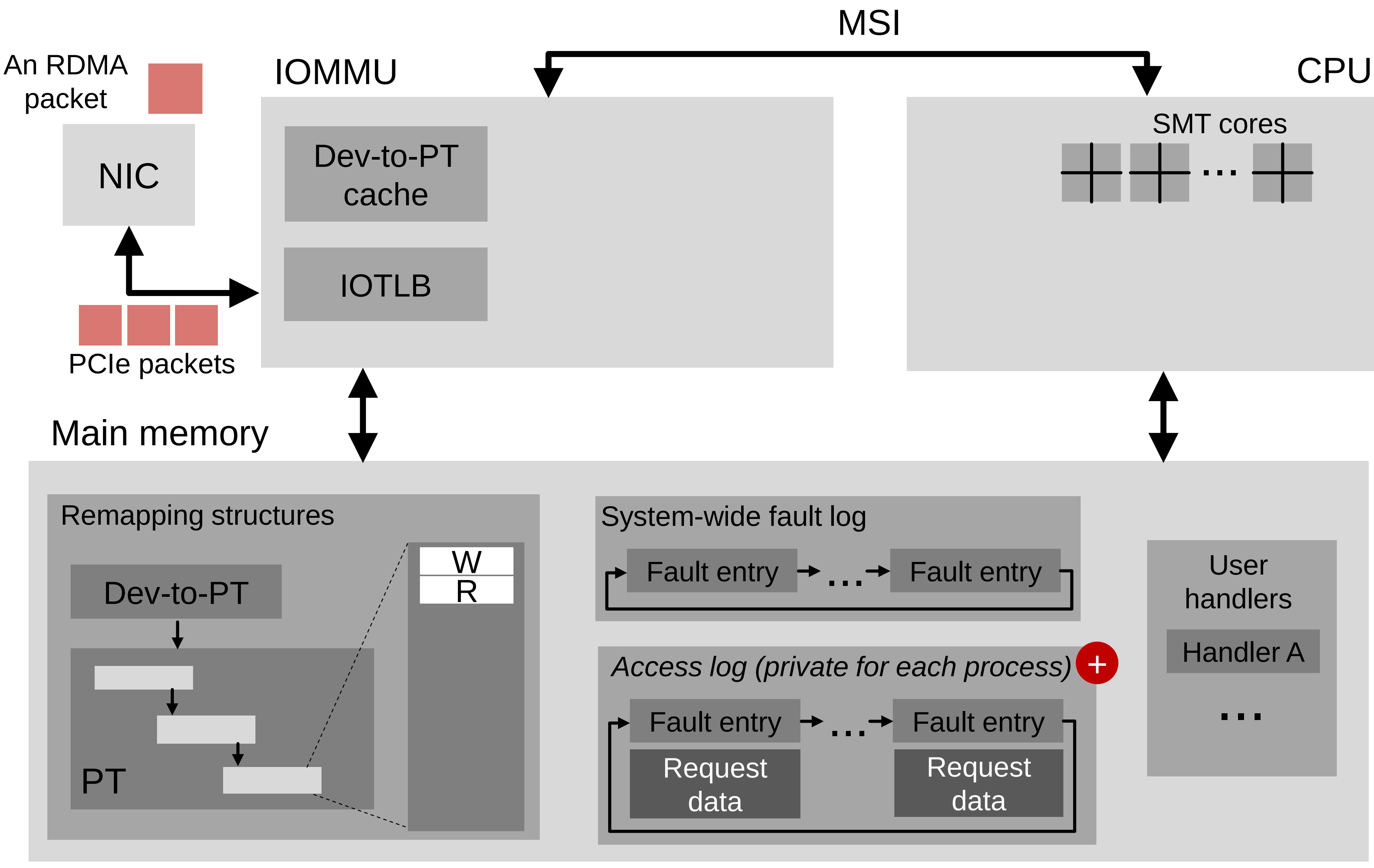
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Request data
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User handlers
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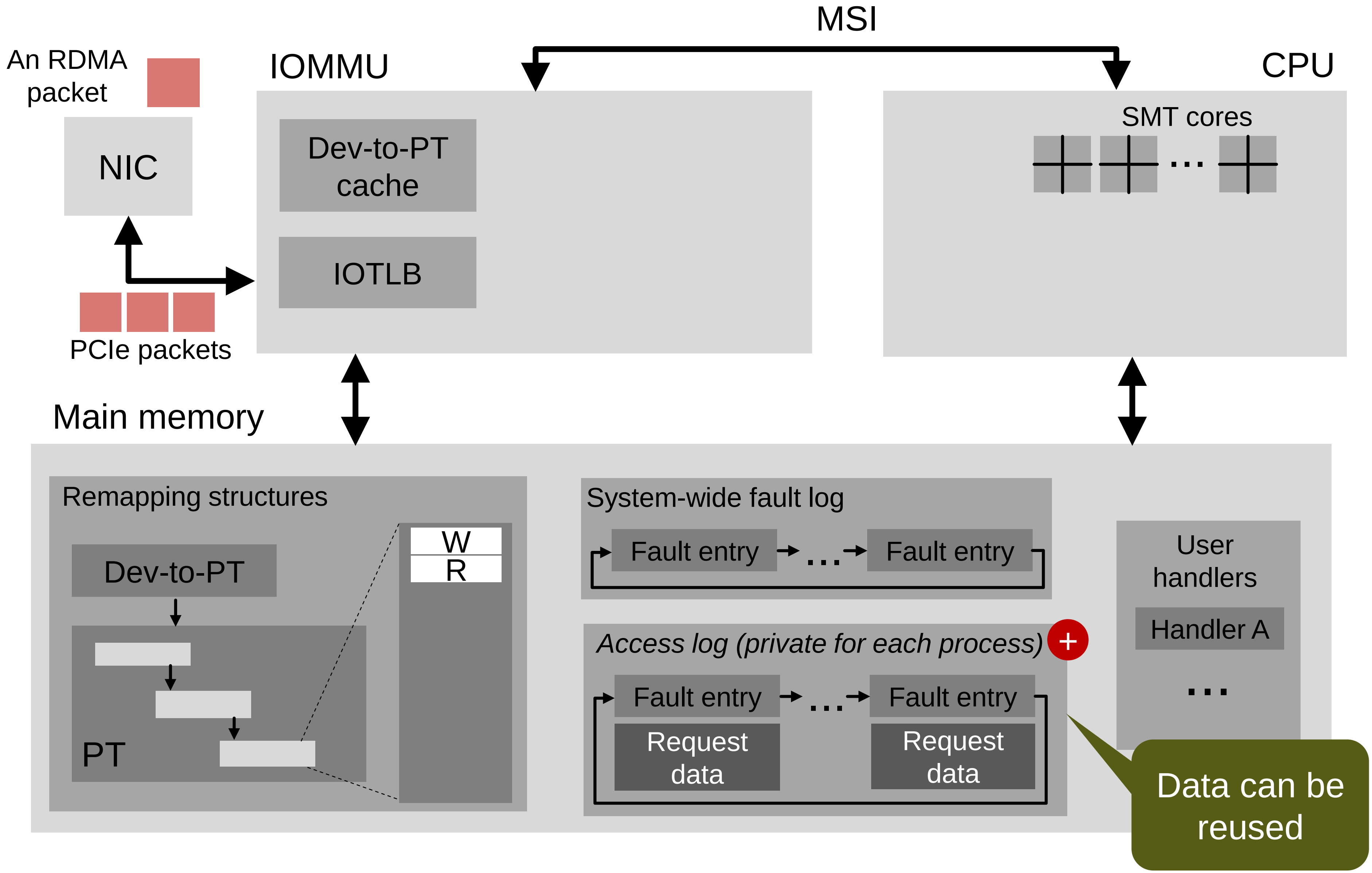
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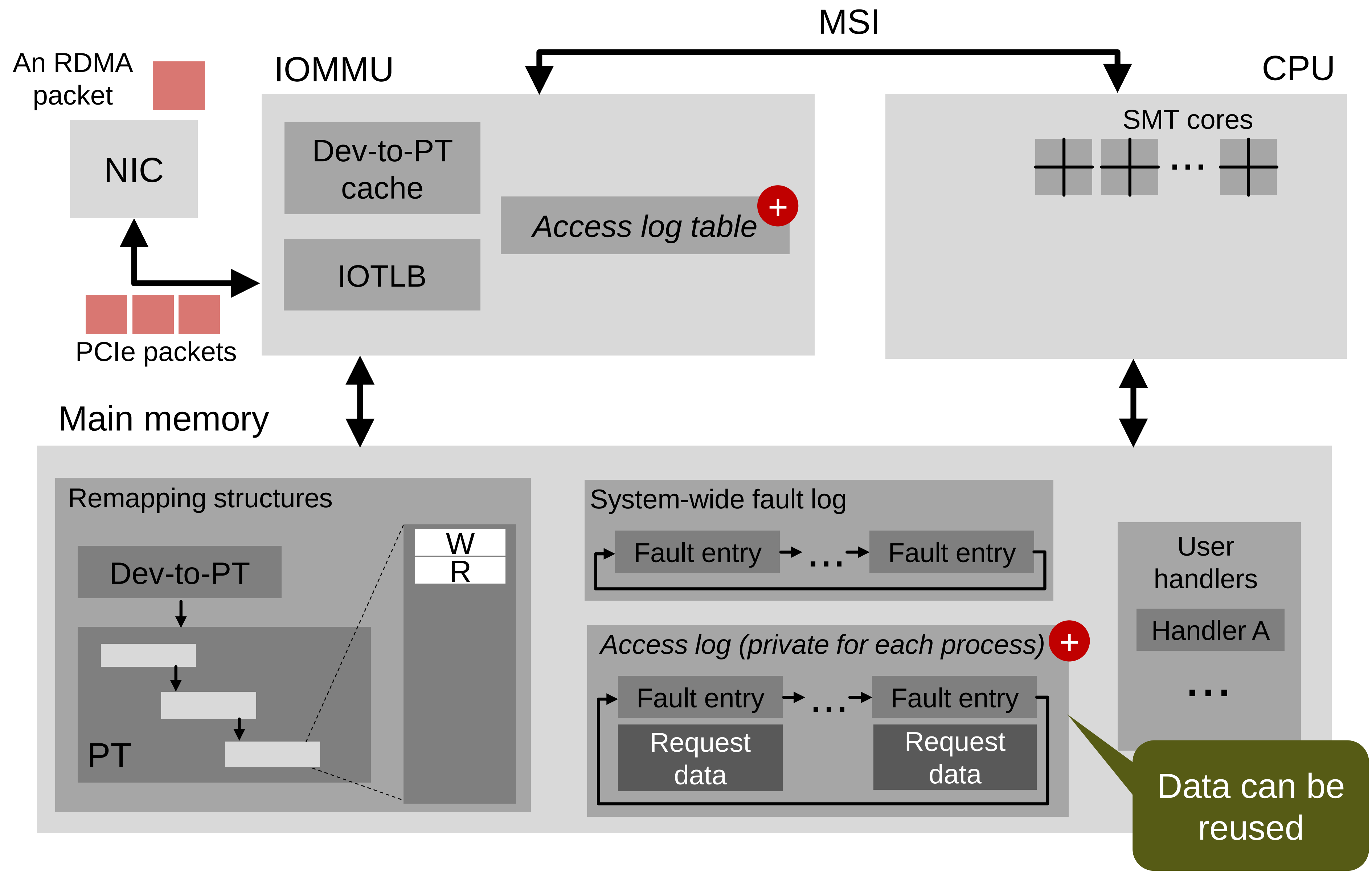
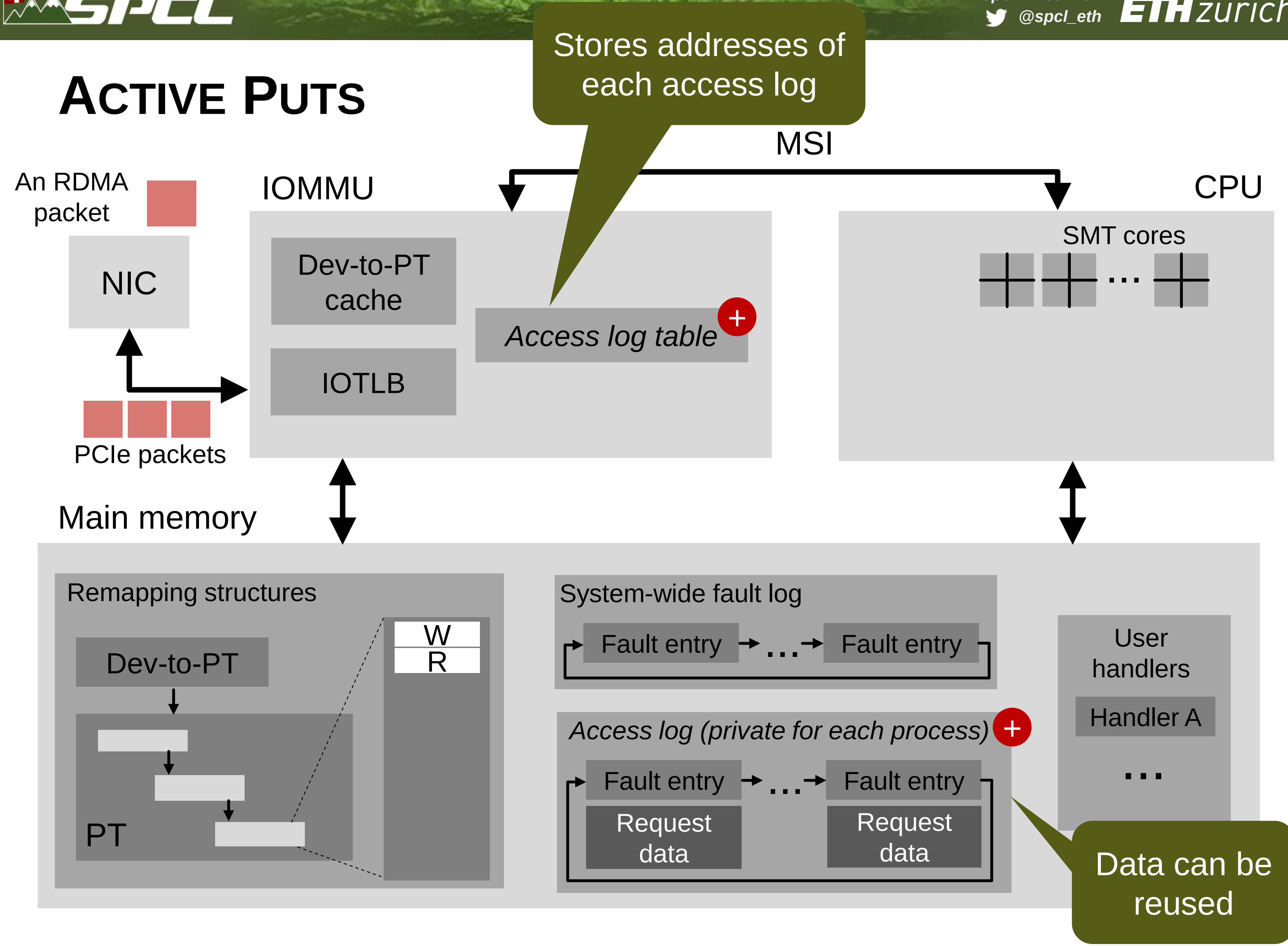
System-wide fault log
Fault entry
Fault entry
Access log (private for each process)
Fault entry
Fault entry
Request data
Request data
User handlers
Handler A
Data can be reused

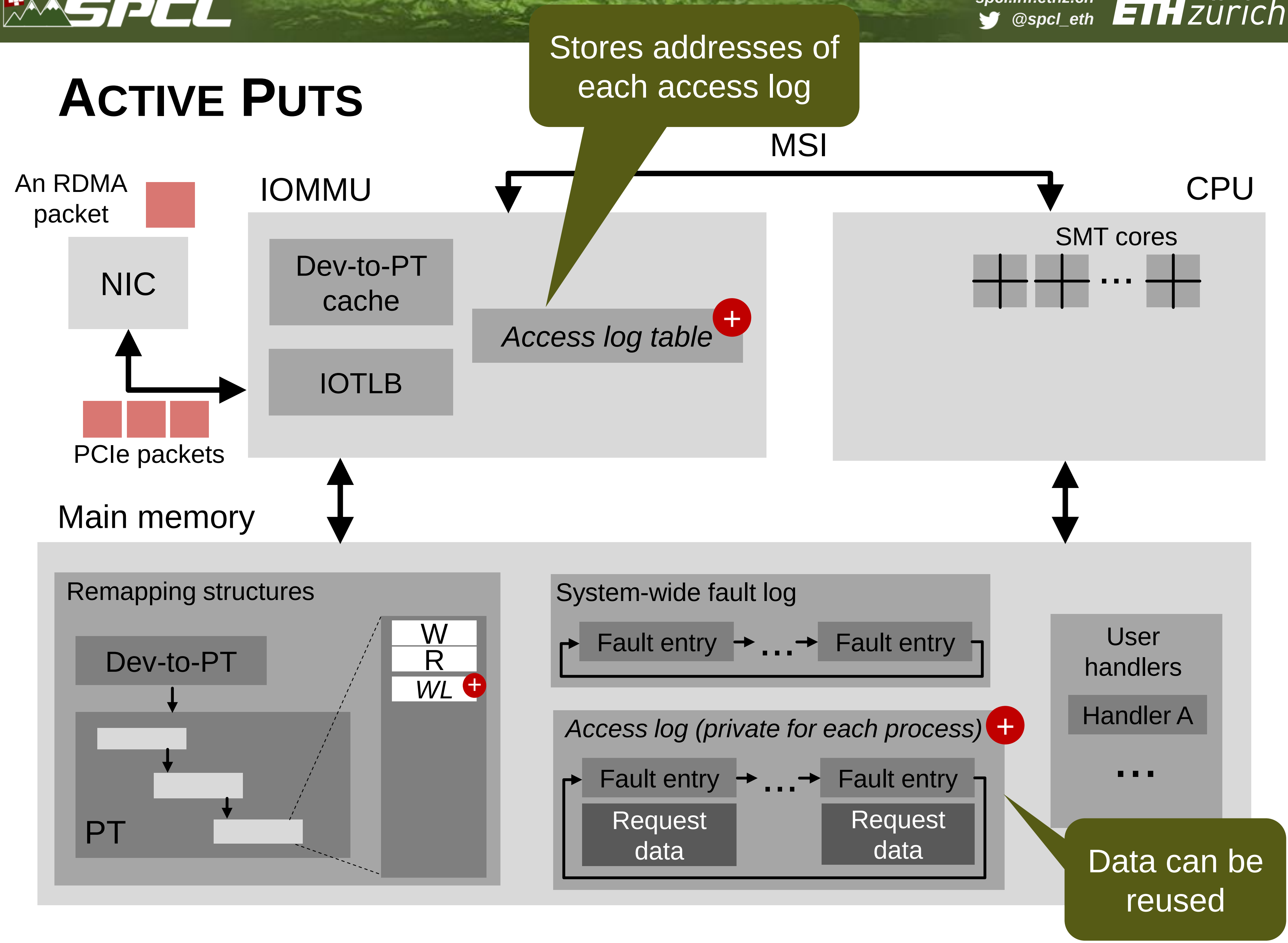
# Active Puts


MSI
An RDMA packet
IOMMU
CPU
NIC
Dev-to-PT cache
IOTLB
Access log table
SMT cores
...
PCIe packets
Main memory
Remapping structures
W
R
Dev-to-PT
PT
System-wide fault log
Fault entry
...
Fault entry
User handlers
Handler A
...
Access log (private for each process)
Fault entry
...
Fault entry
Request data
Request data
Data can be reused

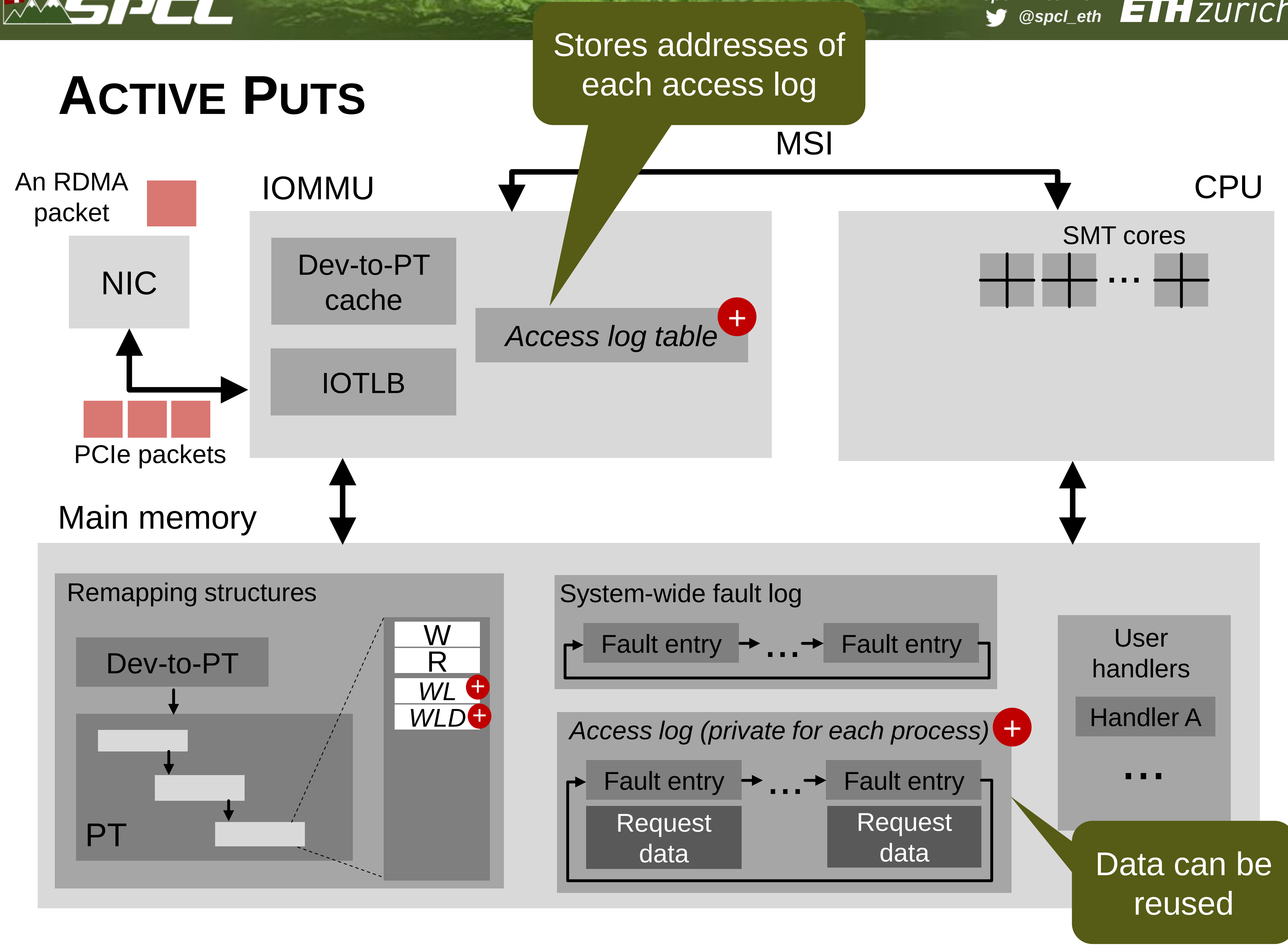
# ACTIVE PUTS


Stores addresses of each access log
MSI
An RDMA packet
NIC
PCIe packets
IOMMU
Dev-to-PT cache
IOTLB
Access log table
+
CPU
SMT cores
...
Main memory
Remapping structures
Dev-to-PT
PT
W
R
System-wide fault log
Fault entry
...
Fault entry
Access log (private for each process)
+
Fault entry
...
Fault entry
Request data
Request data
User handlers
Handler A
...
Data can be reused

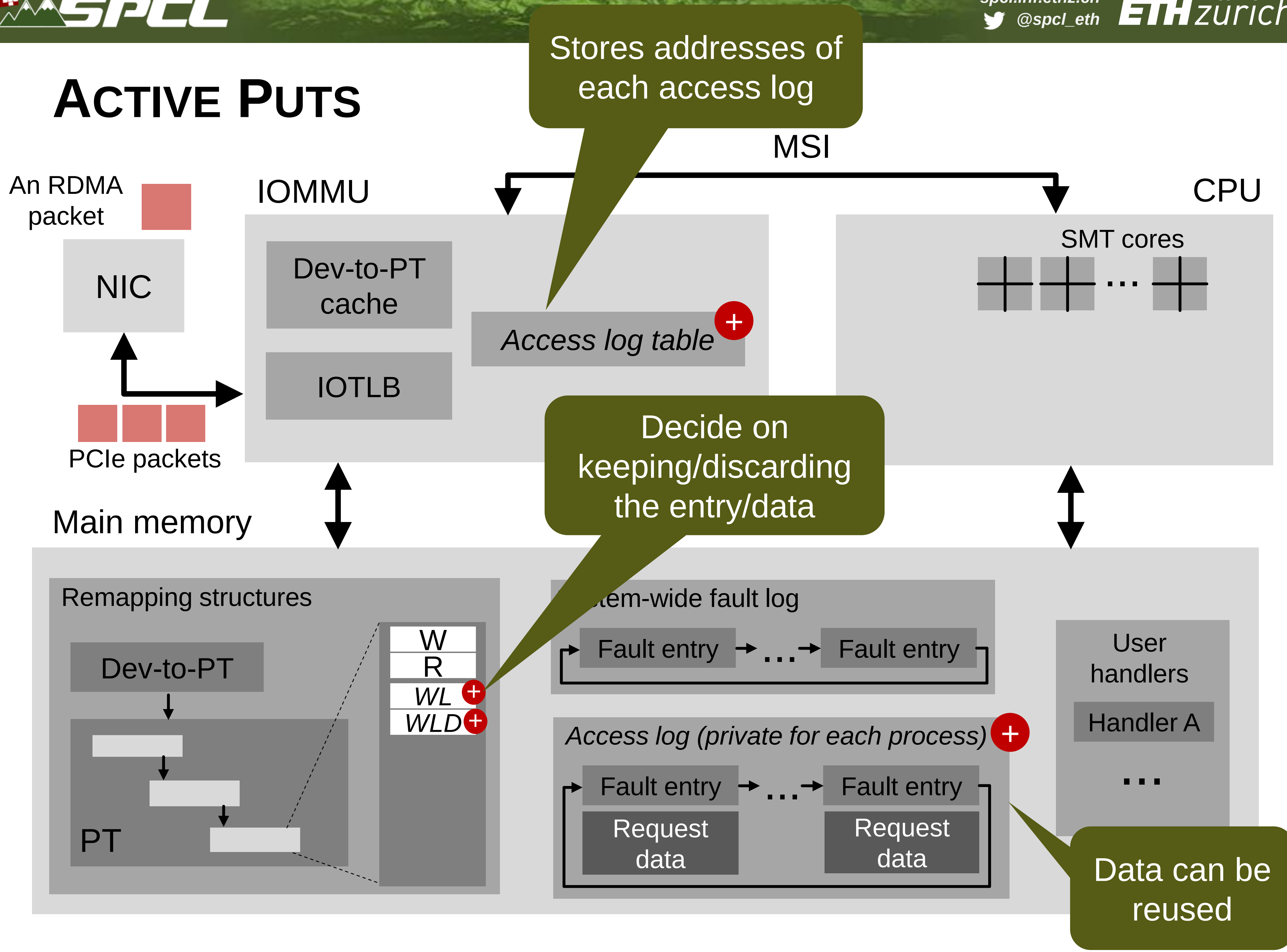
# Active Puts


Stores addresses of each access log
MSI
An RDMA packet
IOMMU
CPU
NIC
Dev-to-PT cache
SMT cores
…
Access log table
+
IOTLB
PCIe packets
Main memory
Remapping structures
W
R
WL
+
Dev-to-PT
PT
System-wide fault log
Fault entry
…
Fault entry
Access log (private for each process)
+
Fault entry
…
Fault entry
Request data
Request data
User handlers
Handler A
…
Data can be reused

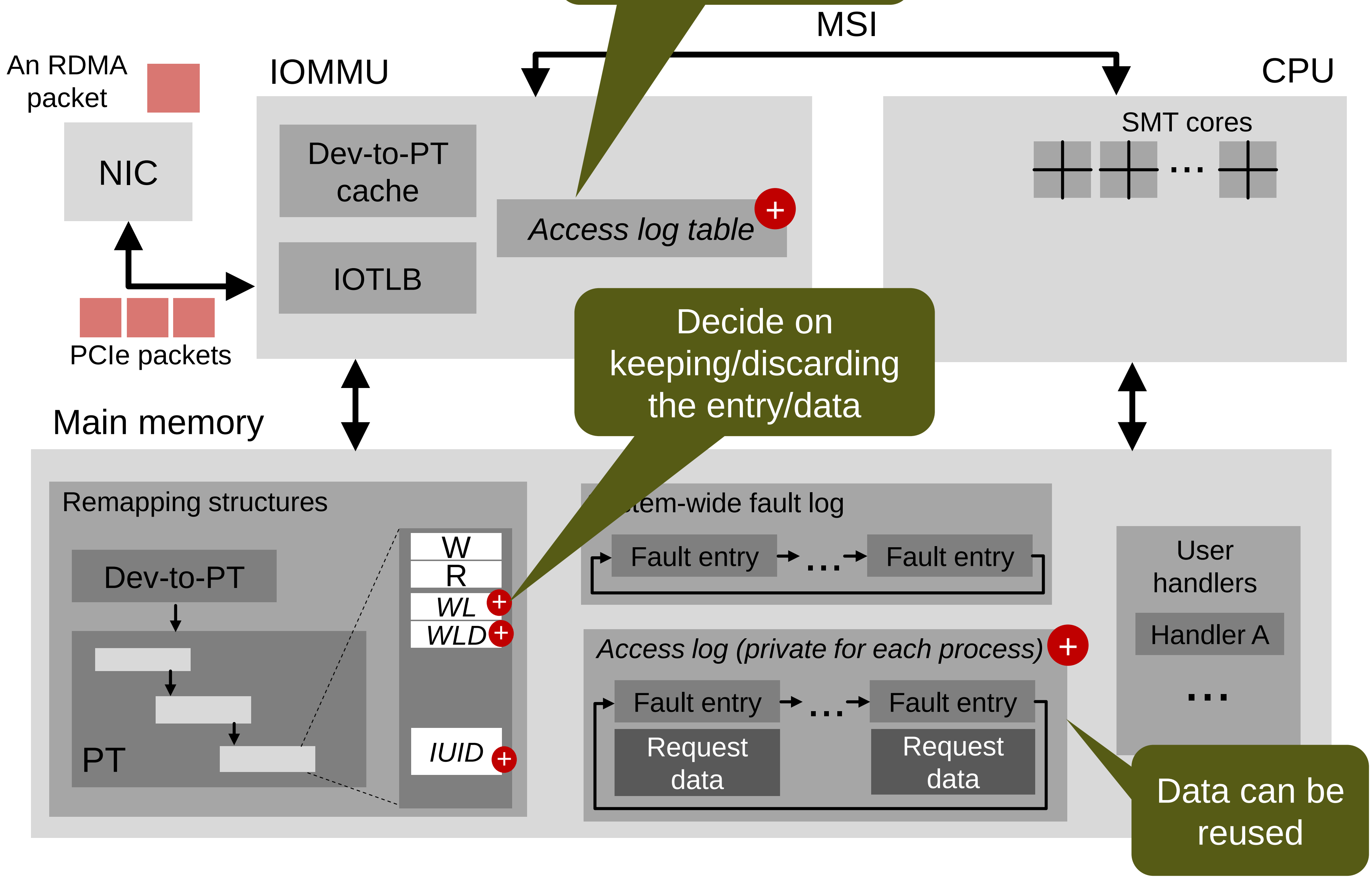
# Active Puts


Stores addresses of each access log
MSI
An RDMA packet
IOMMU
CPU
NIC
Dev-to-PT cache
IOTLB
Access log table
+
SMT cores
...
PCIe packets
Main memory
Remapping structures
Dev-to-PT
PT
W
R
WL
WLD
System-wide fault log
Fault entry
...
Fault entry
User handlers
Handler A
...
Access log (private for each process)
Fault entry
...
Fault entry
Request data
Request data
Data can be reused

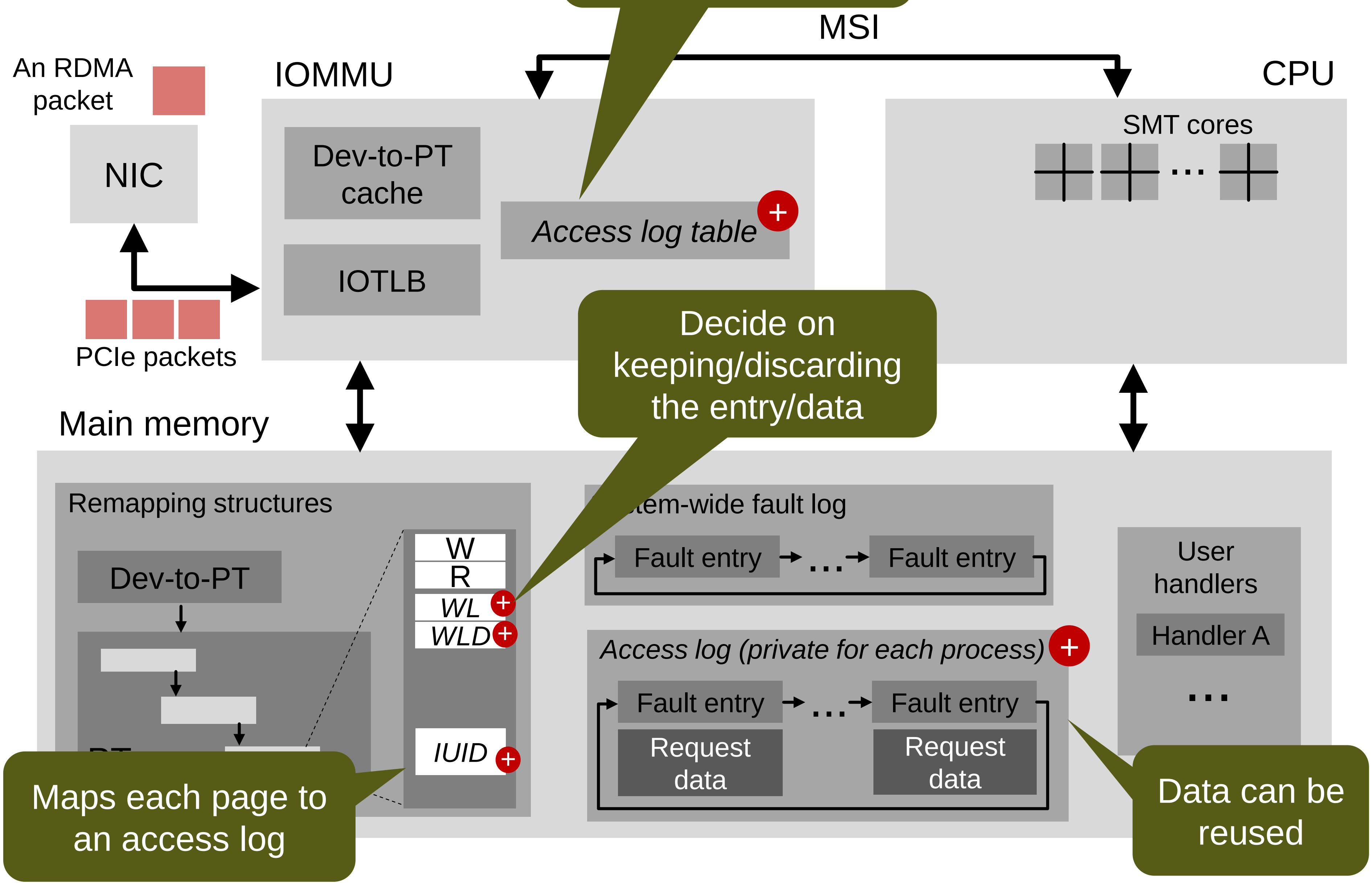
# Active Puts


Stores addresses of each access log
MSI
An RDMA packet
NIC
PCIe packets
IOMMU
Dev-to-PT cache
IOTLB
Access log table
CPU
SMT cores
...
Decide on keeping/discarding the entry/data
Main memory
Remapping structures
Dev-to-PT
PT
W
R
WL
WLD
tem-wide fault log
Fault entry
...
Fault entry
Access log (private for each process)
Fault entry
...
Fault entry
Request data
Request data
User handlers
Handler A
...
Data can be reused

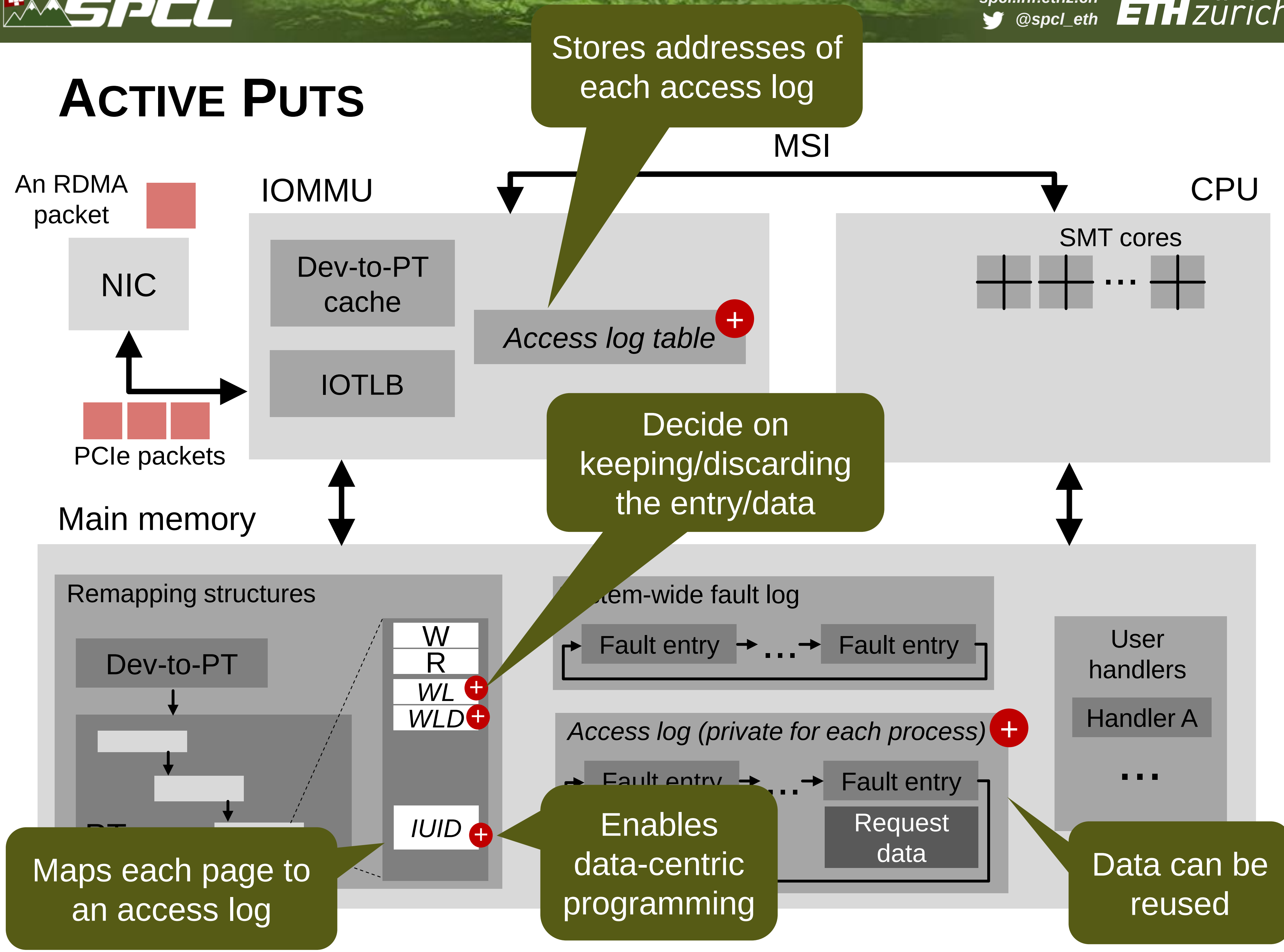
# Active Puts


Stores addresses of each access log
MSI
An RDMA packet
IOMMU
CPU
NIC
Dev-to-PT cache
IOTLB
Access log table
SMT cores
...
PCIe packets
Decide on keeping/discarding the entry/data
Main memory
Remapping structures
Dev-to-PT
PT
W
R
WL
WLD
IUID
tem-wide fault log
Fault entry
...
Fault entry
Access log (private for each process)
Fault entry
...
Fault entry
Request data
Request data
User handlers
Handler A
...
Data can be reused

# ACTIVE PUTS

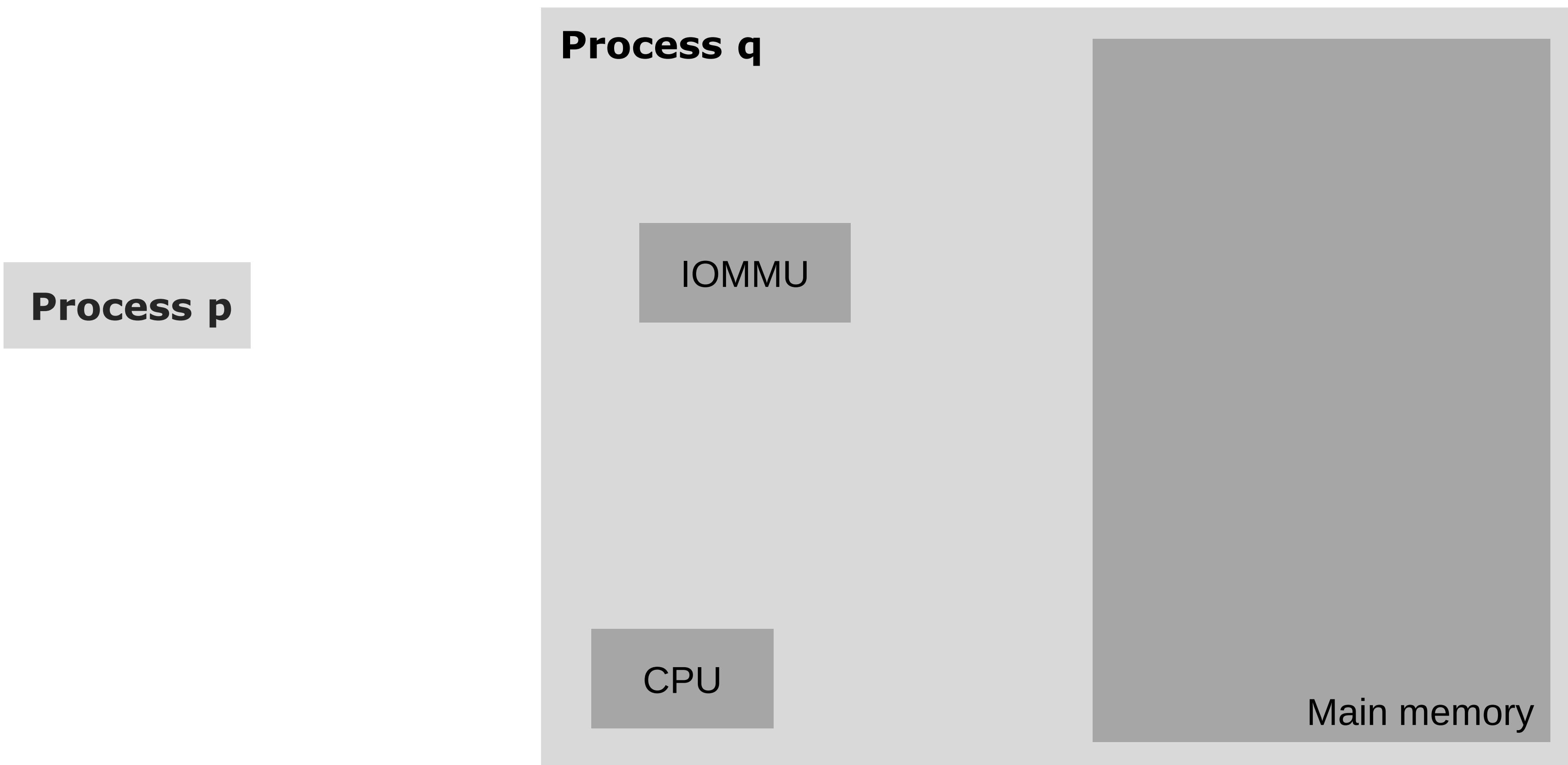

Stores addresses of each access log
MSI
An RDMA packet
IOMMU
CPU
NIC
Dev-to-PT cache
Access log table
IOTLB
SMT cores
PCIe packets
Decide on keeping/discarding the entry/data
Main memory
Remapping structures
tem-wide fault log
Dev-to-PT
W
R
WL
WLD
IUID
Fault entry
Fault entry
User handlers
Handler A
Access log (private for each process)
Fault entry
Fault entry
Request data
Request data
Maps each page to an access log
Data can be reused

# Active Puts

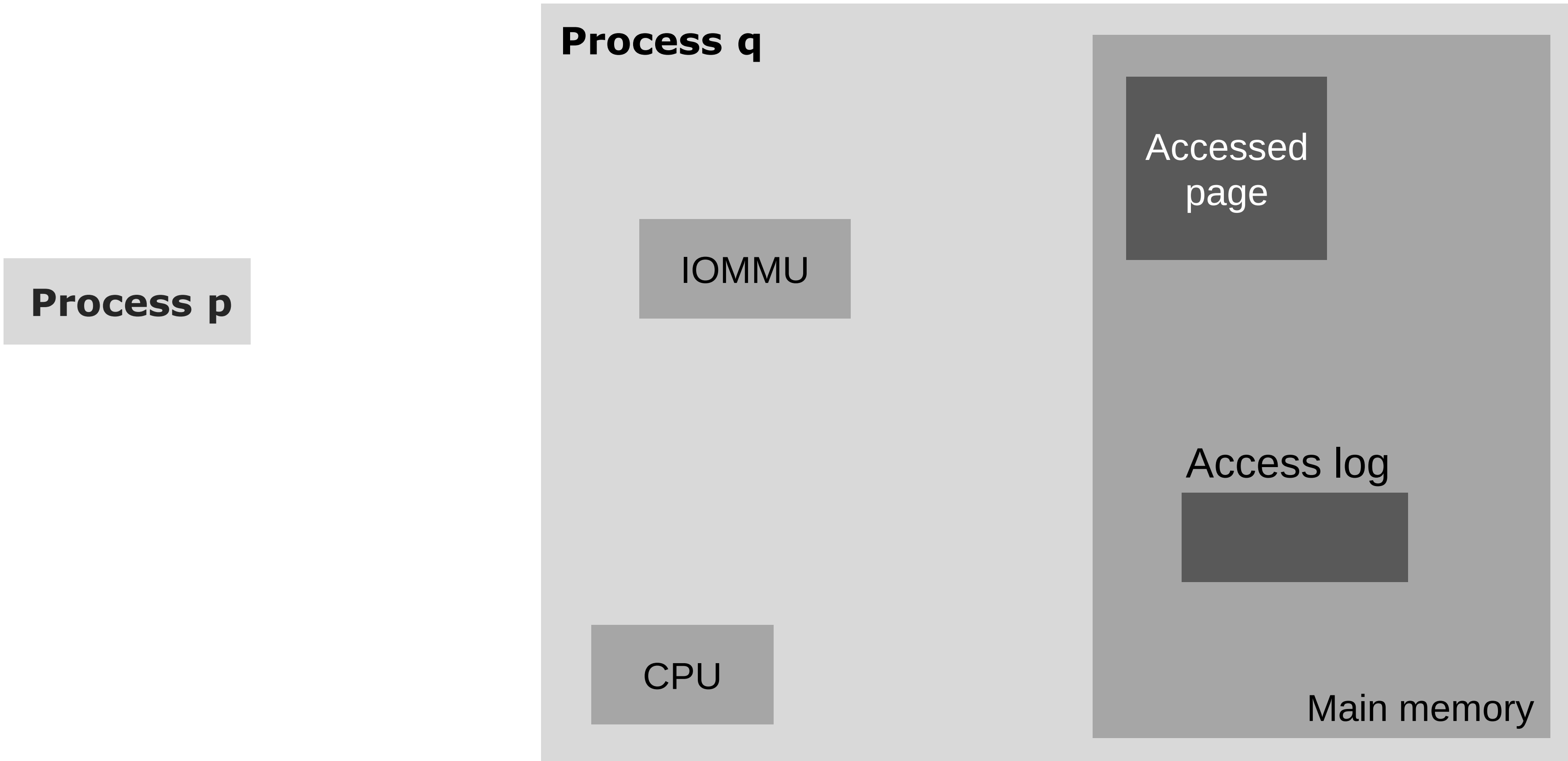

Stores addresses of each access log
MSI
An RDMA packet
IOMMU
CPU
NIC
Dev-to-PT cache
IOTLB
Access log table
SMT cores
PCIe packets
Decide on keeping/discarding the entry/data
Main memory
Remapping structures
Dev-to-PT
W
R
WL
WLD
IUID
tem-wide fault log
Fault entry
Fault entry
Access log (private for each process)
Fault entry
Fault entry
Request data
User handlers
Handler A
Maps each page to an access log
Enables data-centric programming
Data can be reused

# ACTIVE PUTS

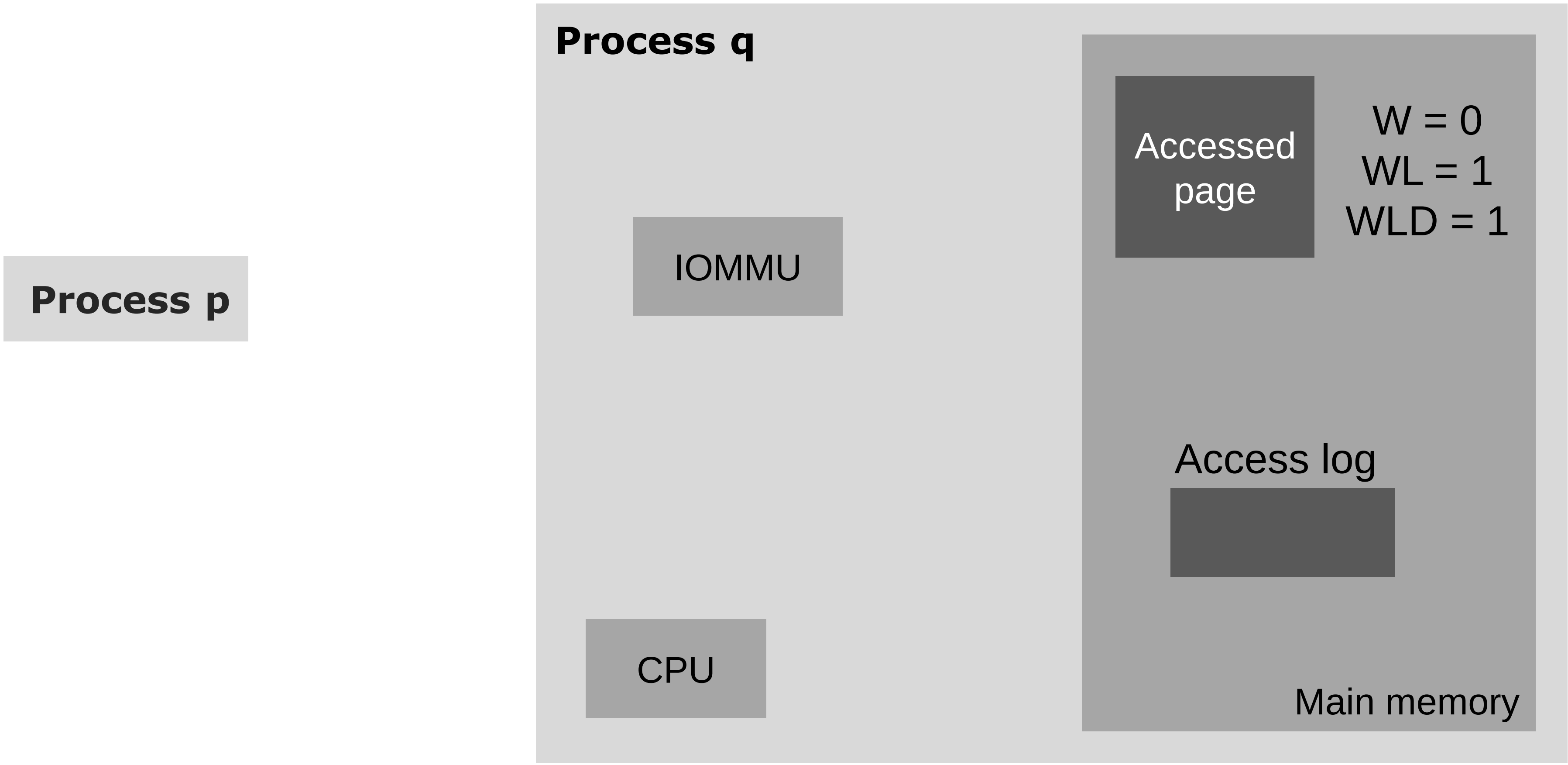
# ACTIVE PUTS



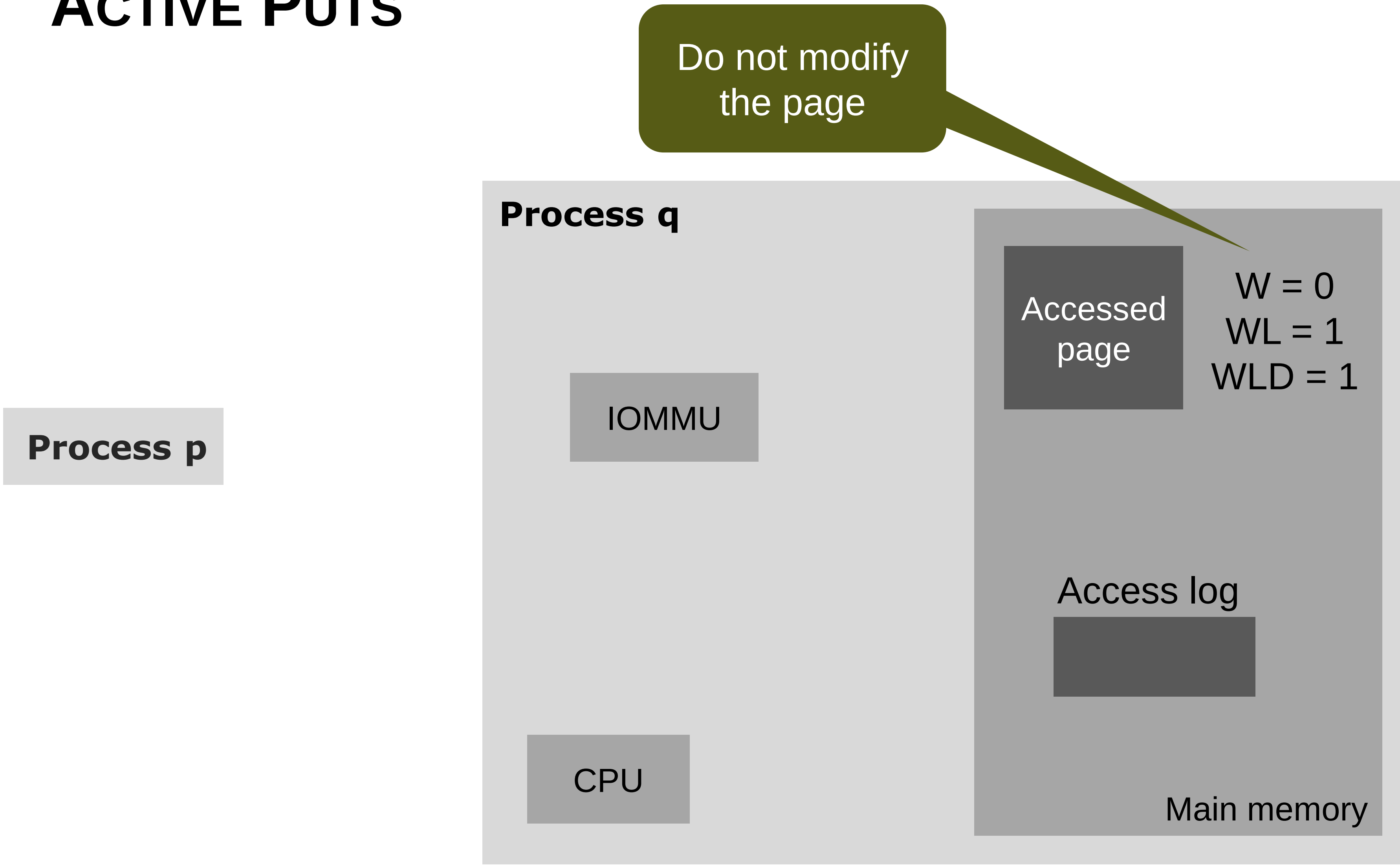
# Active Puts


Process p
Process q
IOMMU
CPU
Accessed page
Access log
Main memory

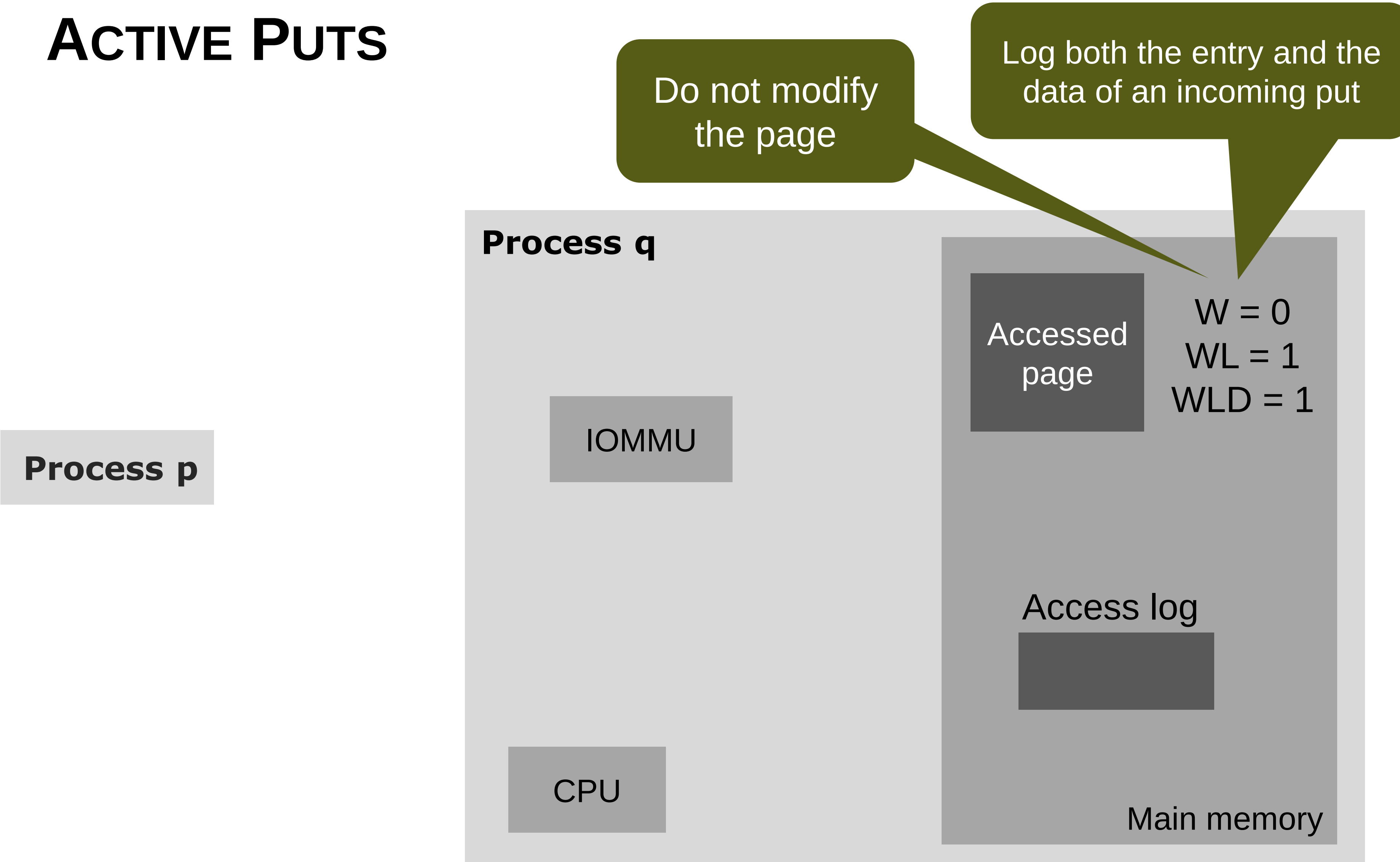
# Active Puts


Process q
Accessed page
W = 0
WL = 1
WLD = 1
IOMMU
Process p
Access log
CPU
Main memory

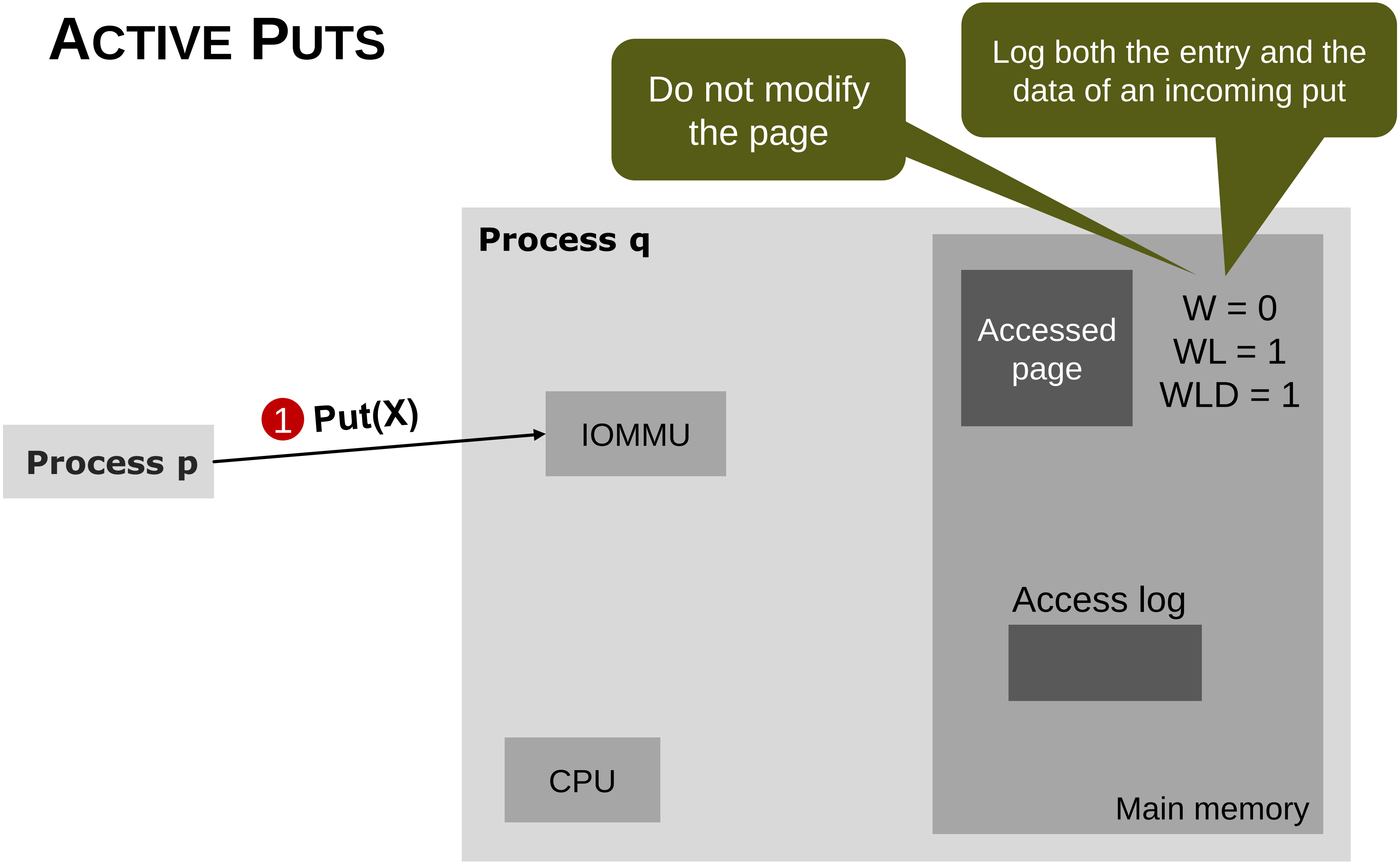
# Active Puts


Do not modify the page
Process q
Accessed page
W = 0
WL = 1
WLD = 1
IOMMU
Process p
Access log
CPU
Main memory

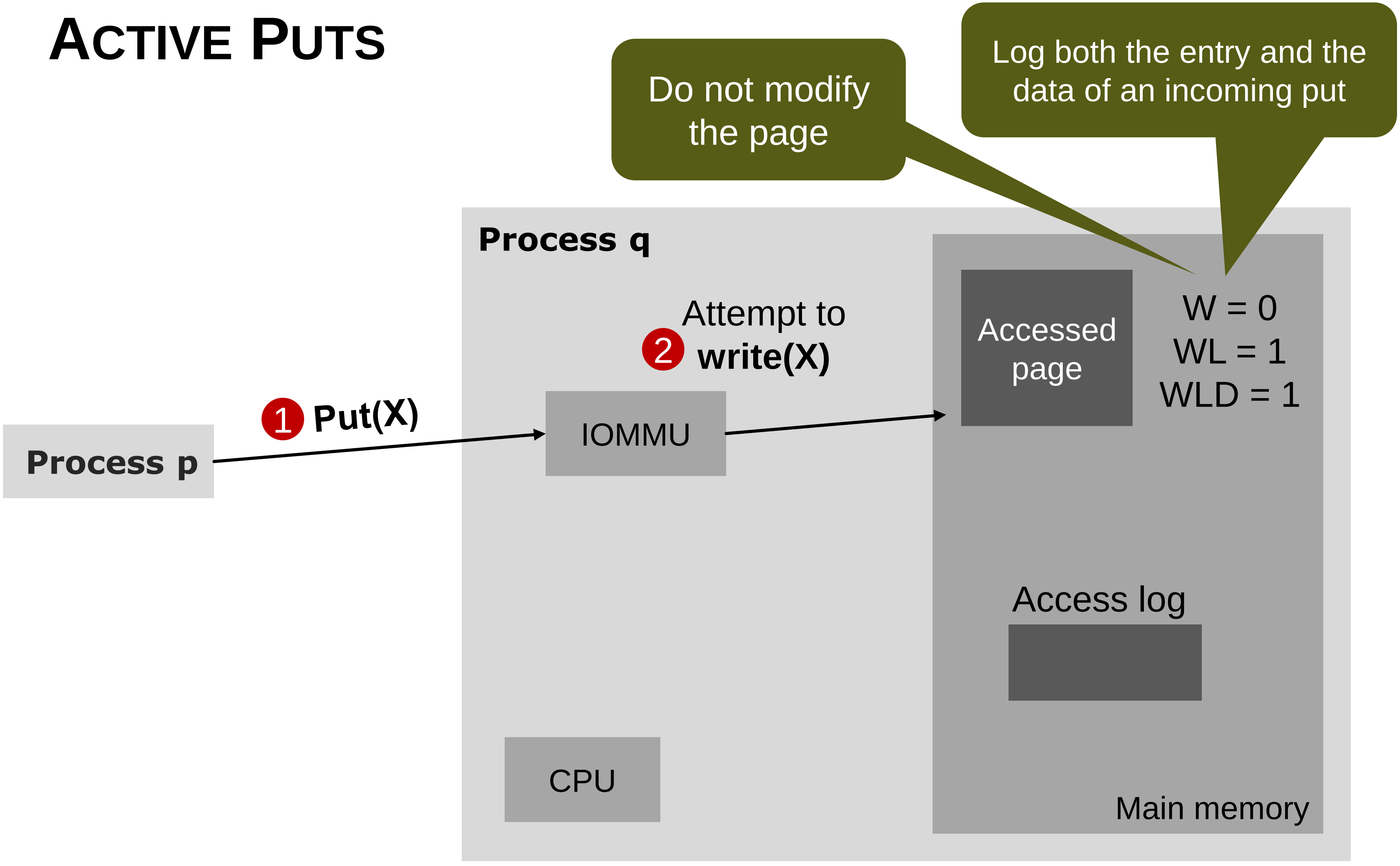
# Active Puts


Do not modify the page
Log both the entry and the data of an incoming put
Process q
Accessed page
W = 0
WL = 1
WLD = 1
IOMMU
Process p
Access log
CPU
Main memory

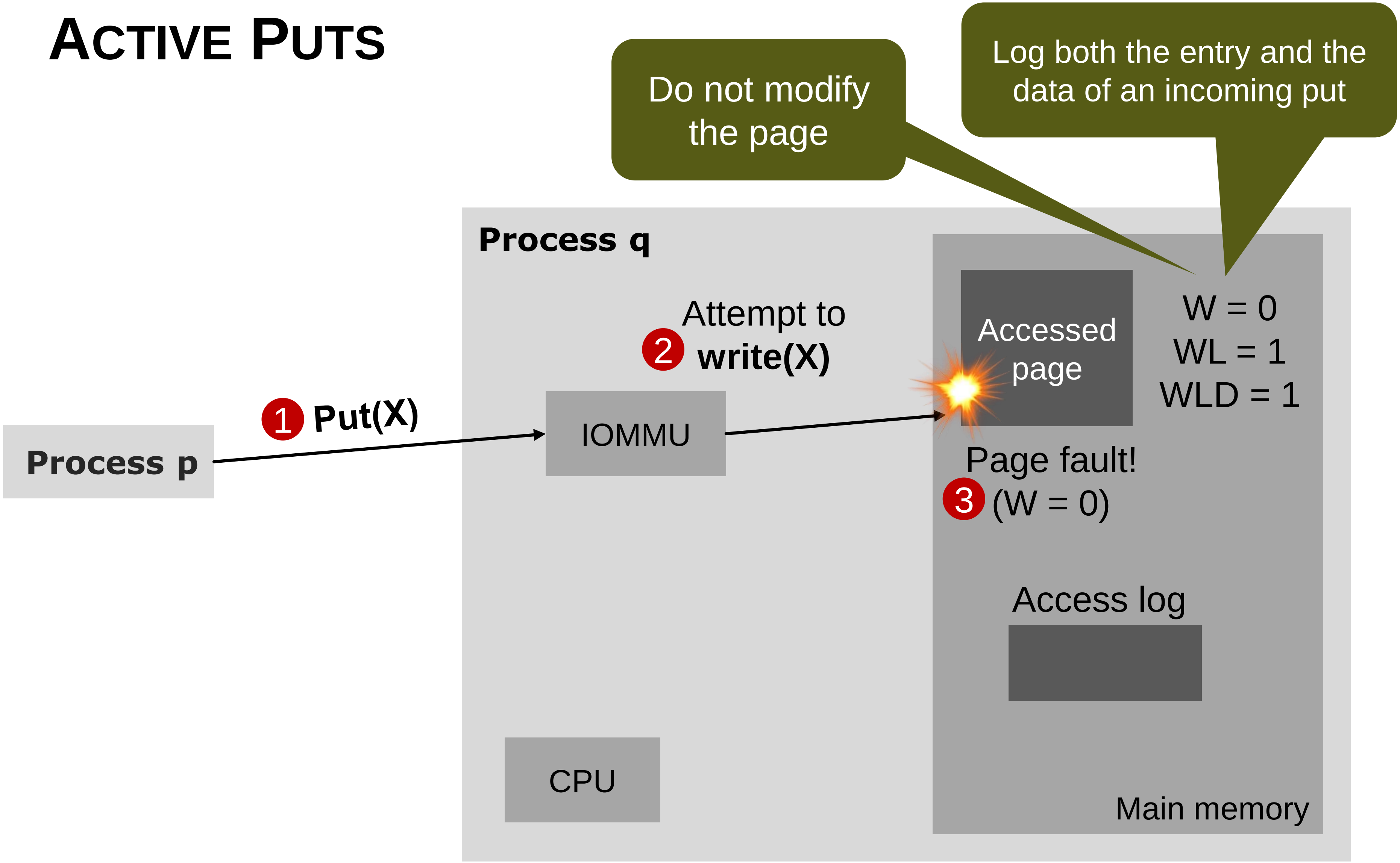
# Active Puts


Do not modify the page
Log both the entry and the data of an incoming put
Process q
Accessed page
W = 0
WL = 1
WLD = 1
1 Put(X)
Process p
IOMMU
Access log
CPU
Main memory

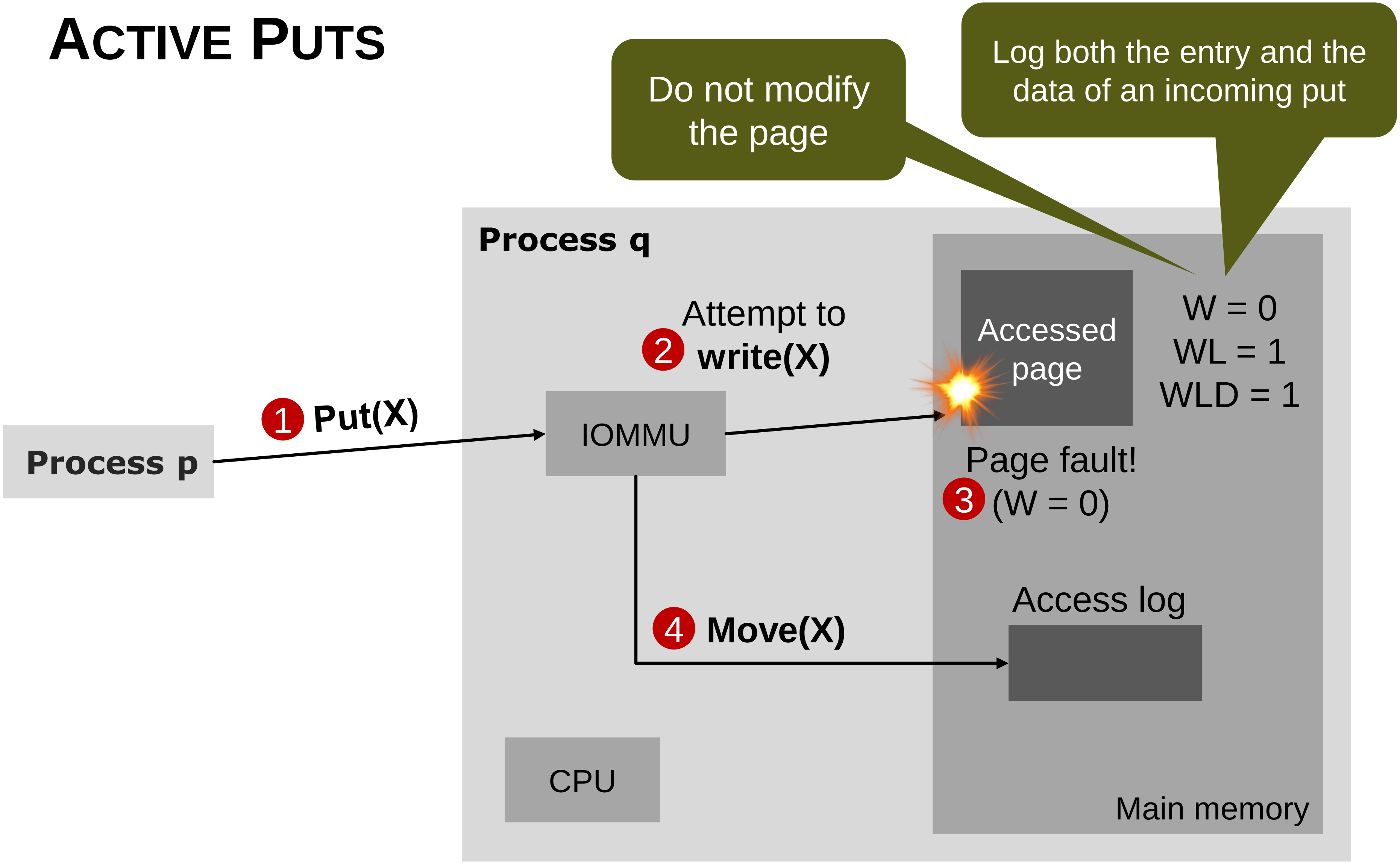
# Active Puts


Do not modify the page
Log both the entry and the data of an incoming put
Process q
Attempt to
2 write(X)
1 Put(X)
Process p
IOMMU
Accessed page
W = 0
WL = 1
WLD = 1
Access log
CPU
Main memory

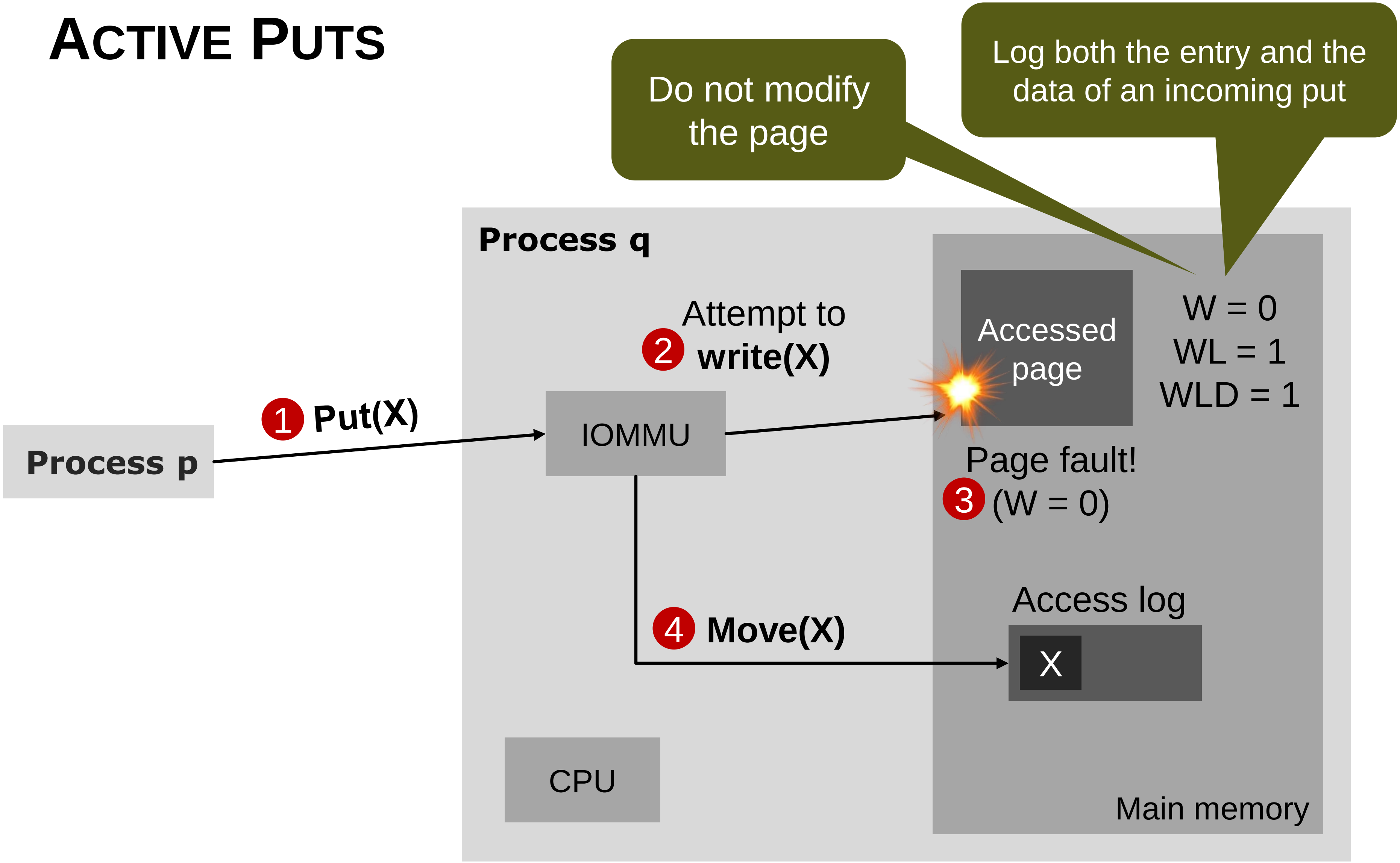
# Active Puts


Do not modify the page
Log both the entry and the data of an incoming put
Process q
Process p
1 Put(X)
IOMMU
Attempt to
2 write(X)
Accessed page
W = 0
WL = 1
WLD = 1
Page fault!
3 (W = 0)
Access log
CPU
Main memory

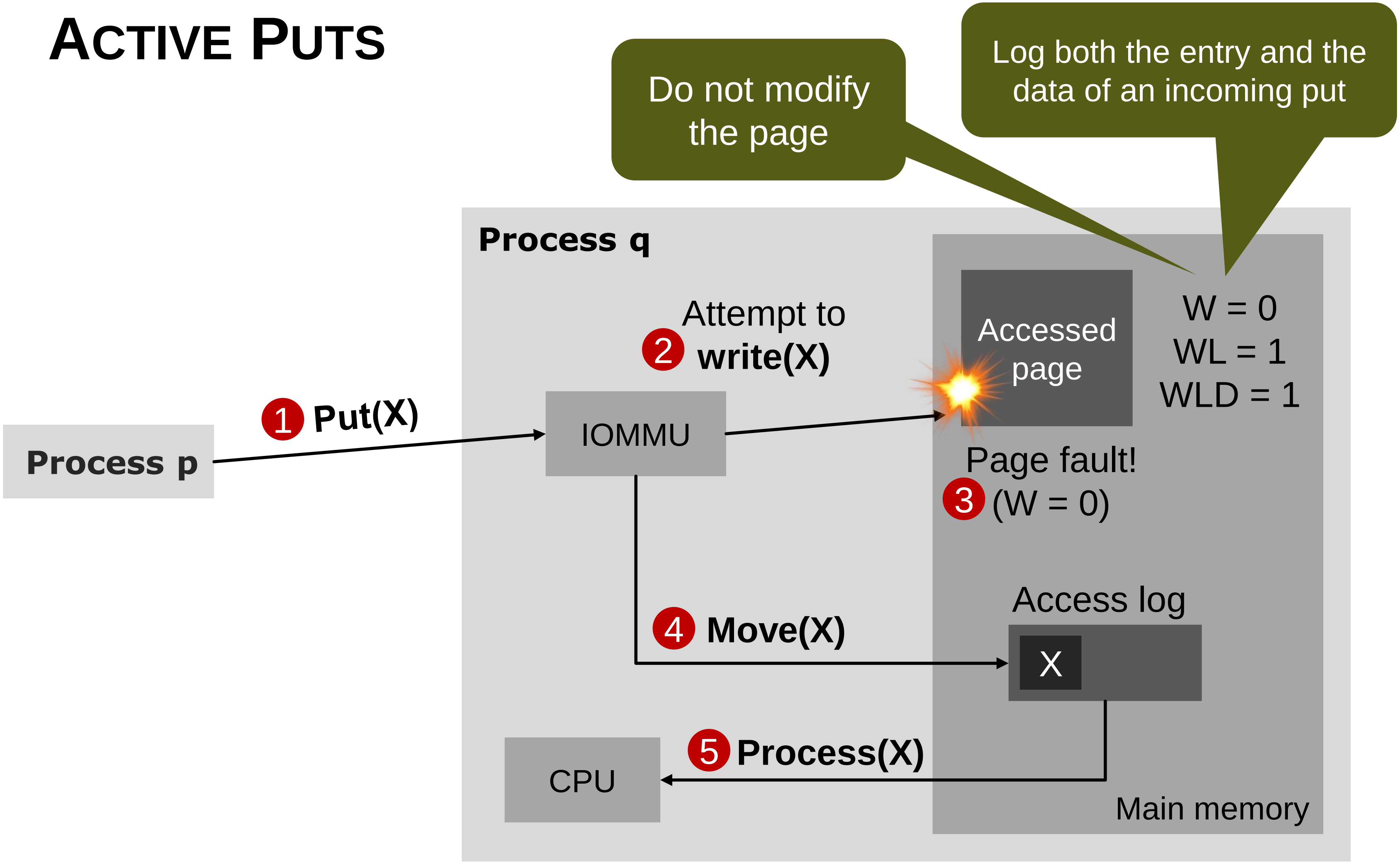
# Active Puts


Do not modify the page
Log both the entry and the data of an incoming put
Process q
Attempt to
2 write(X)
Accessed page
W = 0
WL = 1
WLD = 1
1 Put(X)
Process p
IOMMU
Page fault!
3 (W = 0)
Access log
4 Move(X)
CPU
Main memory

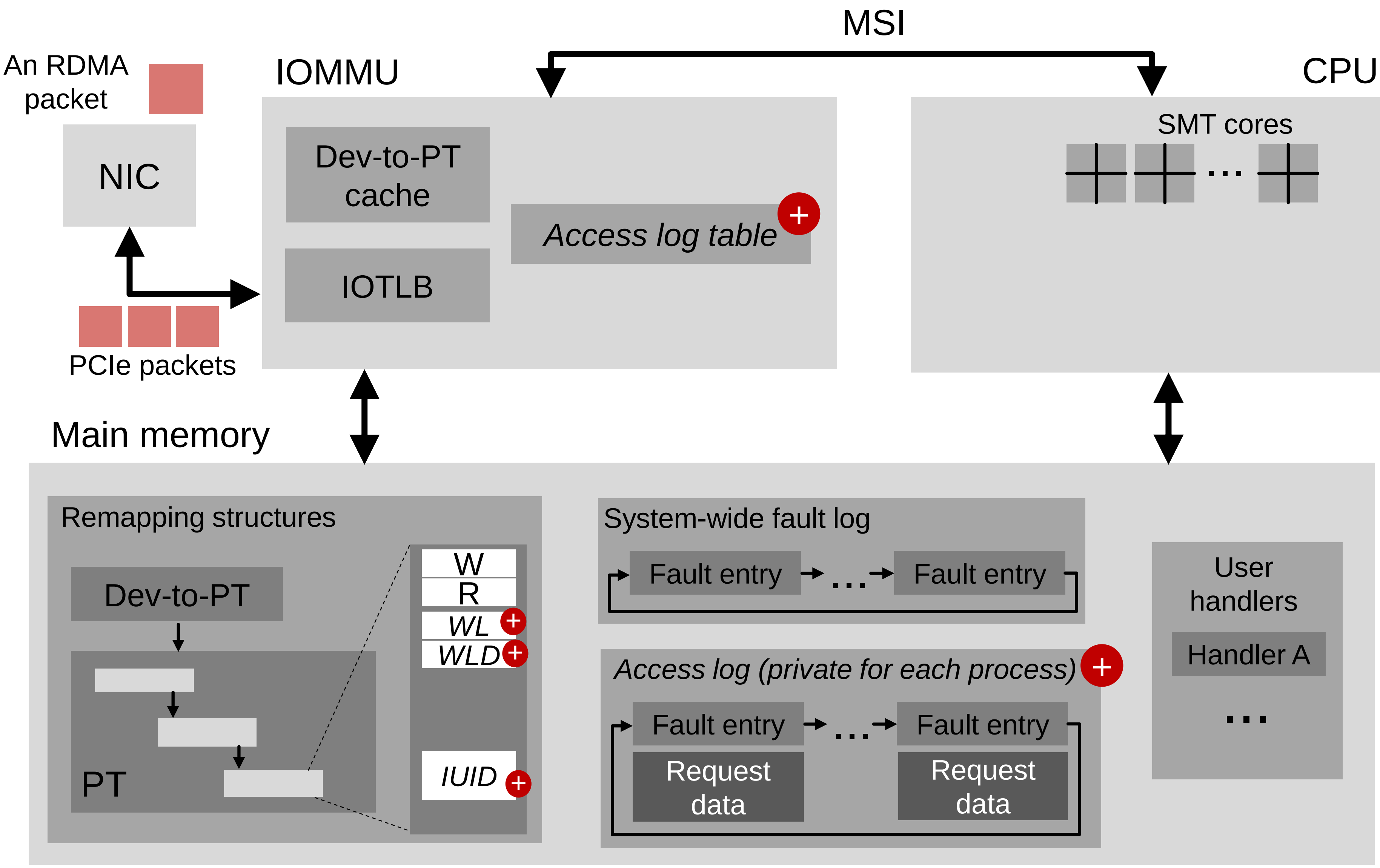
# Active Puts


Do not modify the page
Log both the entry and the data of an incoming put
Process q
Attempt to
2 write(X)
Accessed page
W = 0
WL = 1
WLD = 1
Process p
1 Put(X)
IOMMU
Page fault!
3 (W = 0)
Access log
4 Move(X)
X
CPU
Main memory

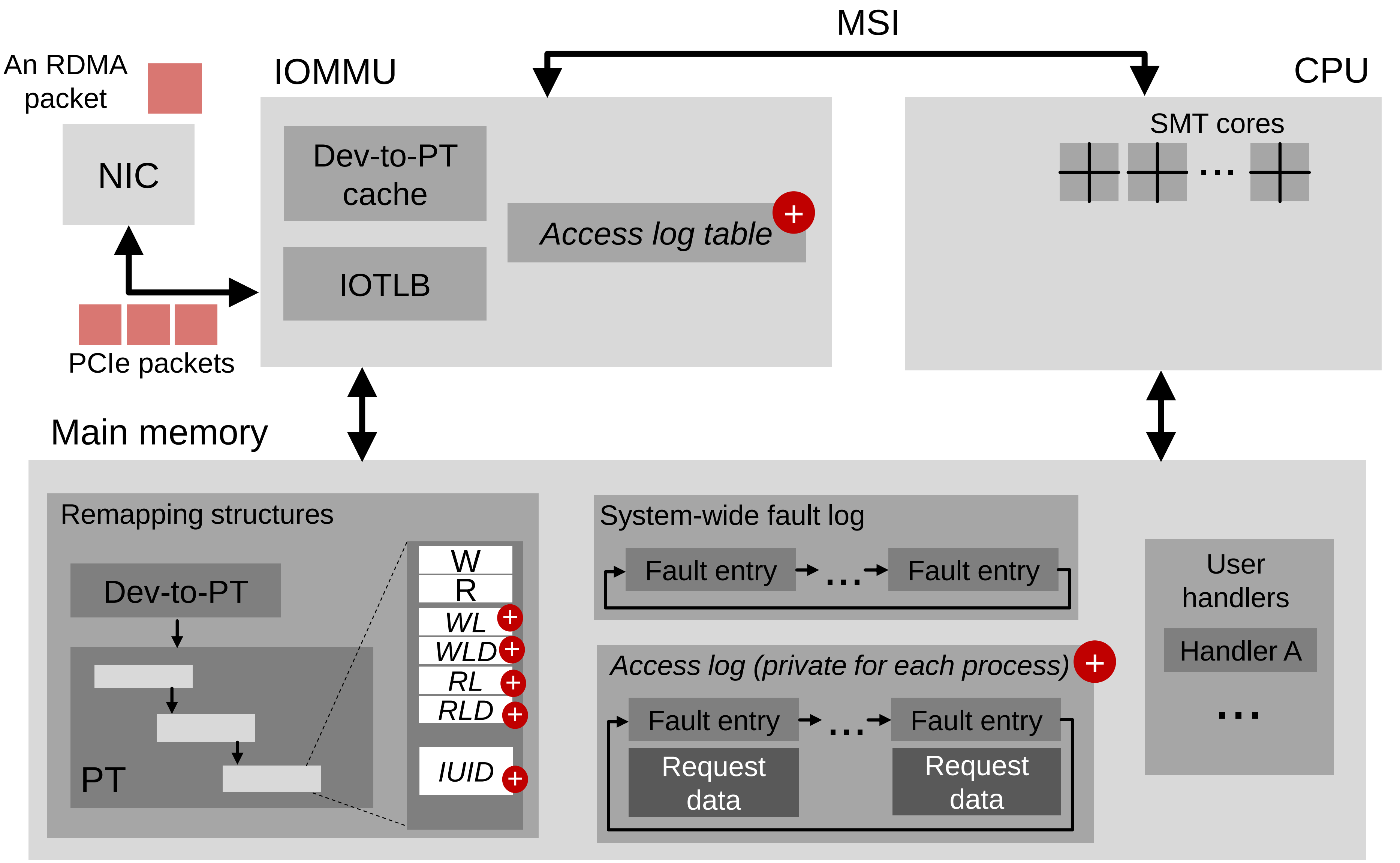
# Active Puts


Do not modify the page
Log both the entry and the data of an incoming put
Process q
Process p
1 Put(X)
IOMMU
Attempt to
2 write(X)
Accessed page
W = 0
WL = 1
WLD = 1
Page fault!
3 (W = 0)
4 Move(X)
Access log
X
CPU
5 Process(X)
Main memory

# Active Gets

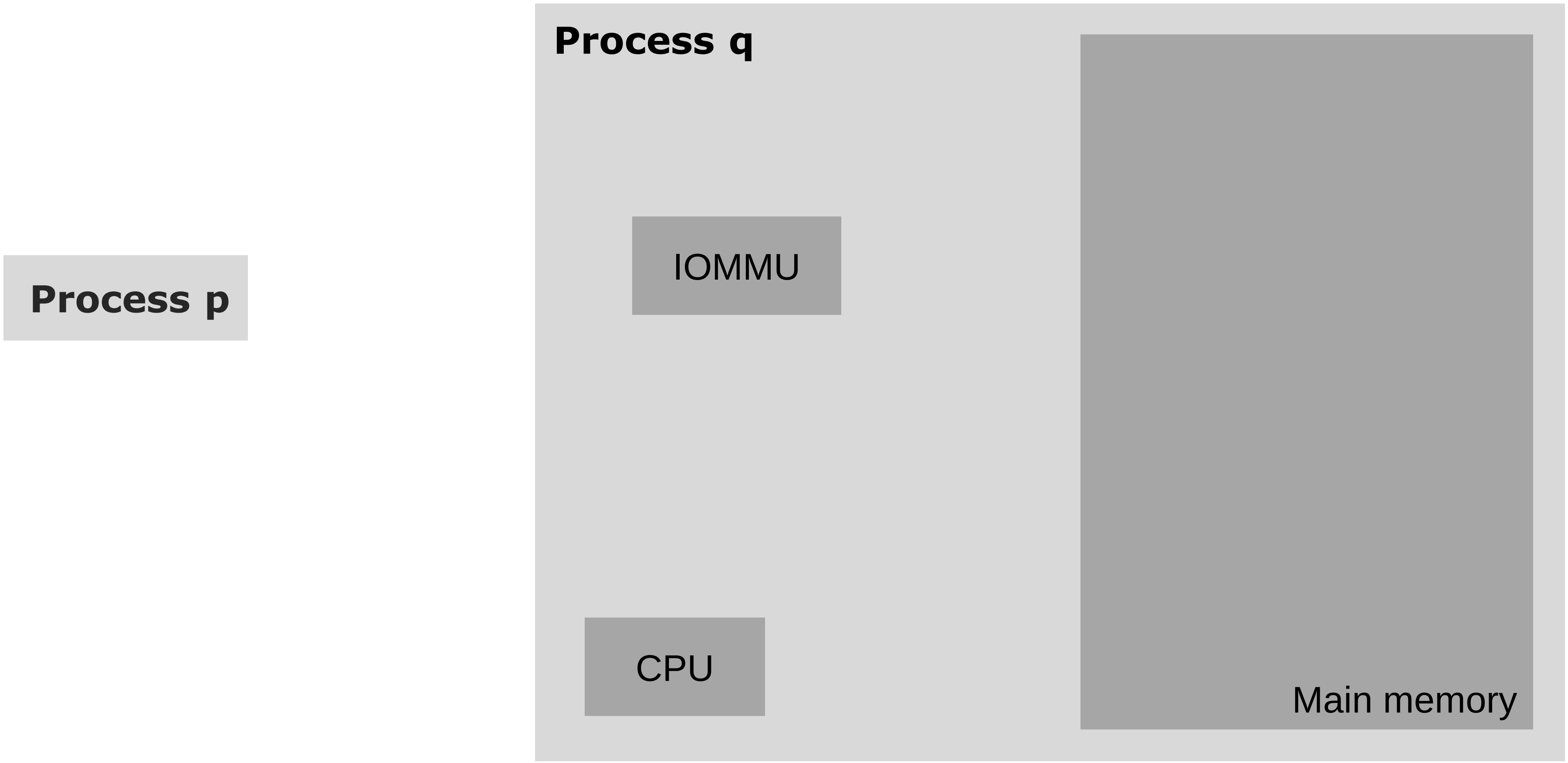

MSI
An RDMA packet
IOMMU
CPU
NIC
Dev-to-PT cache
IOTLB
Access log table
SMT cores
...
PCIe packets
Main memory
Remapping structures
Dev-to-PT
PT
W
R
WL
WLD
IUID
System-wide fault log
Fault entry
...
Fault entry
Access log (private for each process)
Fault entry
...
Fault entry
Request data
Request data
User handlers
Handler A
...

# Active Gets

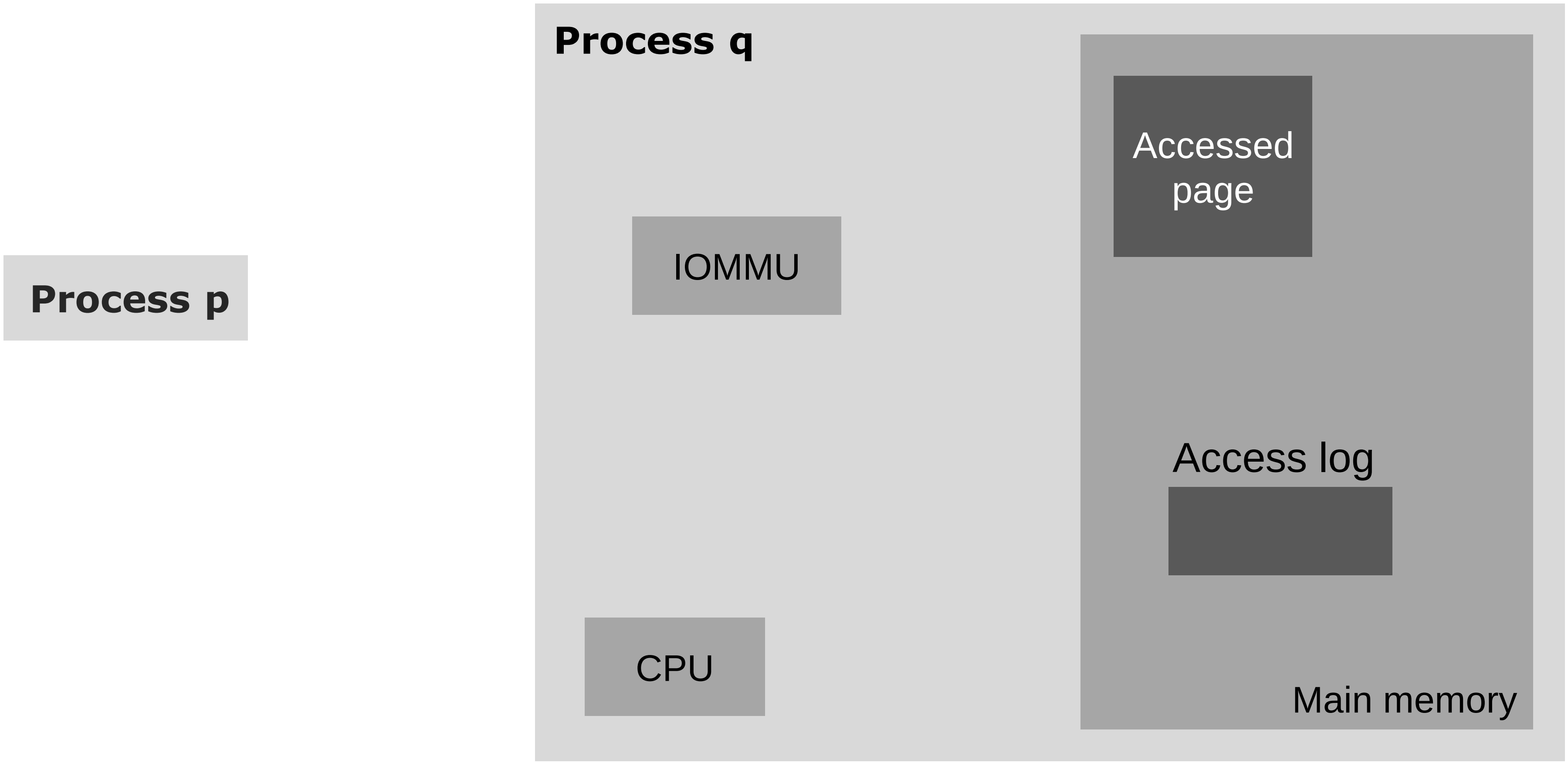

MSI
An RDMA packet
IOMMU
CPU
NIC
Dev-to-PT cache
IOTLB
Access log table
SMT cores
PCIe packets
Main memory
Remapping structures
Dev-to-PT
PT
W
R
WL
WLD
RL
RLD
IUID
System-wide fault log
Fault entry
Fault entry
Access log (private for each process)
Fault entry
Fault entry
Request data
Request data
User handlers
Handler A

# Active Gets

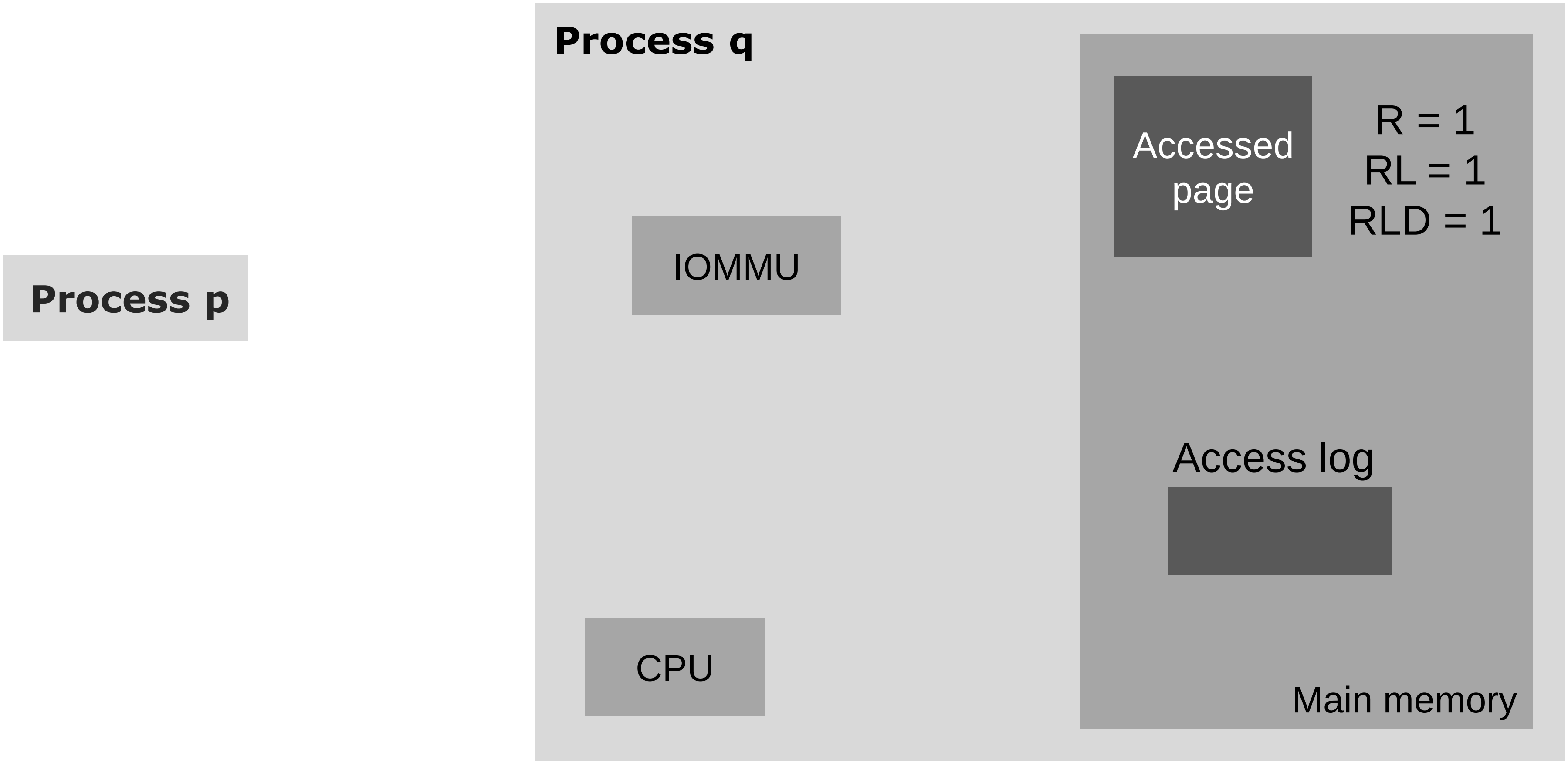
# ACTIVE GETS



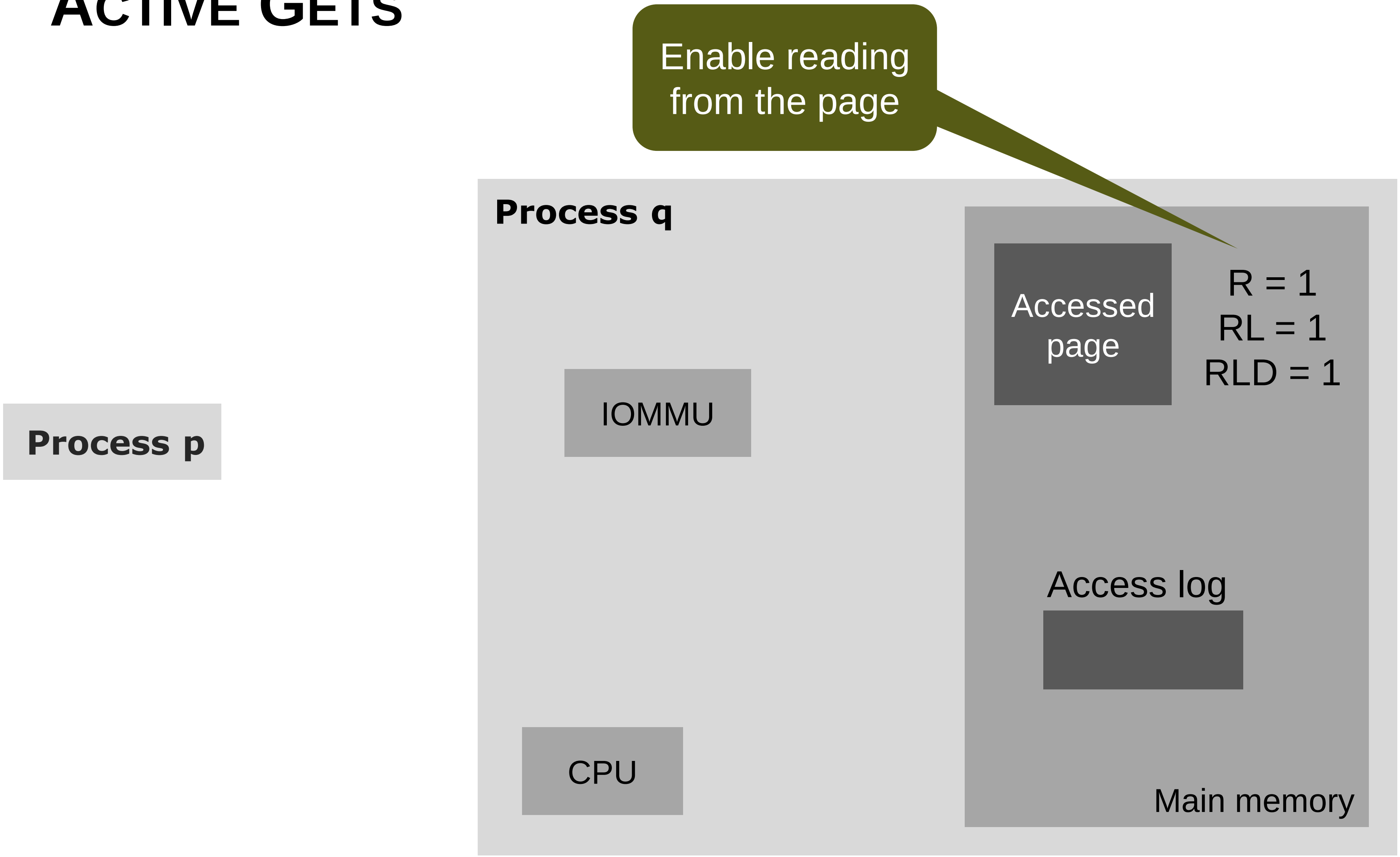
# ACTIVE GETS


Process p
Process q
IOMMU
CPU
Accessed page
Access log
Main memory

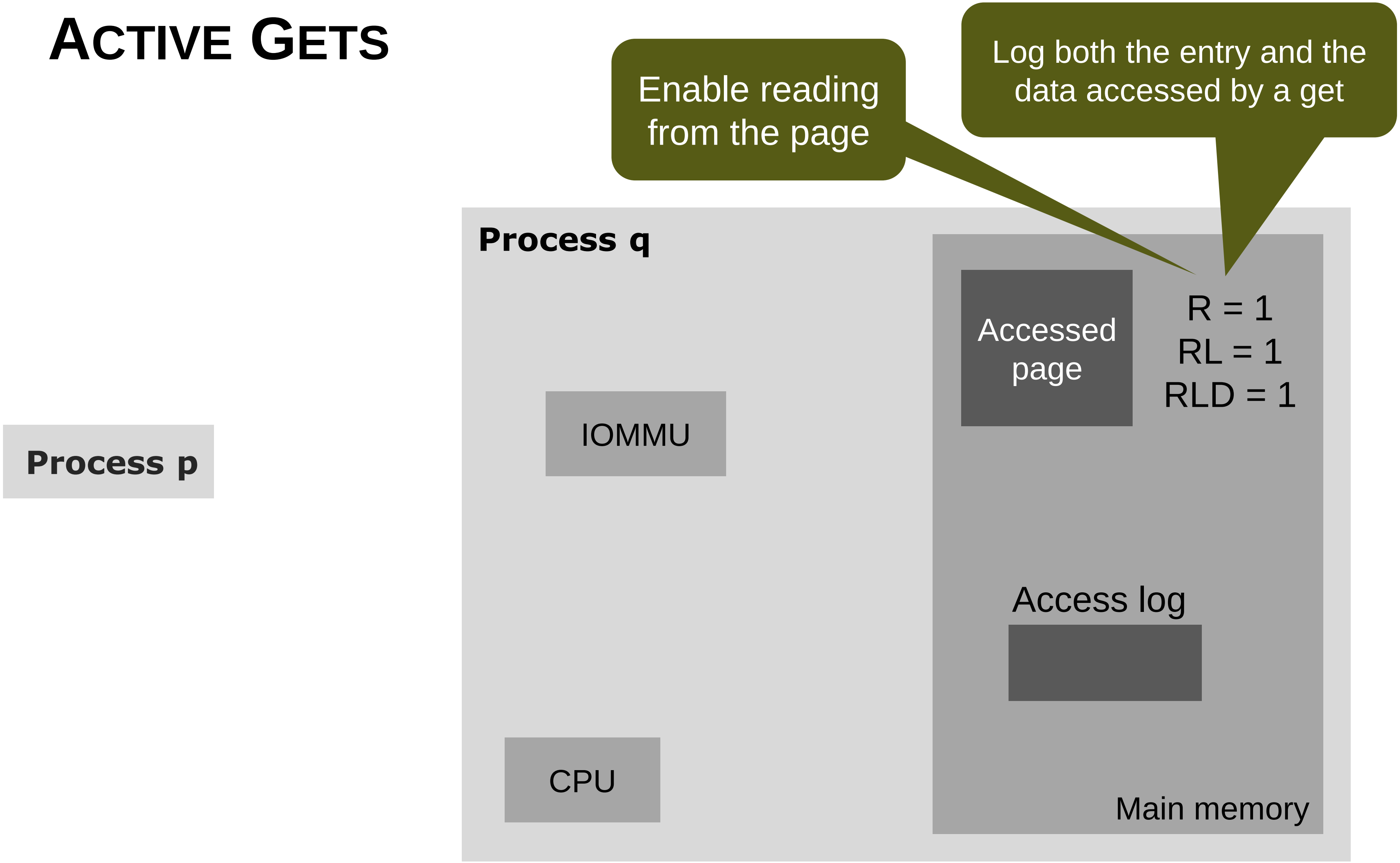
# ACTIVE GETS


Process p
Process q
Accessed page
R = 1
RL = 1
RLD = 1
IOMMU
Access log
CPU
Main memory

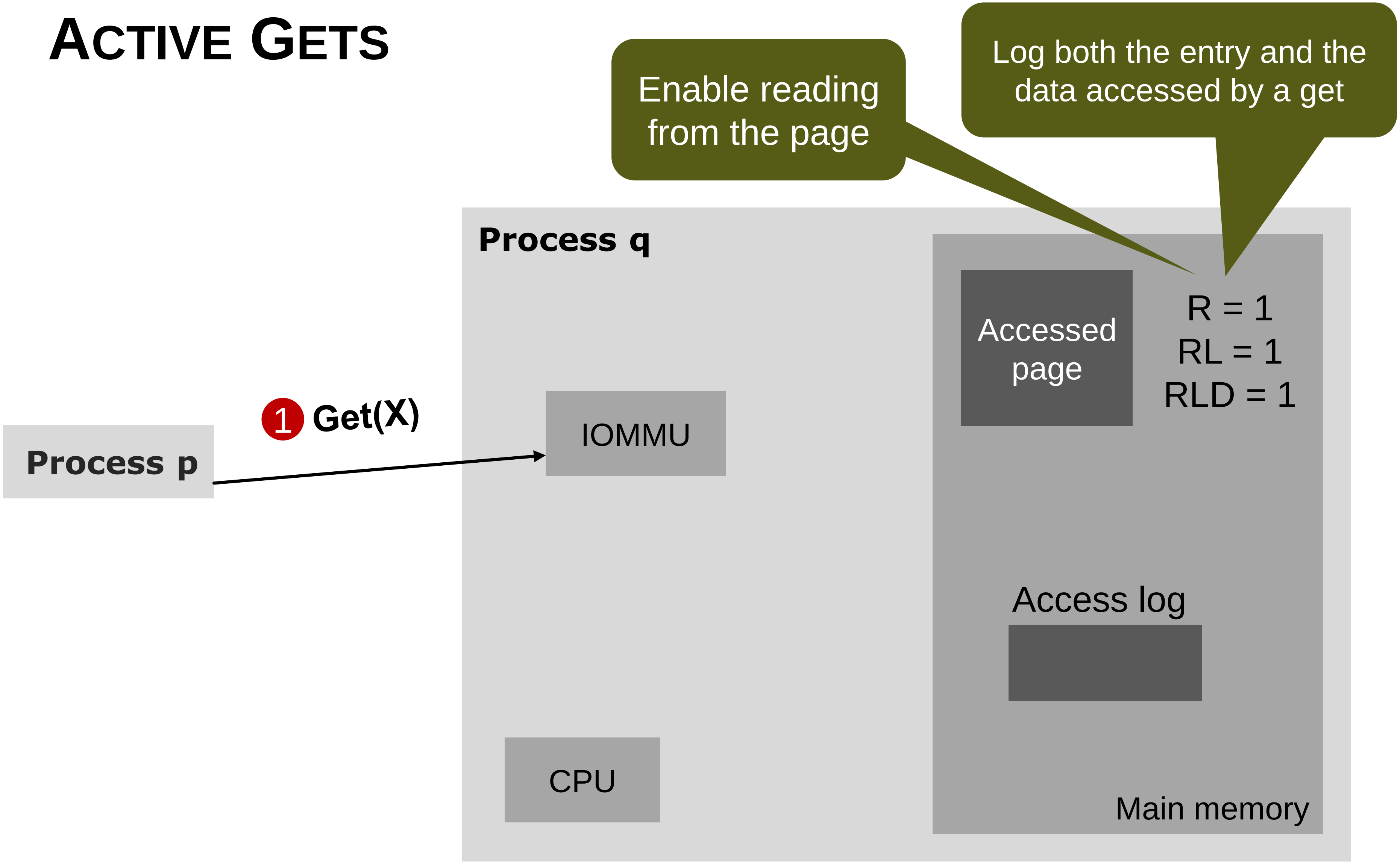
# Active Gets


Enable reading
from the page
Process q
Accessed
page
R = 1
RL = 1
RLD = 1
IOMMU
Process p
Access log
CPU
Main memory

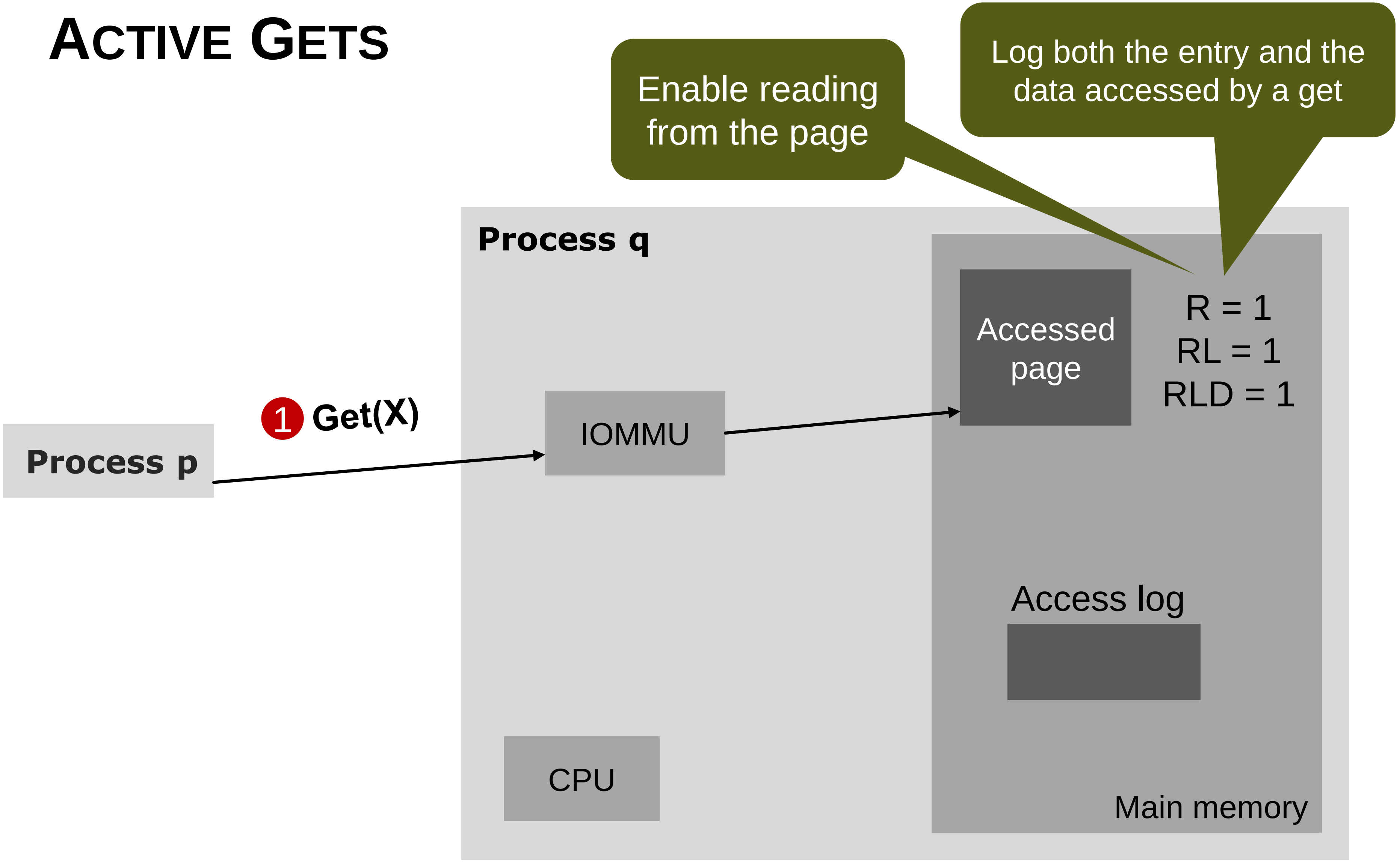
# ACTIVE GETS


Enable reading from the page
Log both the entry and the data accessed by a get
Process q
Process p
Accessed page
R = 1
RL = 1
RLD = 1
IOMMU
Access log
CPU
Main memory

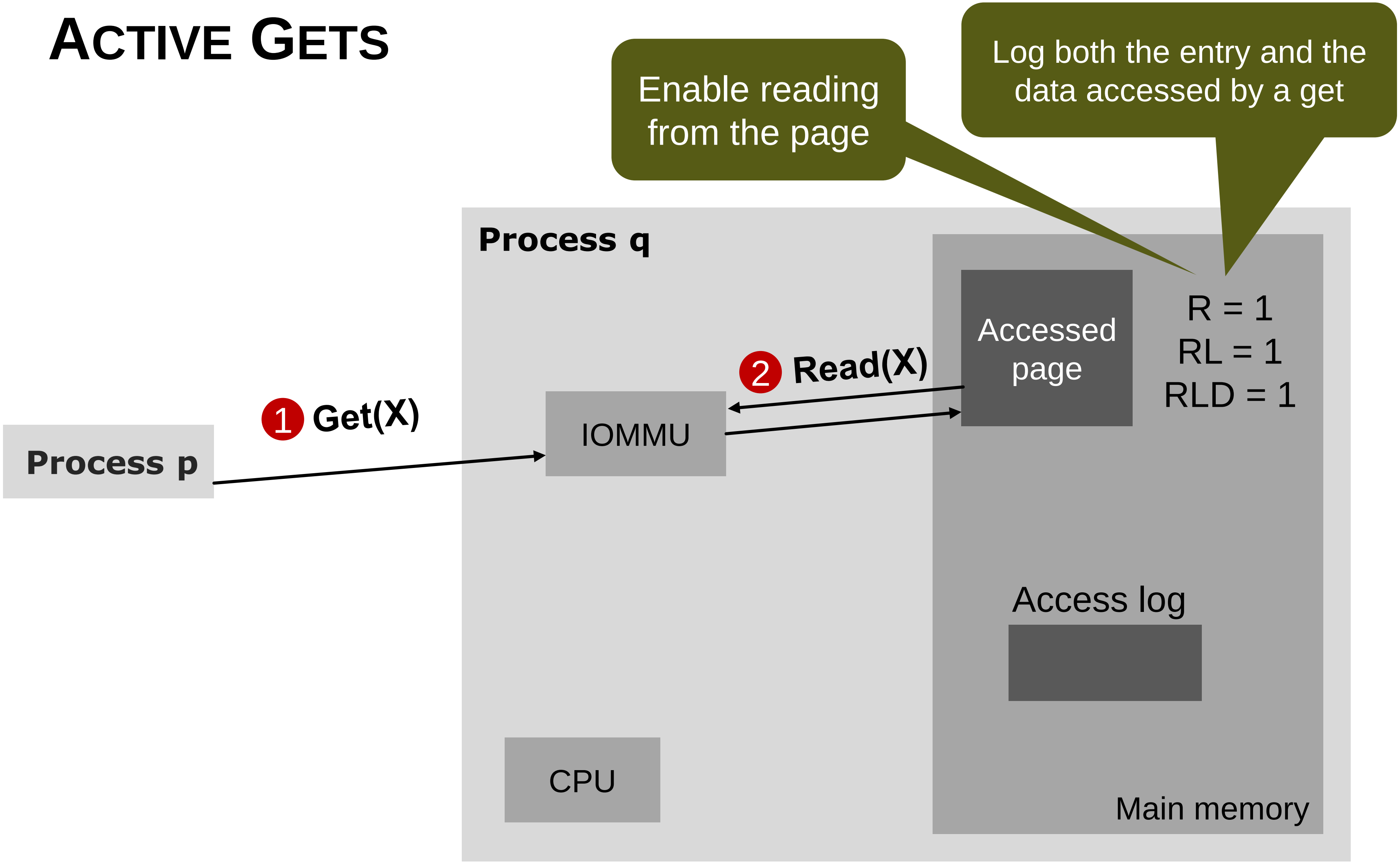
# ACTIVE GETS


Enable reading from the page
Log both the entry and the data accessed by a get
Process q
Accessed page
R = 1
RL = 1
RLD = 1
1 Get(X)
Process p
IOMMU
Access log
CPU
Main memory

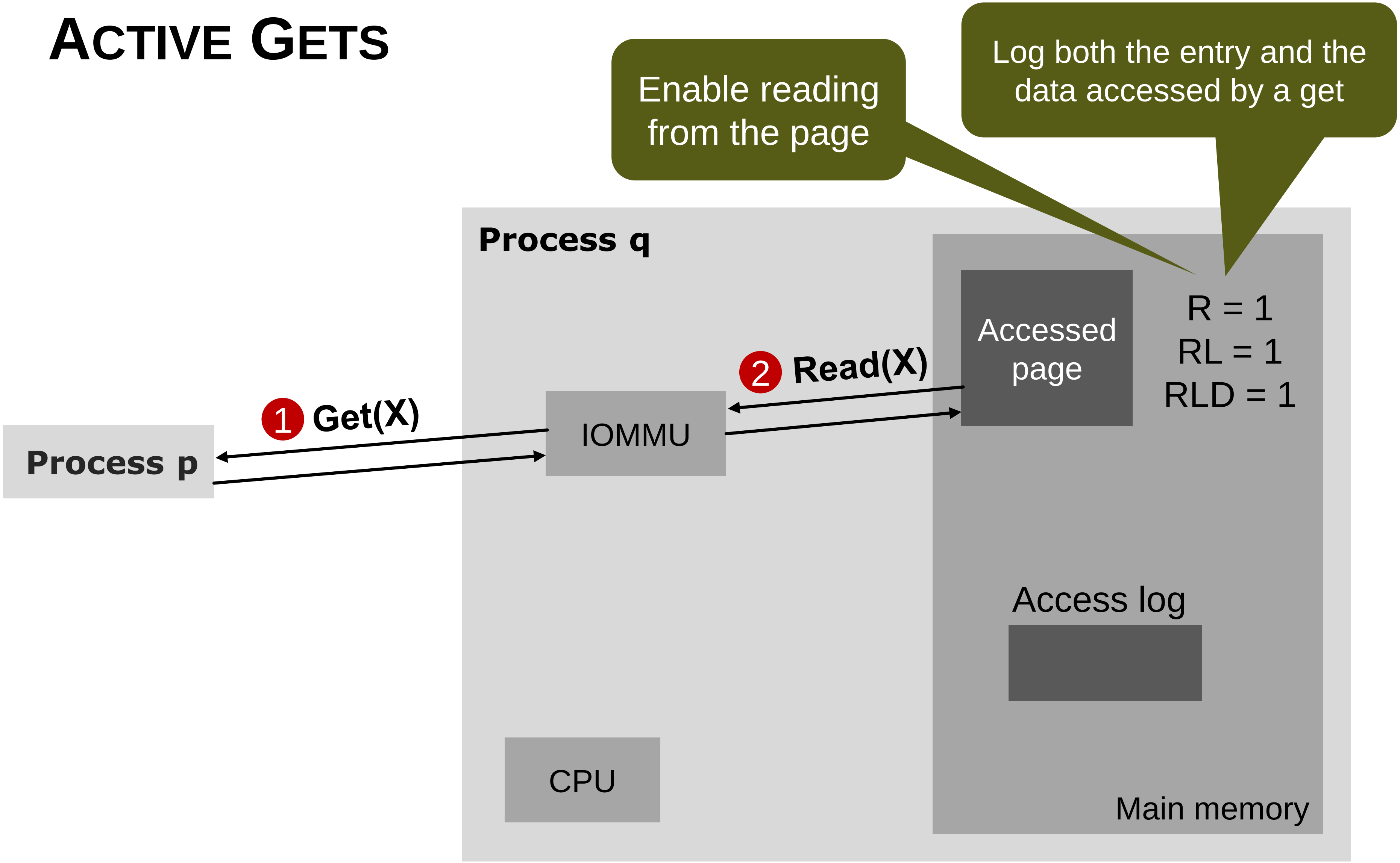
# ACTIVE GETS


Enable reading from the page
Log both the entry and the data accessed by a get
Process q
Accessed page
R = 1
RL = 1
RLD = 1
1 Get(X)
IOMMU
Process p
Access log
CPU
Main memory

# ACTIVE GETS

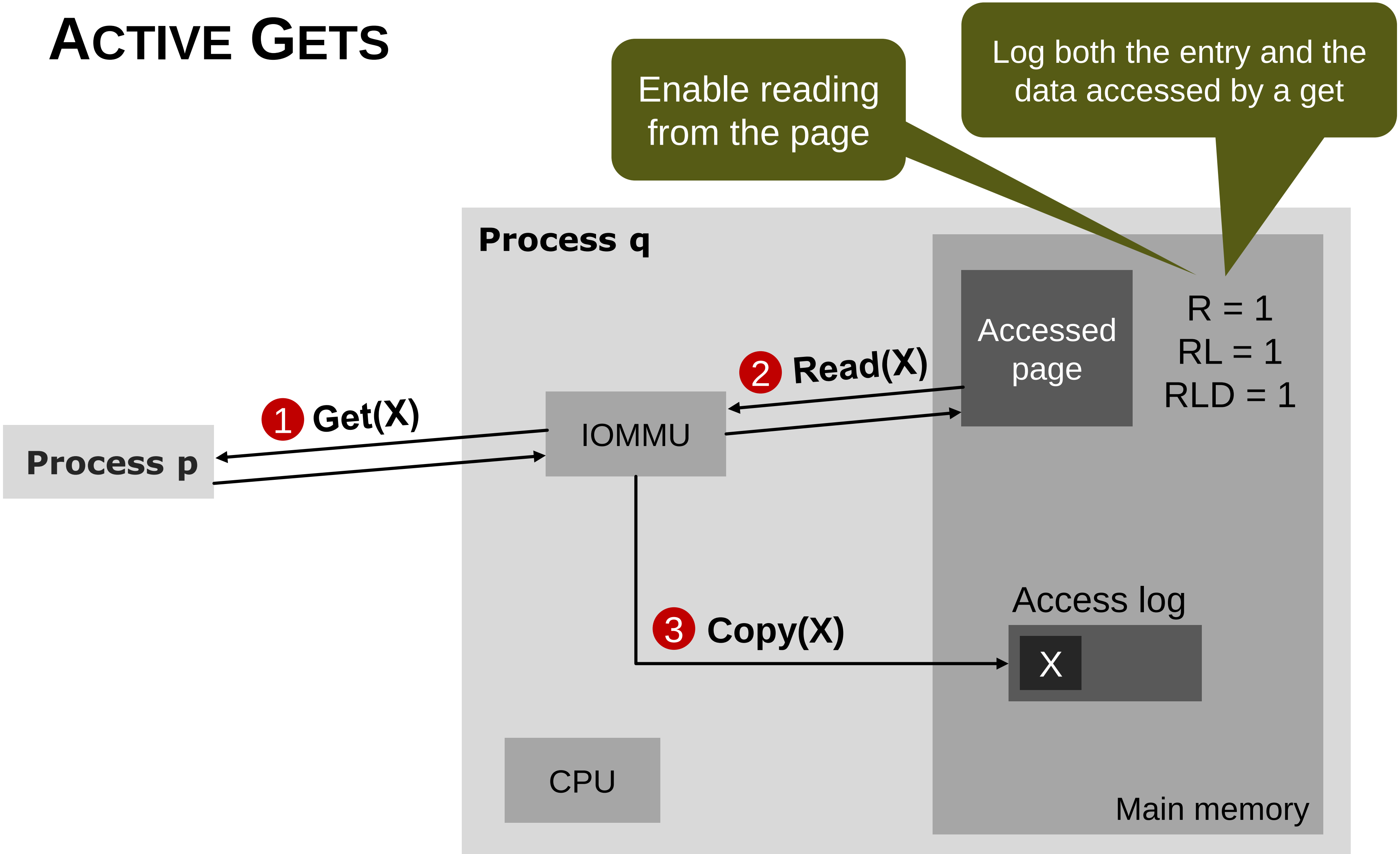

Enable reading from the page
Log both the entry and the data accessed by a get
Process q
Accessed page
R = 1
RL = 1
RLD = 1
2 Read(X)
1 Get(X)
IOMMU
Process p
Access log
CPU
Main memory

# Active Gets

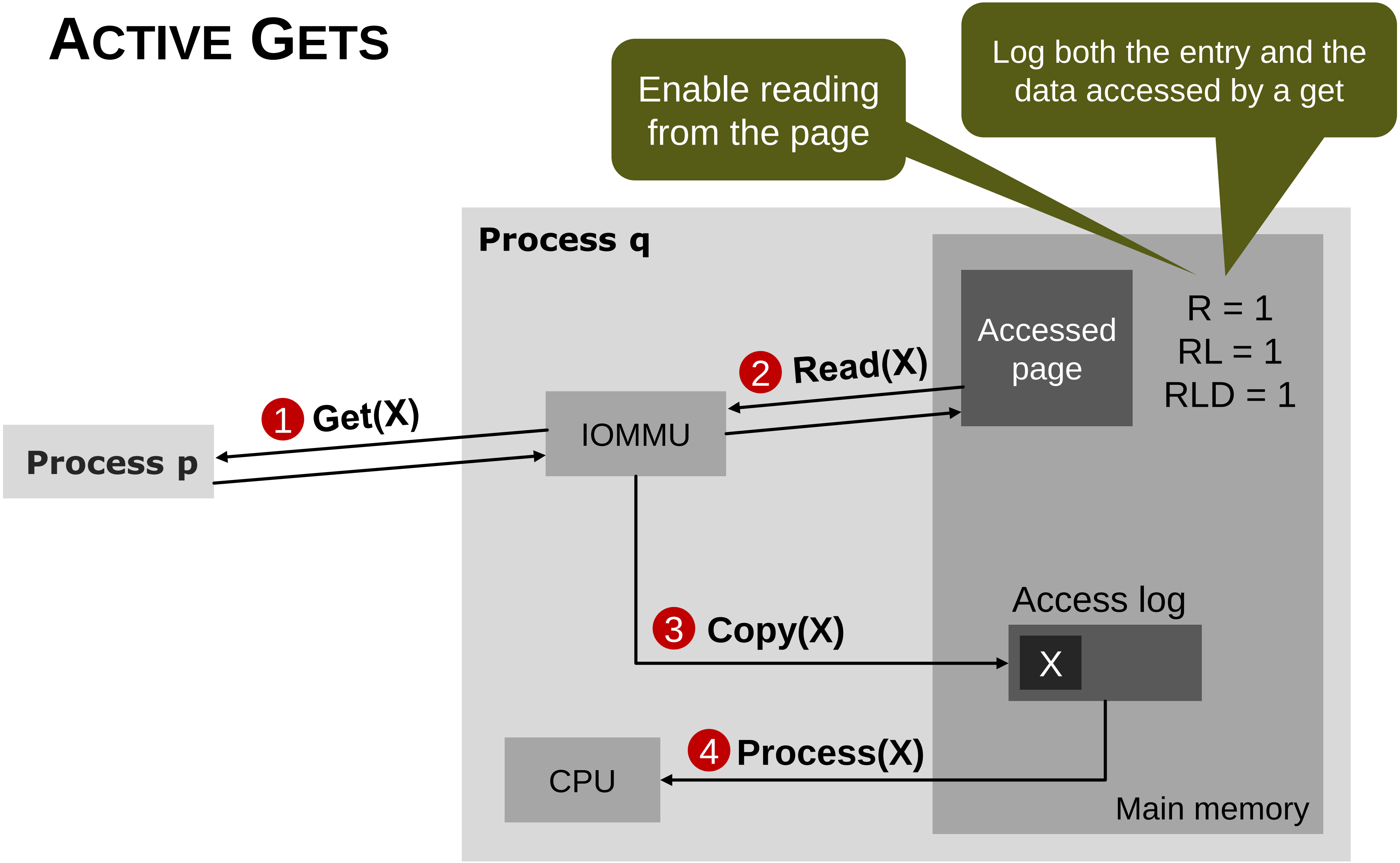


Enable reading from the page
Log both the entry and the data accessed by a get
Process q
Accessed page
R = 1
RL = 1
RLD = 1
2 Read(X)
1 Get(X)
Process p
IOMMU
Access log
CPU
Main memory

# ACTIVE GETS


Enable reading from the page
Log both the entry and the data accessed by a get
Process q
Accessed page
R = 1
RL = 1
RLD = 1
2 Read(X)
1 Get(X)
Process p
IOMMU
3 Copy(X)
Access log
X
CPU
Main memory

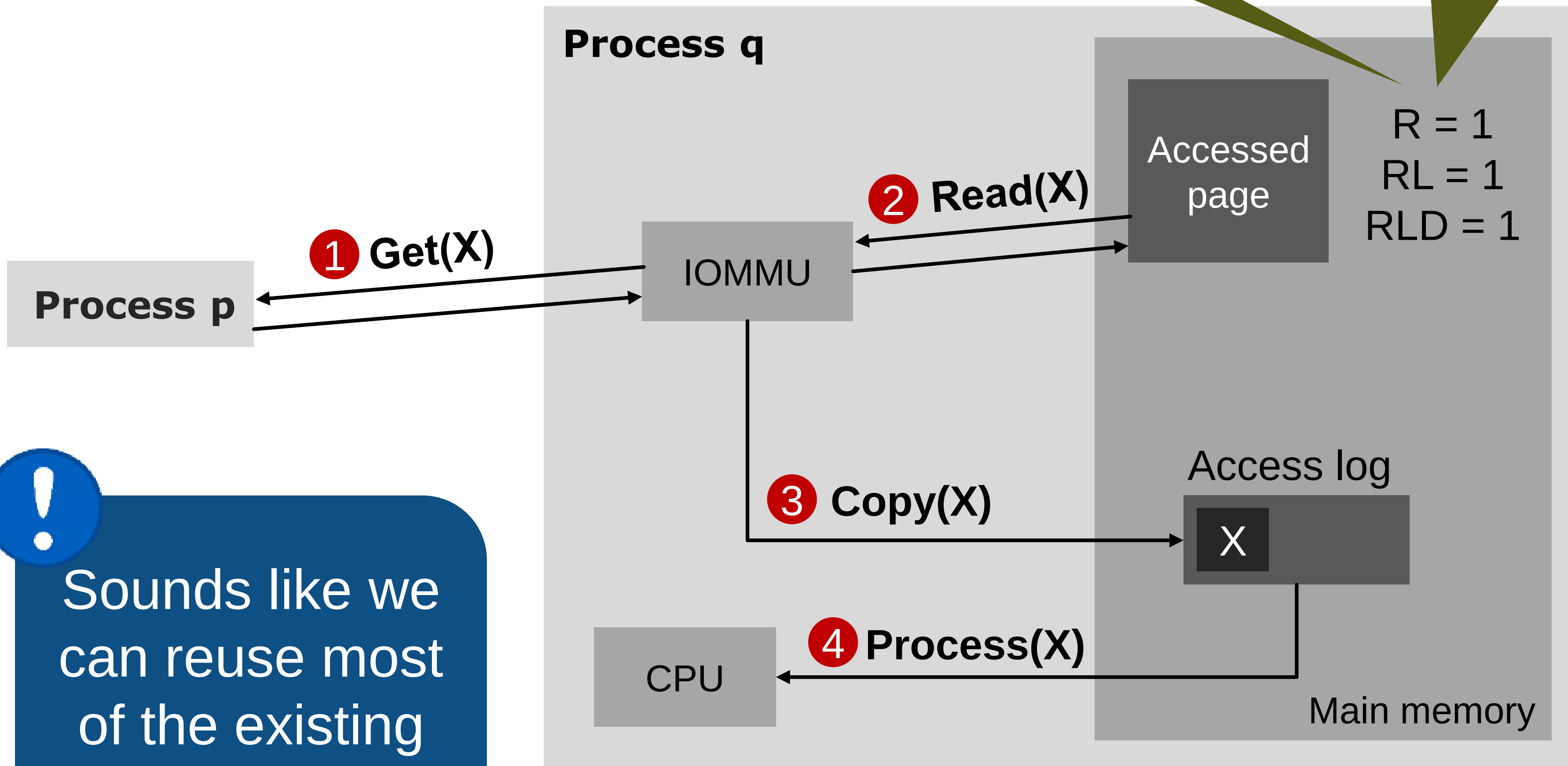
# Active Gets


Enable reading from the page
Log both the entry and the data accessed by a get
Process q
Accessed page
R = 1
RL = 1
RLD = 1
2 Read(X)
1 Get(X)
Process p
IOMMU
Access log
X
3 Copy(X)
4 Process(X)
CPU
Main memory

# ACTIVE GETS

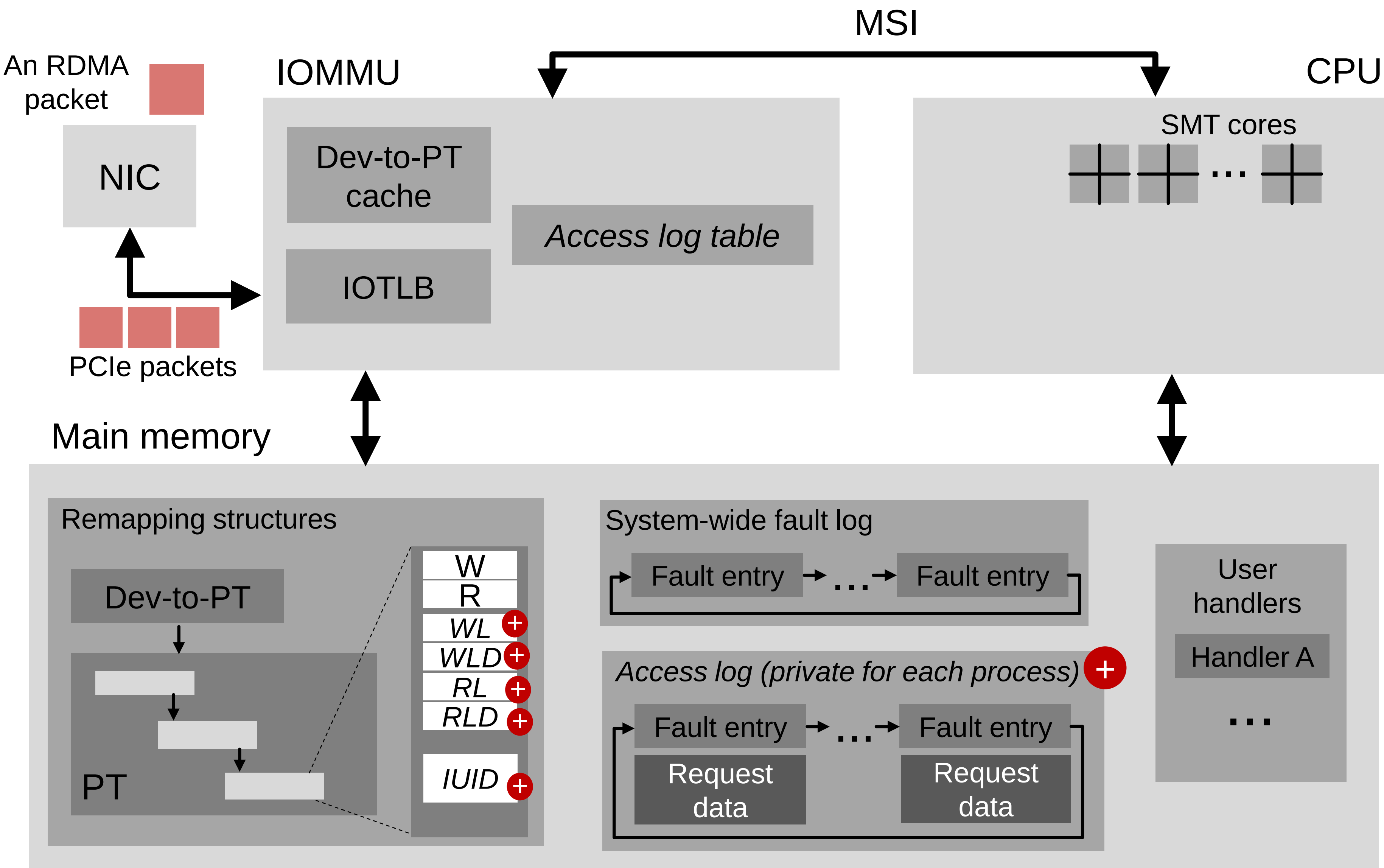
Enable reading from the page

Log both the entry and the data accessed by a get

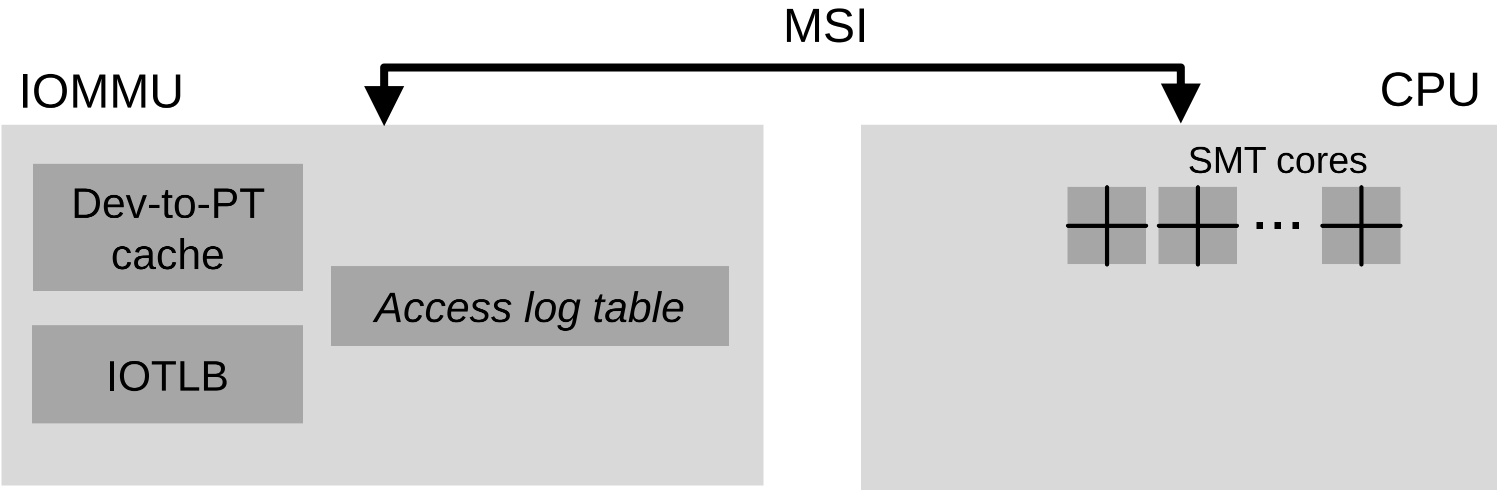



Sounds like we can reuse most of the existing stuff!

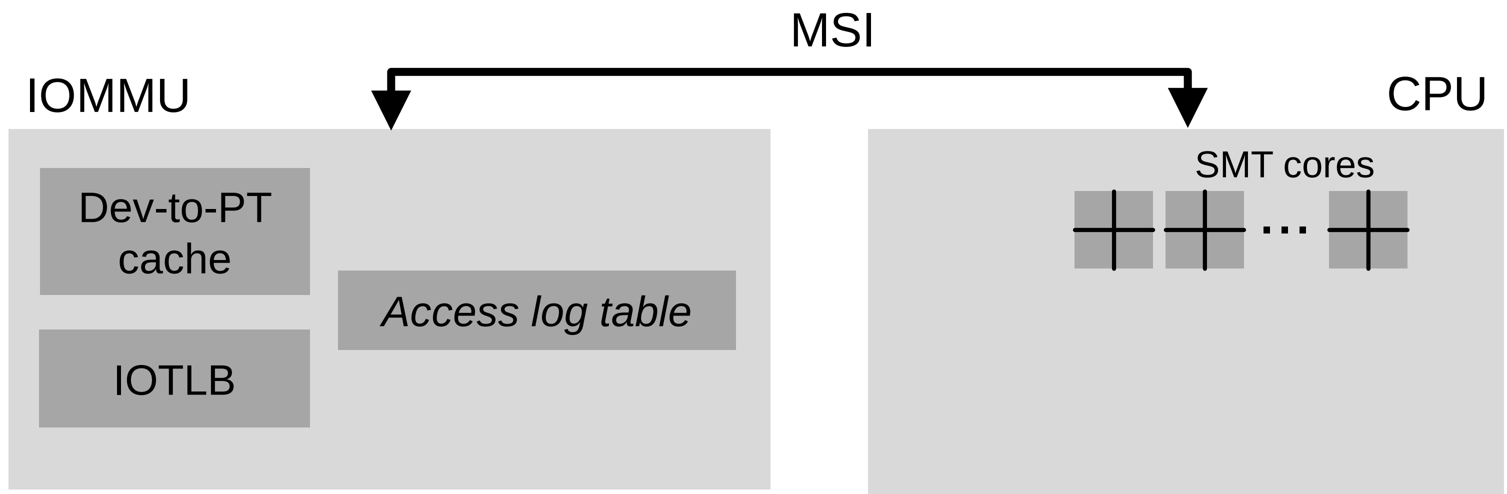
# Interactions with the CPU



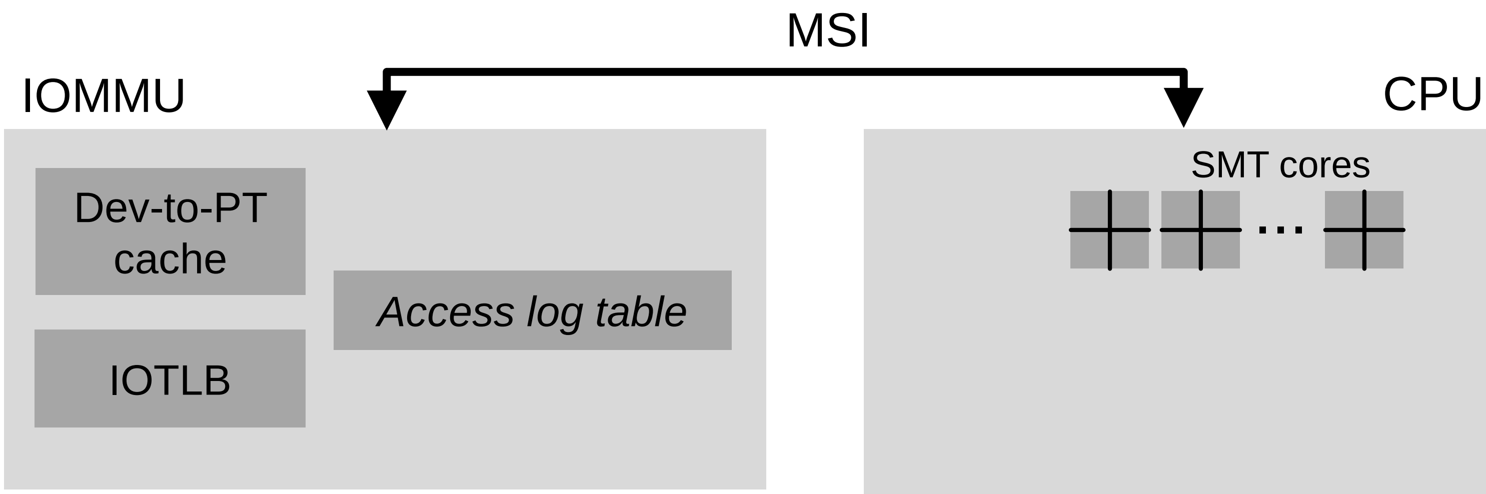
# INTERACTIONS WITH THE CPU



# INTERACTIONS WITH THE CPU

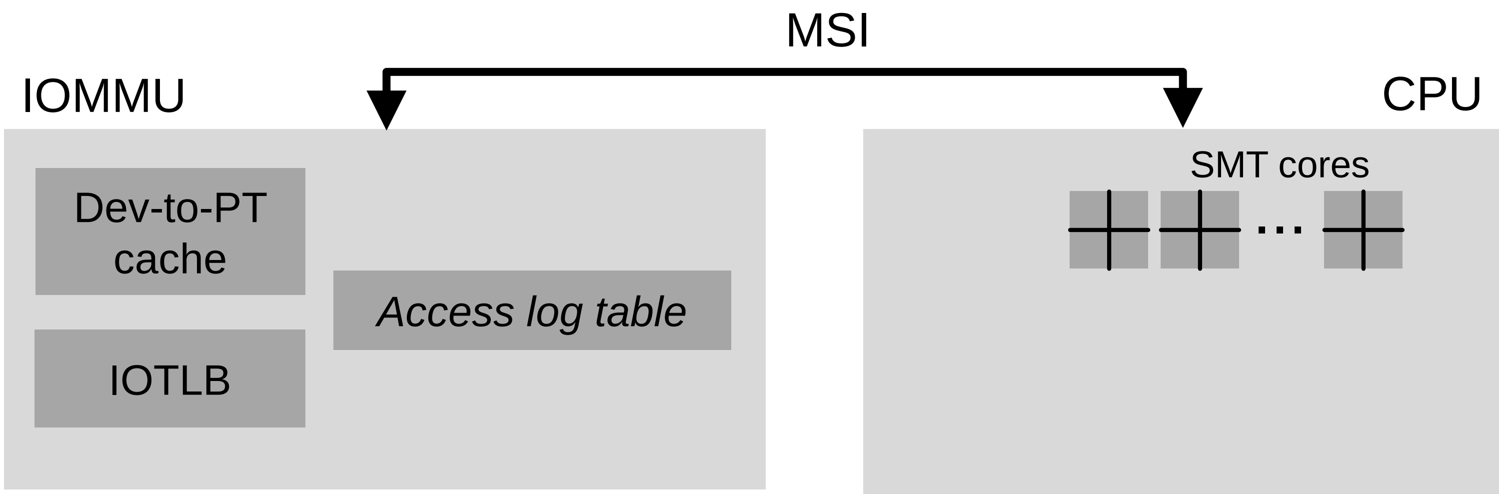


# INTERACTIONS WITH THE CPU



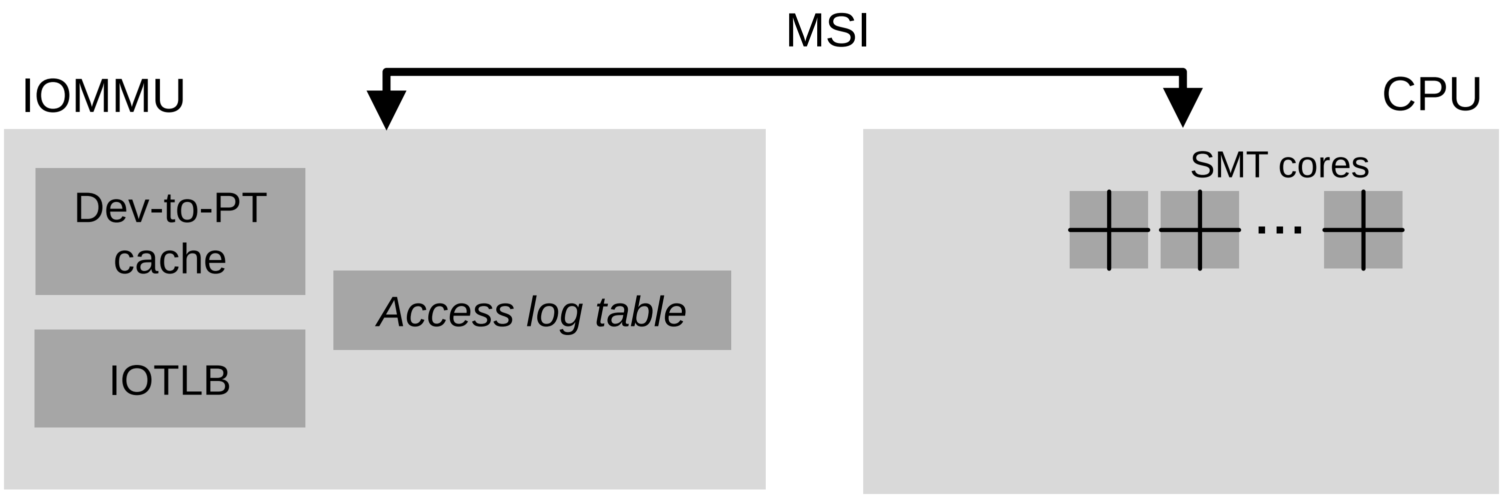

- Interrupts

# INTERACTIONS WITH THE CPU



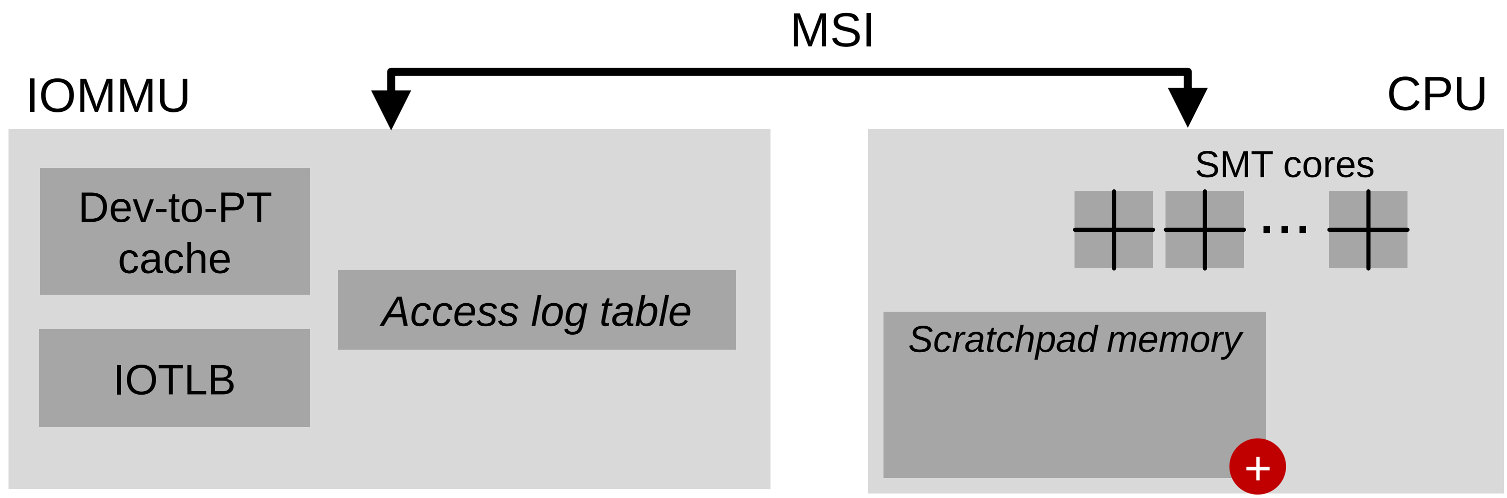

- Interrupts
- Polling

# INTERACTIONS WITH THE CPU



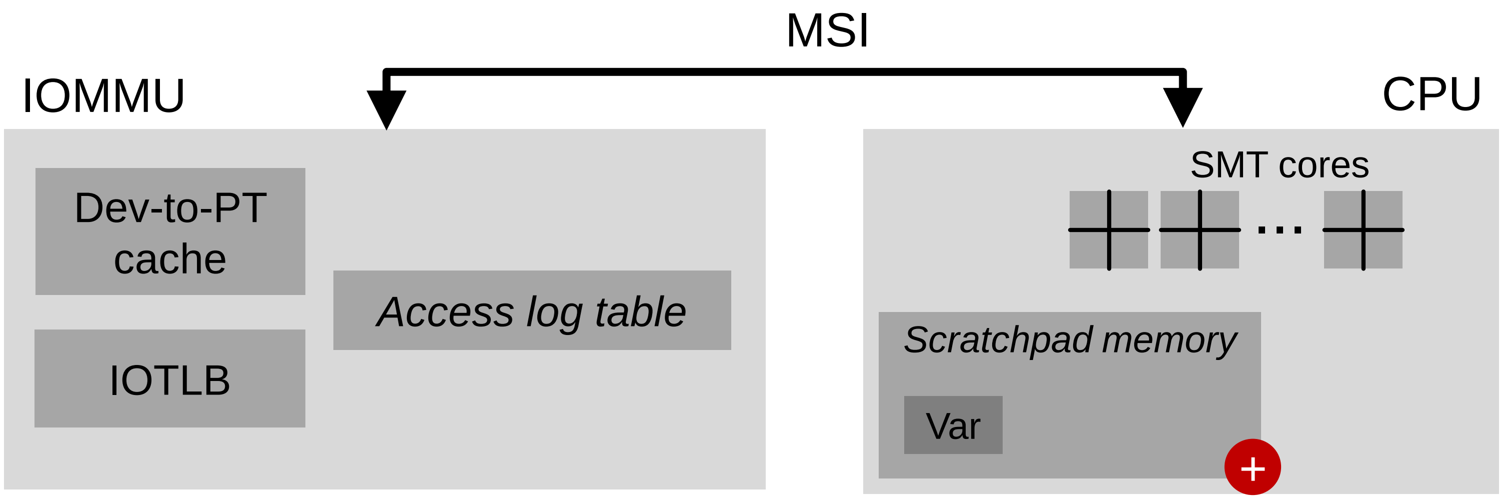

- Interrupts
- Polling
- Direct notifications via scratchpads

# INTERACTIONS WITH THE CPU



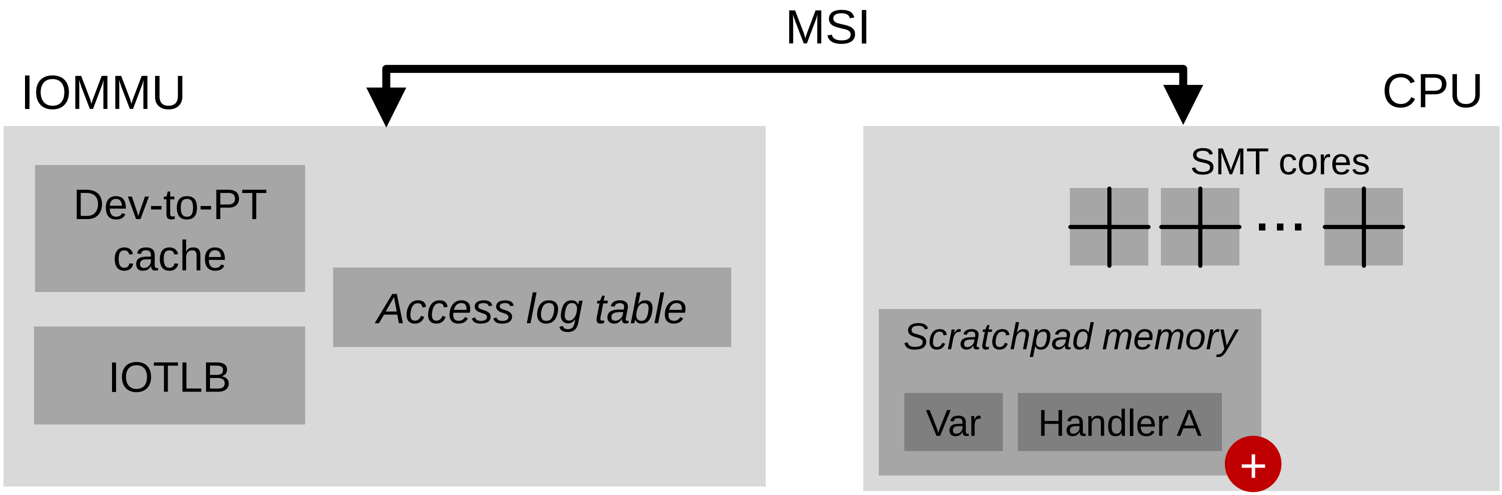

- Interrupts
- Polling
- Direct notifications via scratchpads

# INTERACTIONS WITH THE CPU



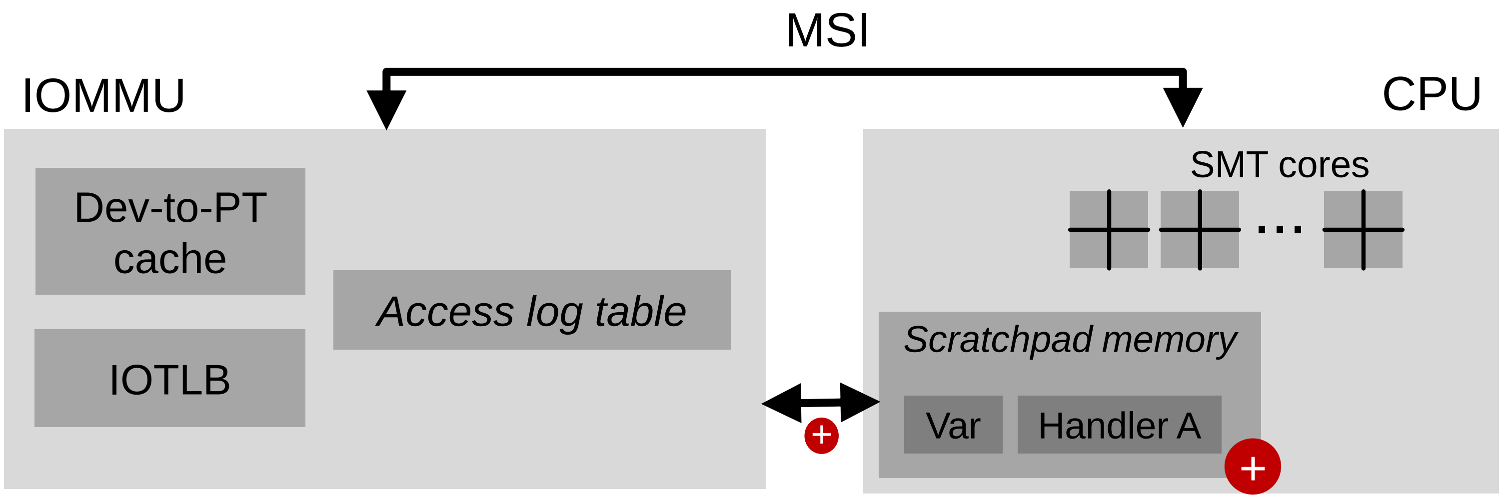

- Interrupts
- Polling
- Direct notifications via scratchpads

# INTERACTIONS WITH THE CPU




- Interrupts
- Polling
- Direct notifications via scratchpads

# INTERACTIONS WITH THE CPU



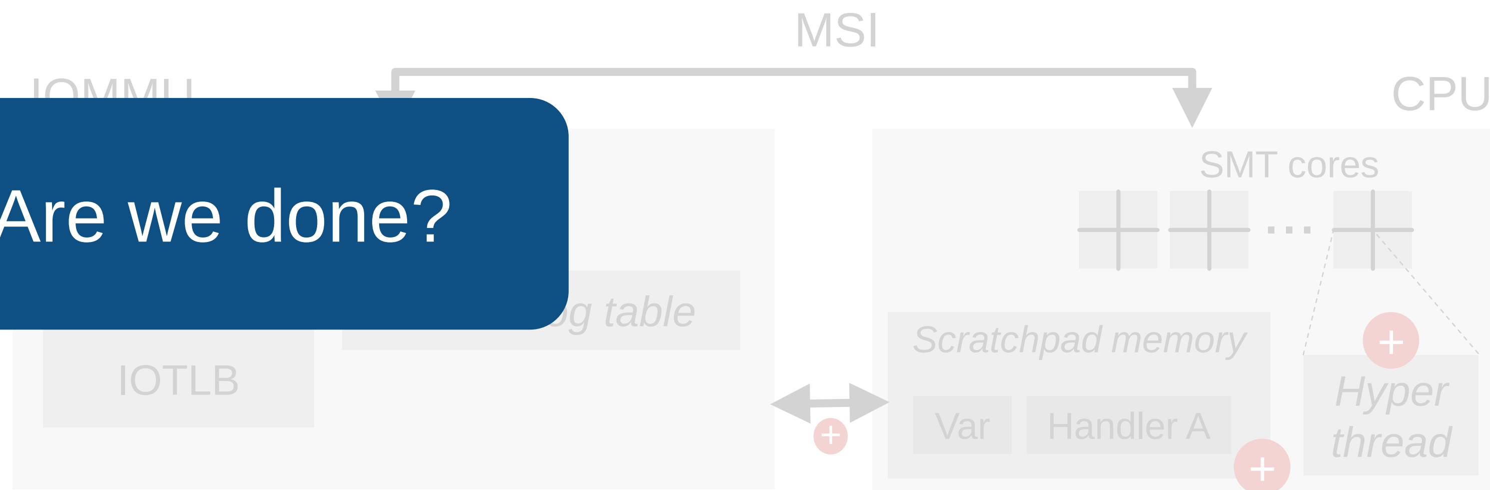

- Interrupts
- Polling
- Direct notifications via scratchpads

# Interactions with the CPU




- Interrupts
- Polling
- Direct notifications via scratchpads

# Interactions with the CPU




Are we done?

- Interrupts
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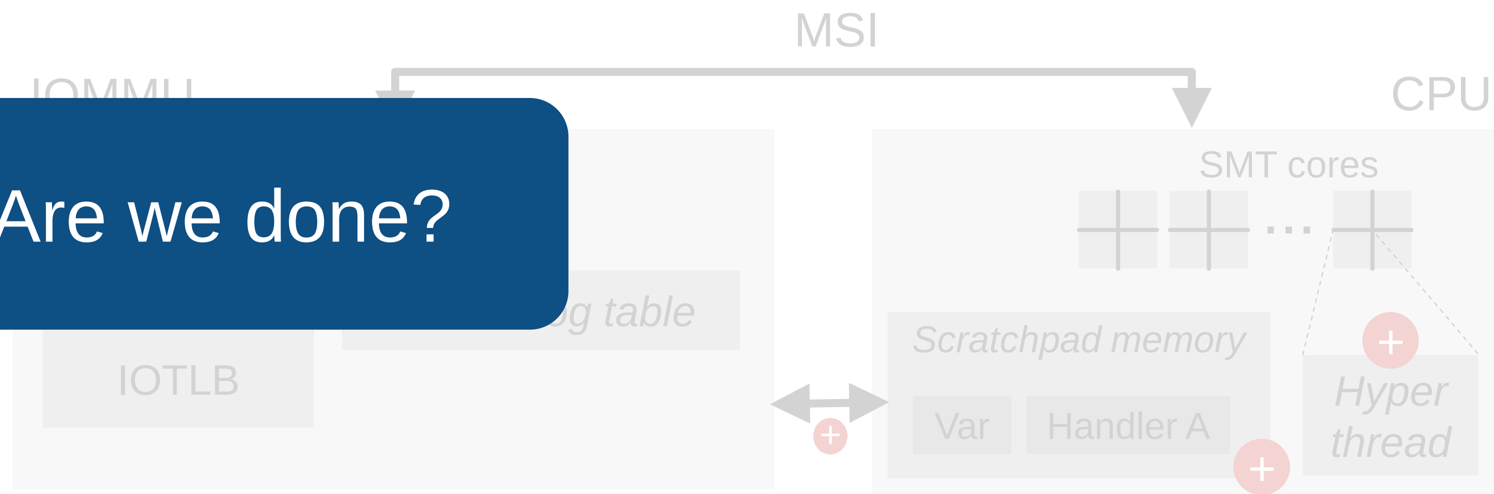


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Well…

# CONSISTENCY

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[1] K. Gharachorloo et al. Memory consistency and event ordering in scalable shared-memory multiprocessors. ISCA '90

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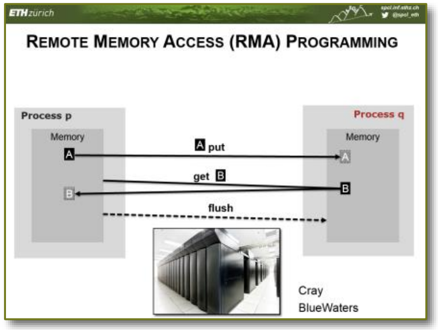


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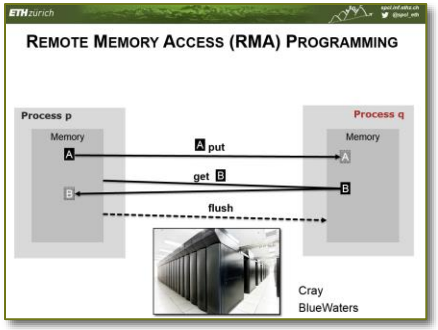


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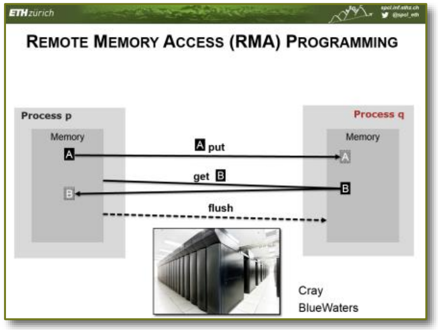


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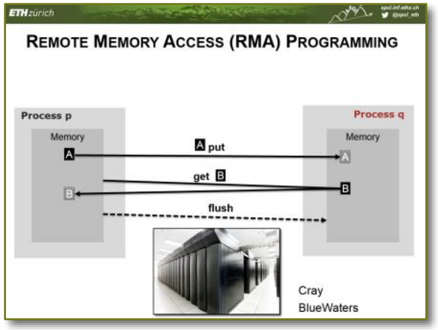


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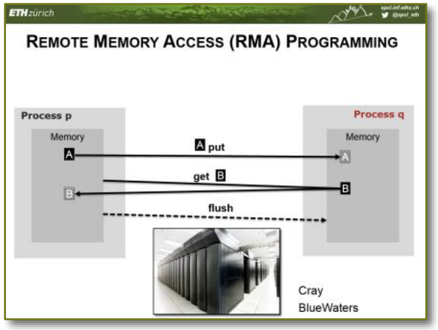


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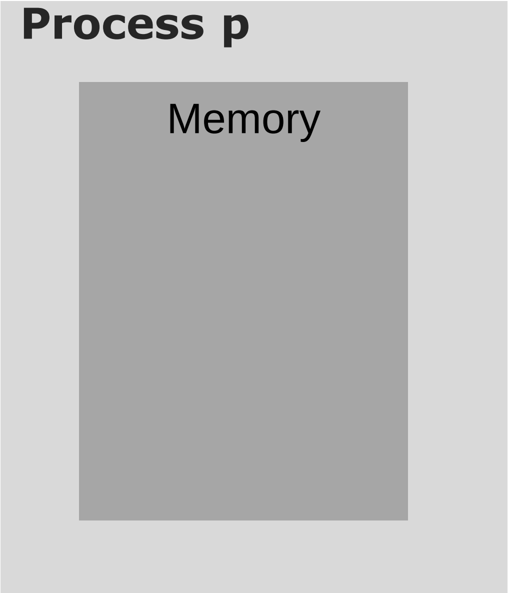


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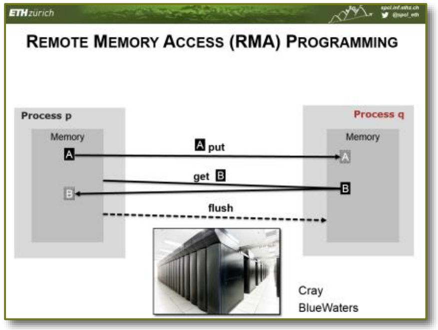


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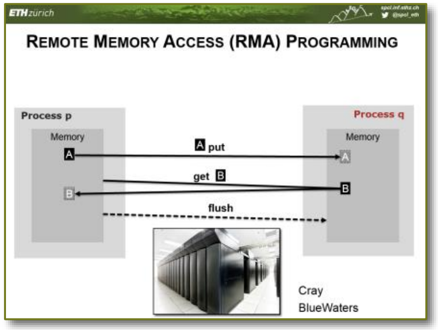


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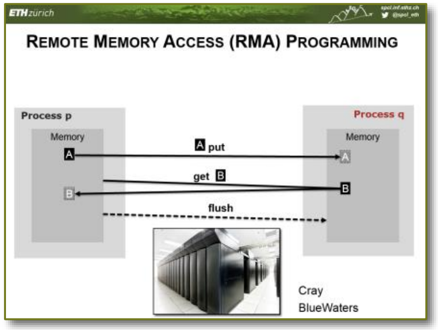


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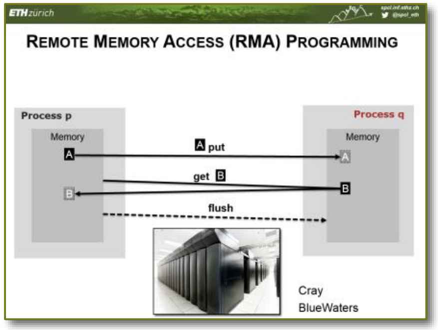


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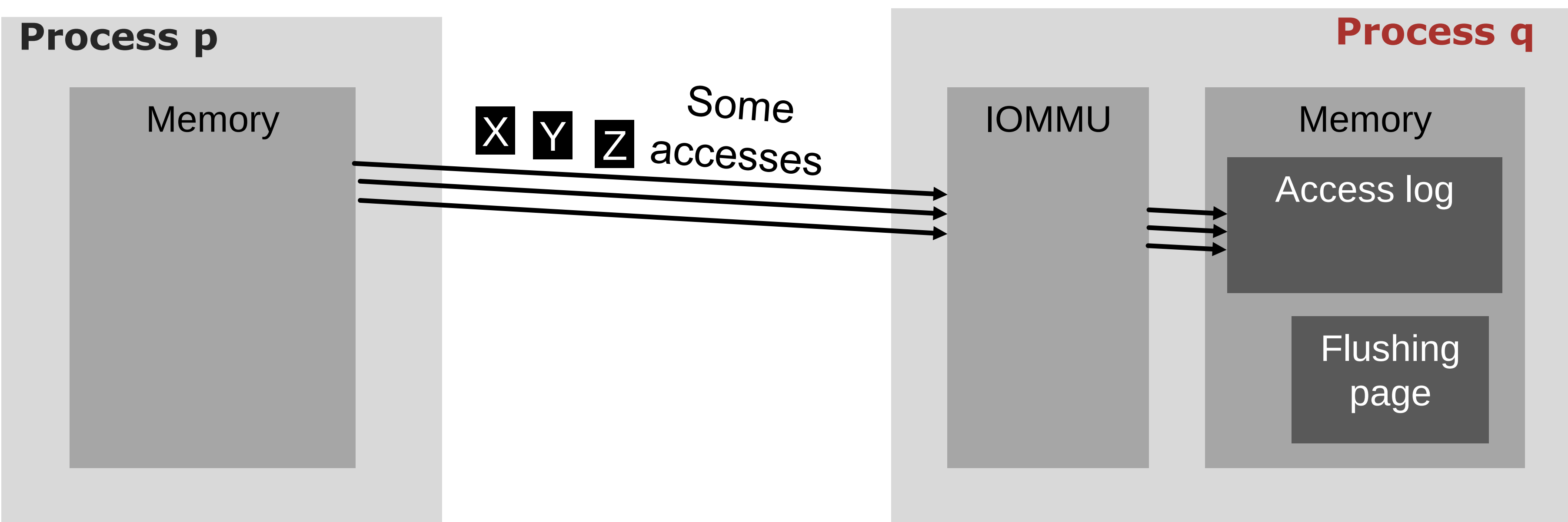


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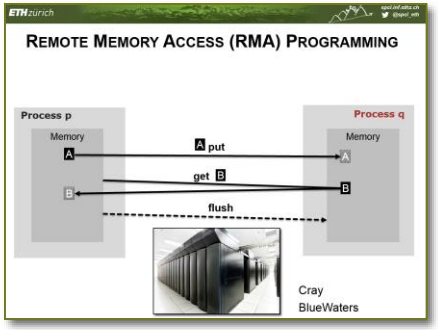


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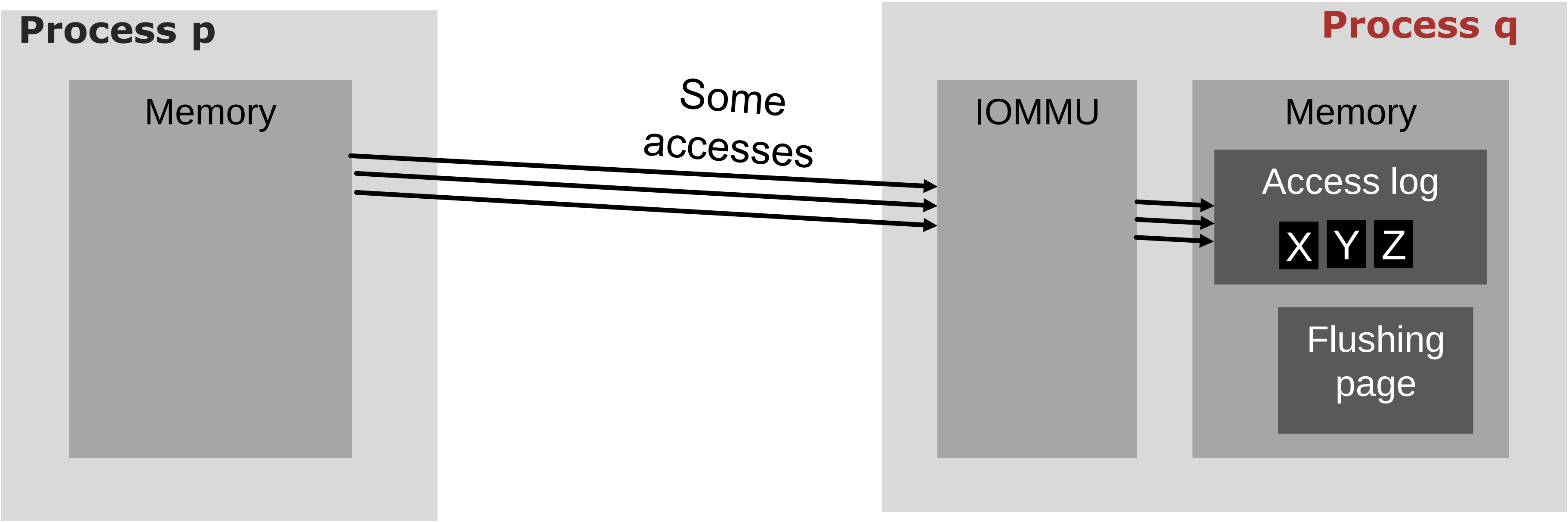


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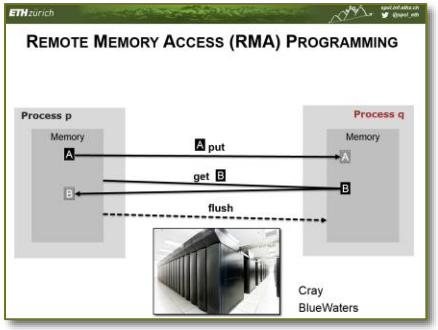


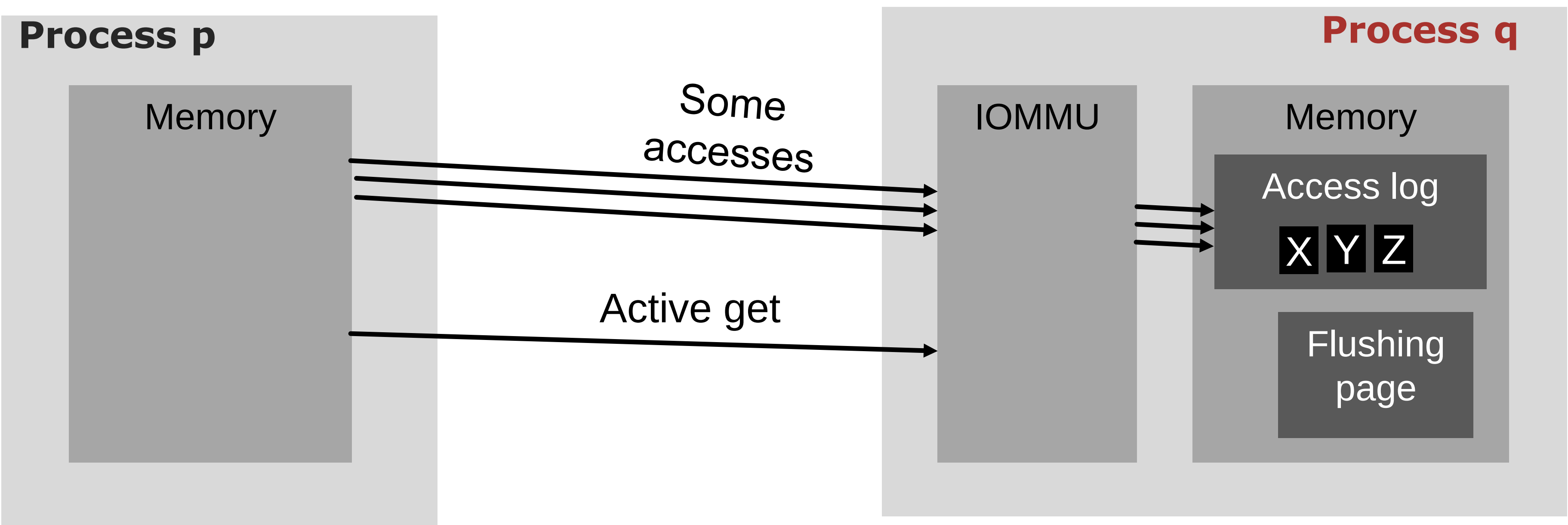


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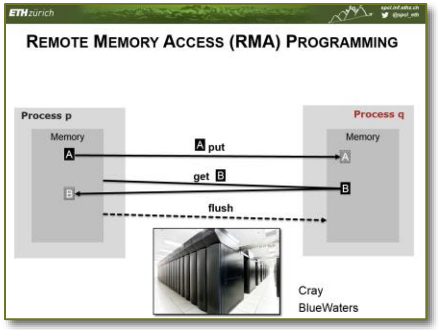


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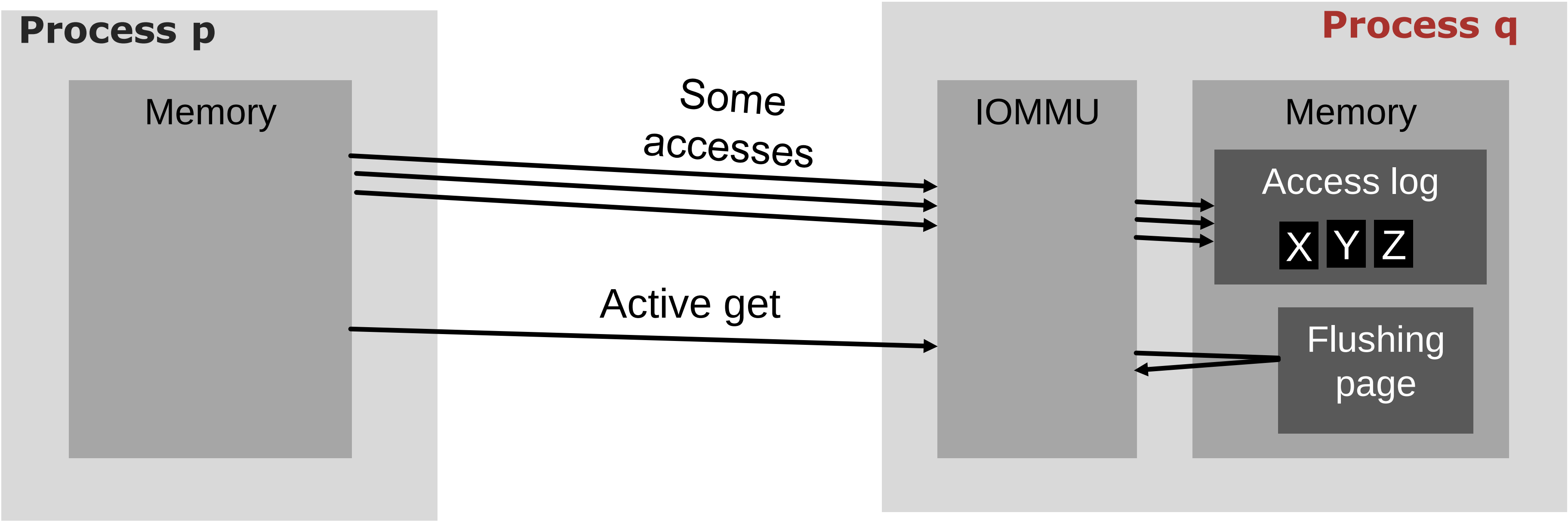


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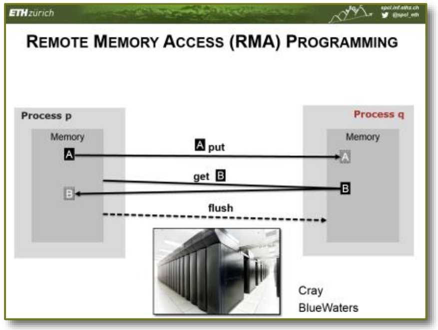


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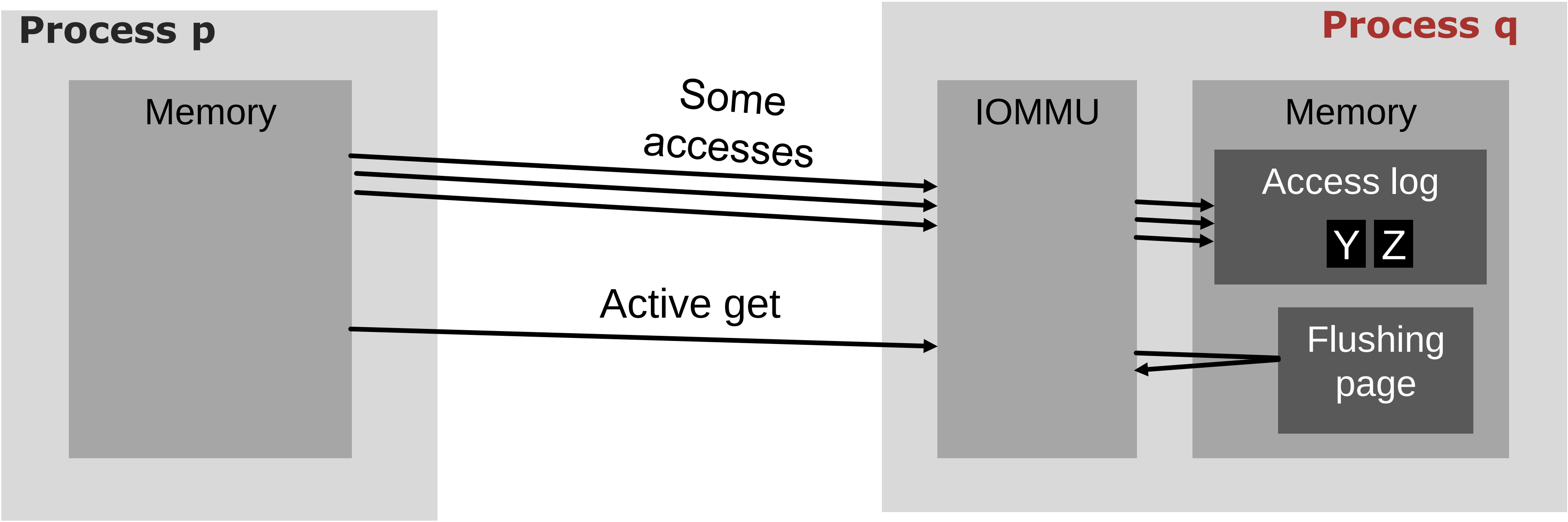


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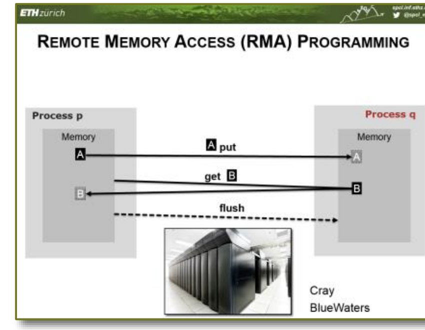


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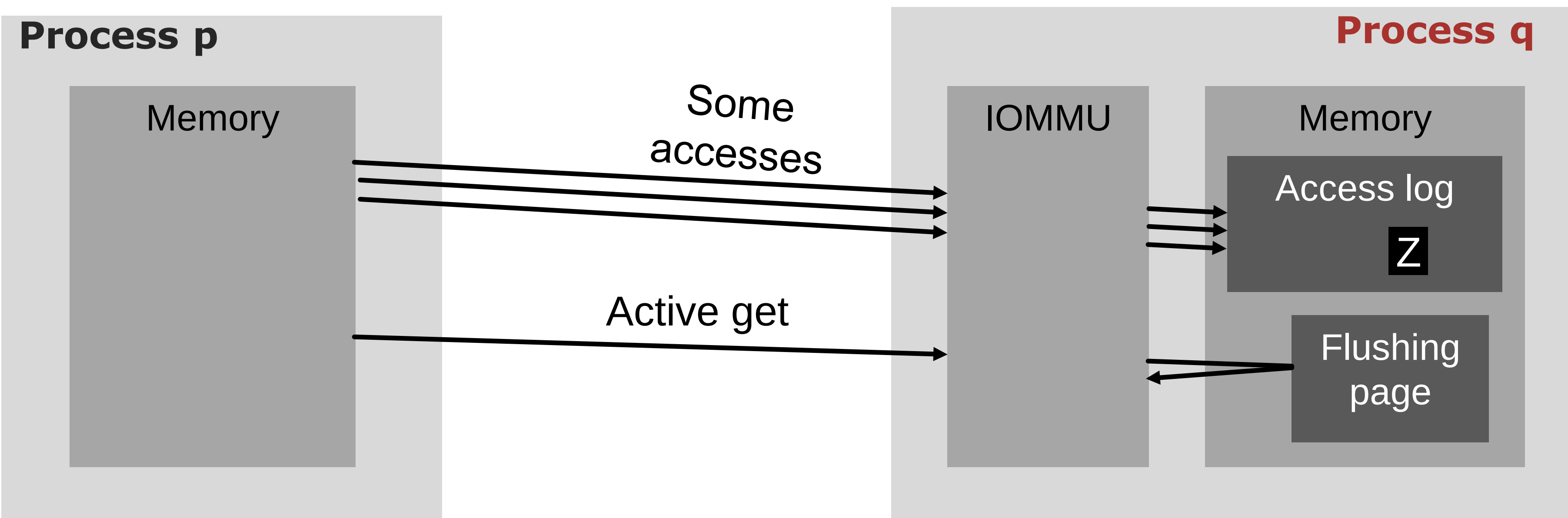


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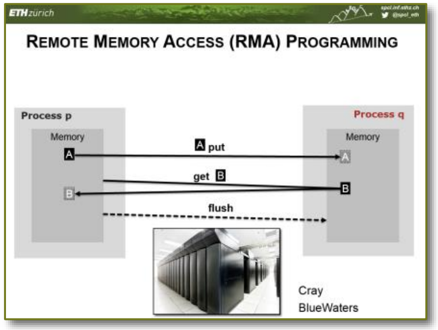


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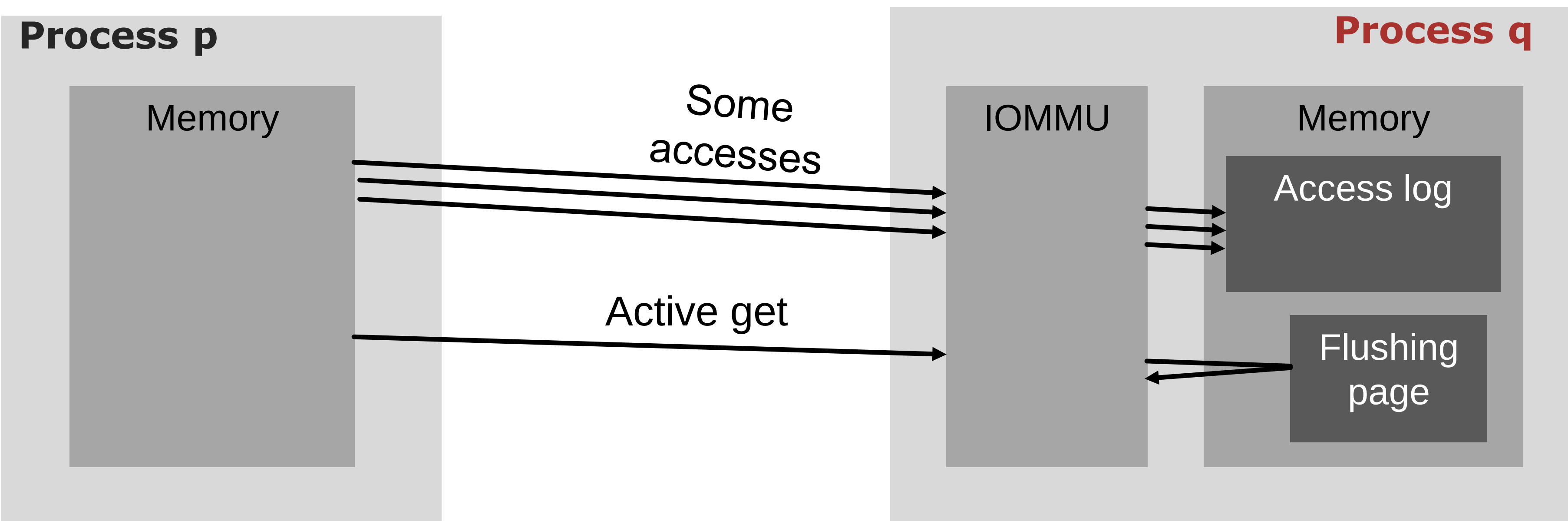


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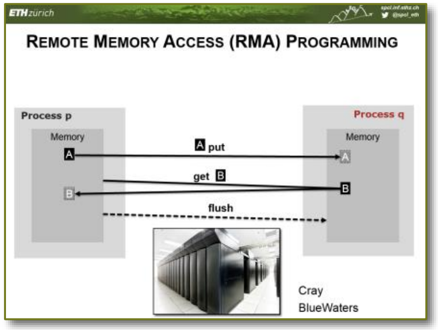


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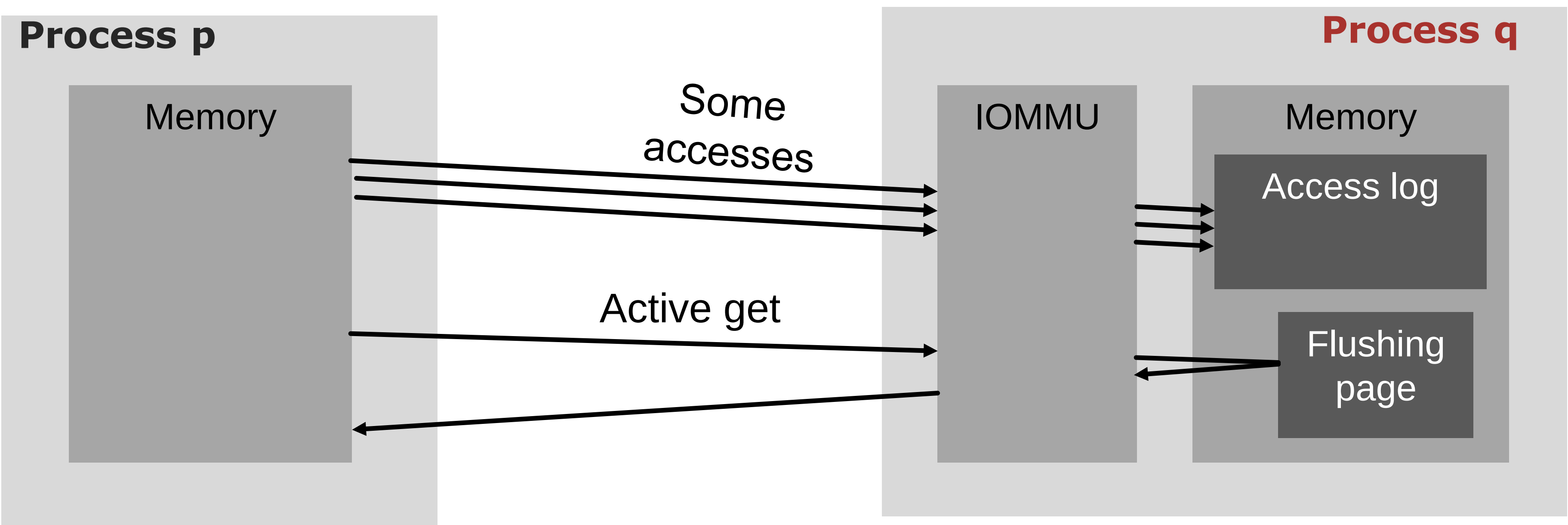


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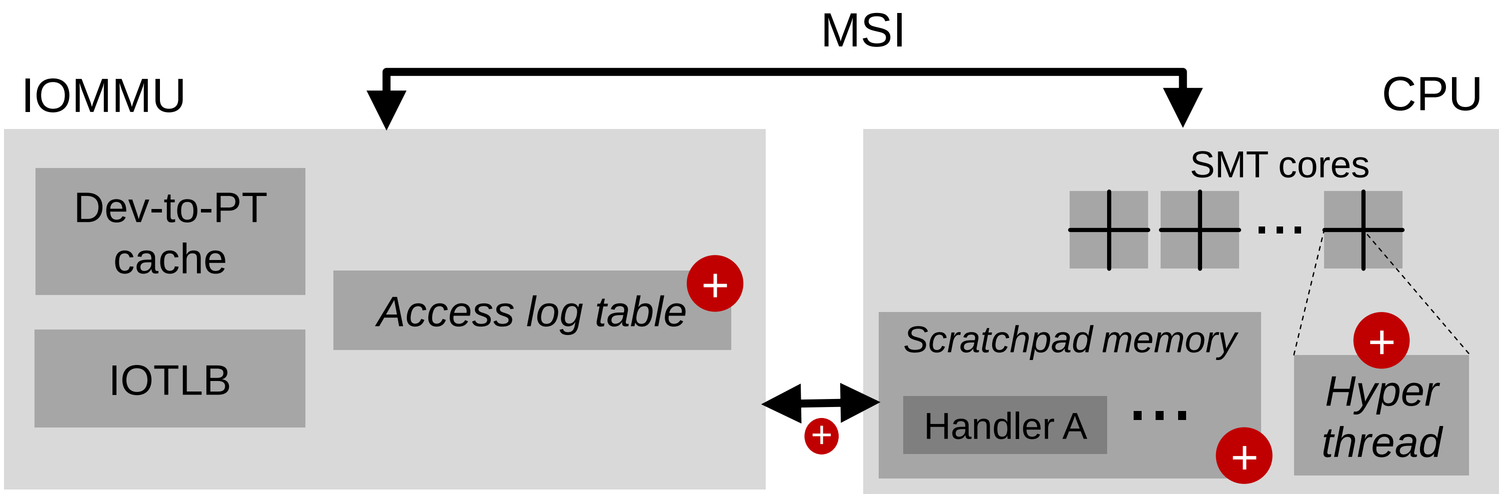

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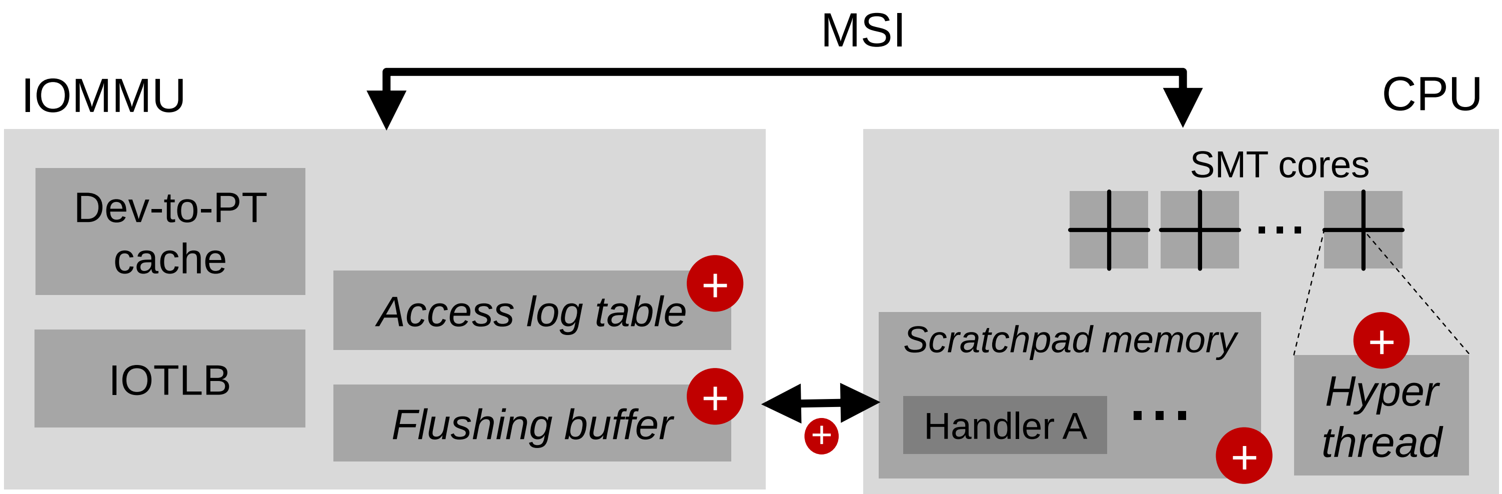

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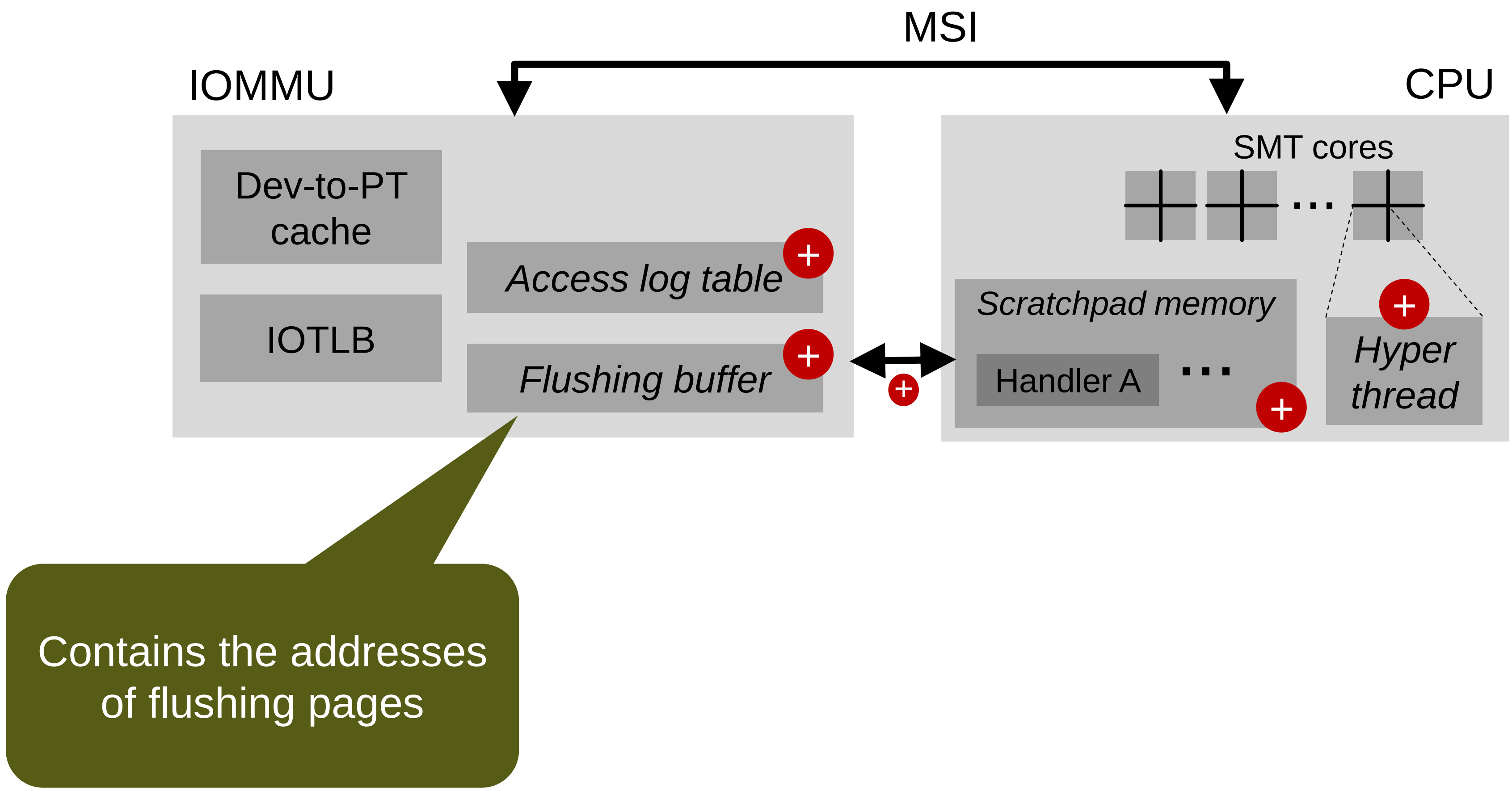

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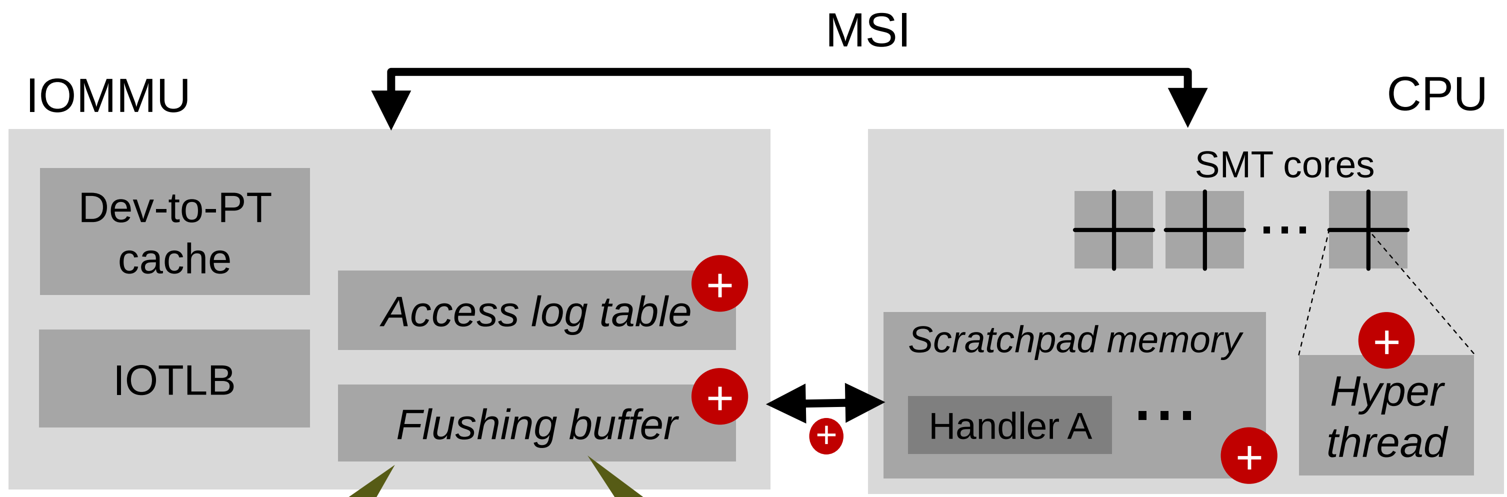


Contains the addresses of flushing pages

Maps flushing pages to IUIDs and access logs

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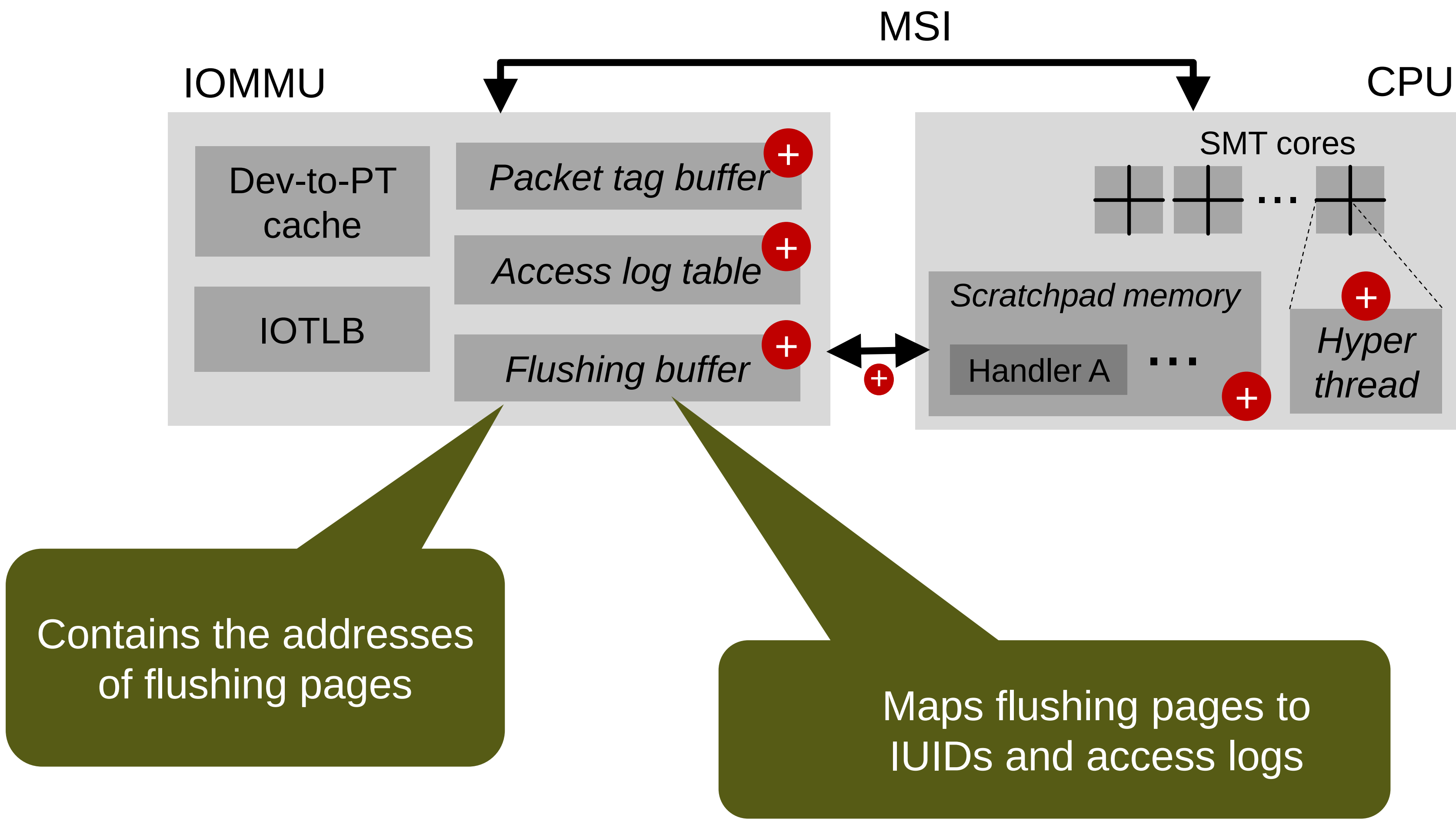

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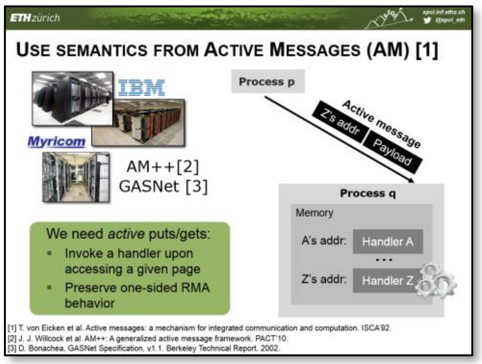


Active Messages

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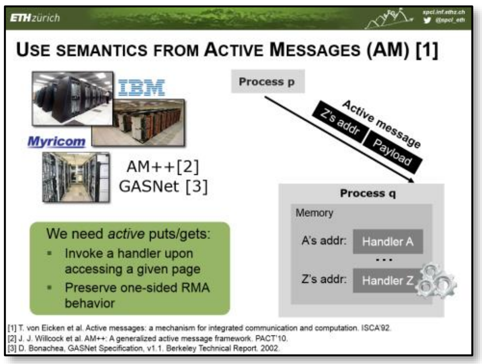


Active Messages

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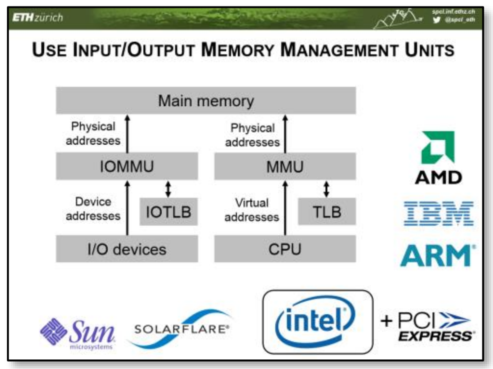

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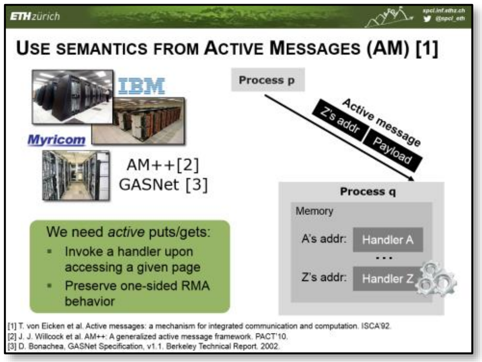


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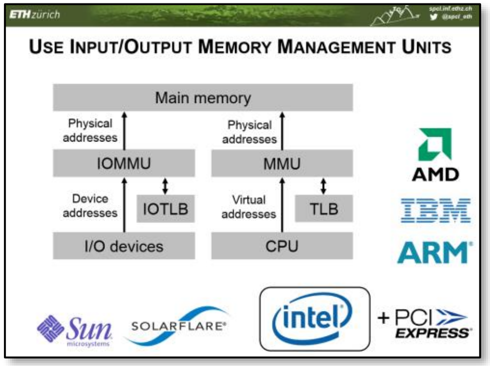
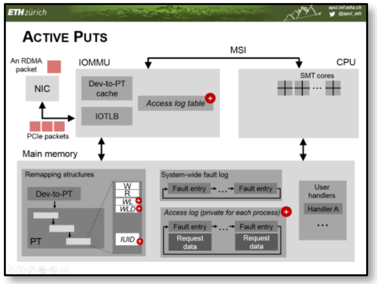
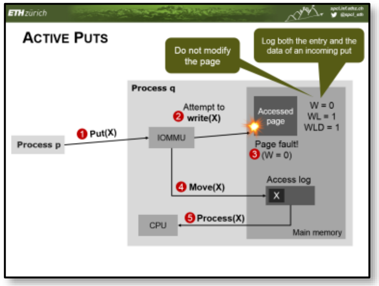



Active Puts/Gets



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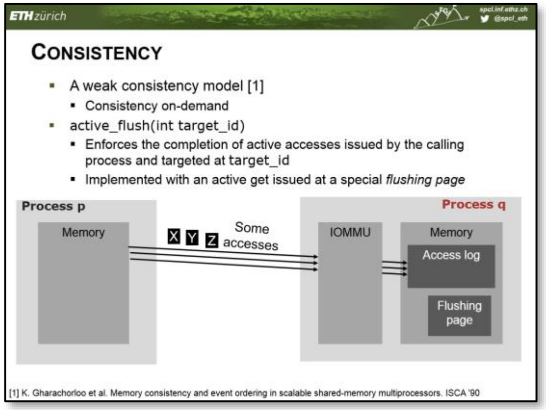


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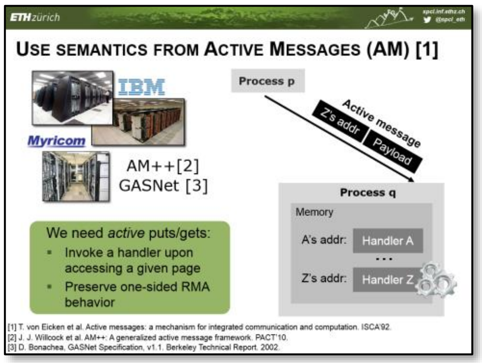


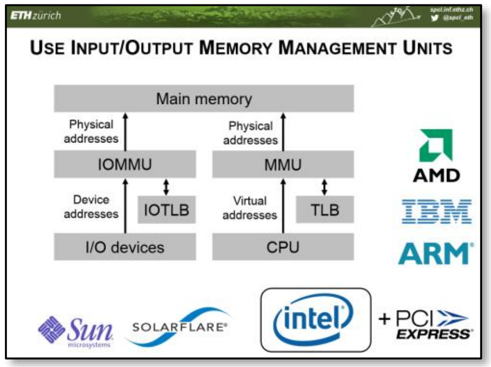


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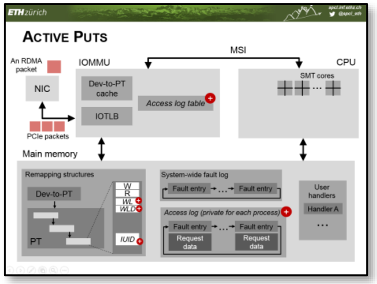


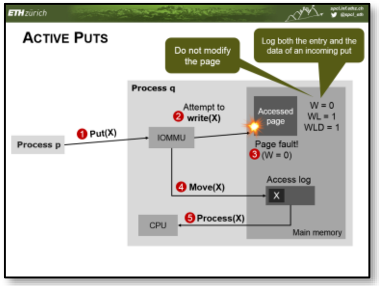

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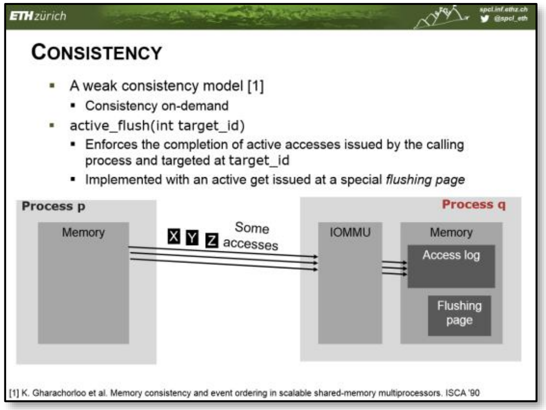


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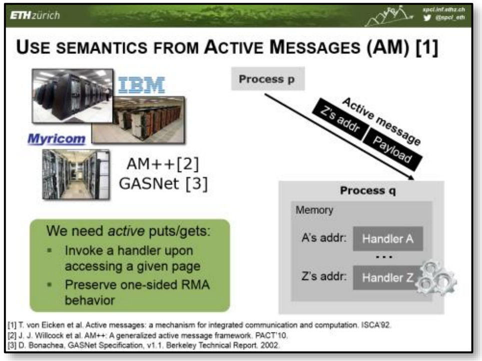


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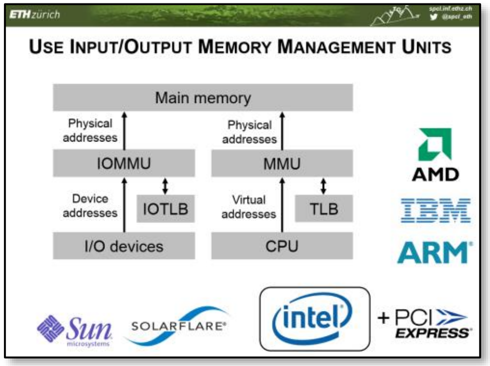


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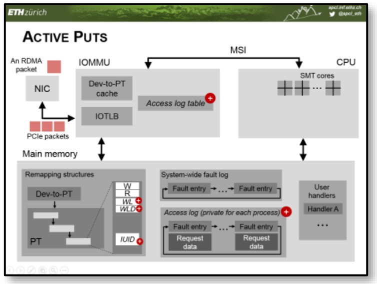


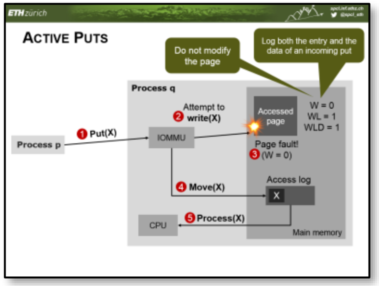


# How can we use it?

# ACTIVE ACCESS USE-CASES

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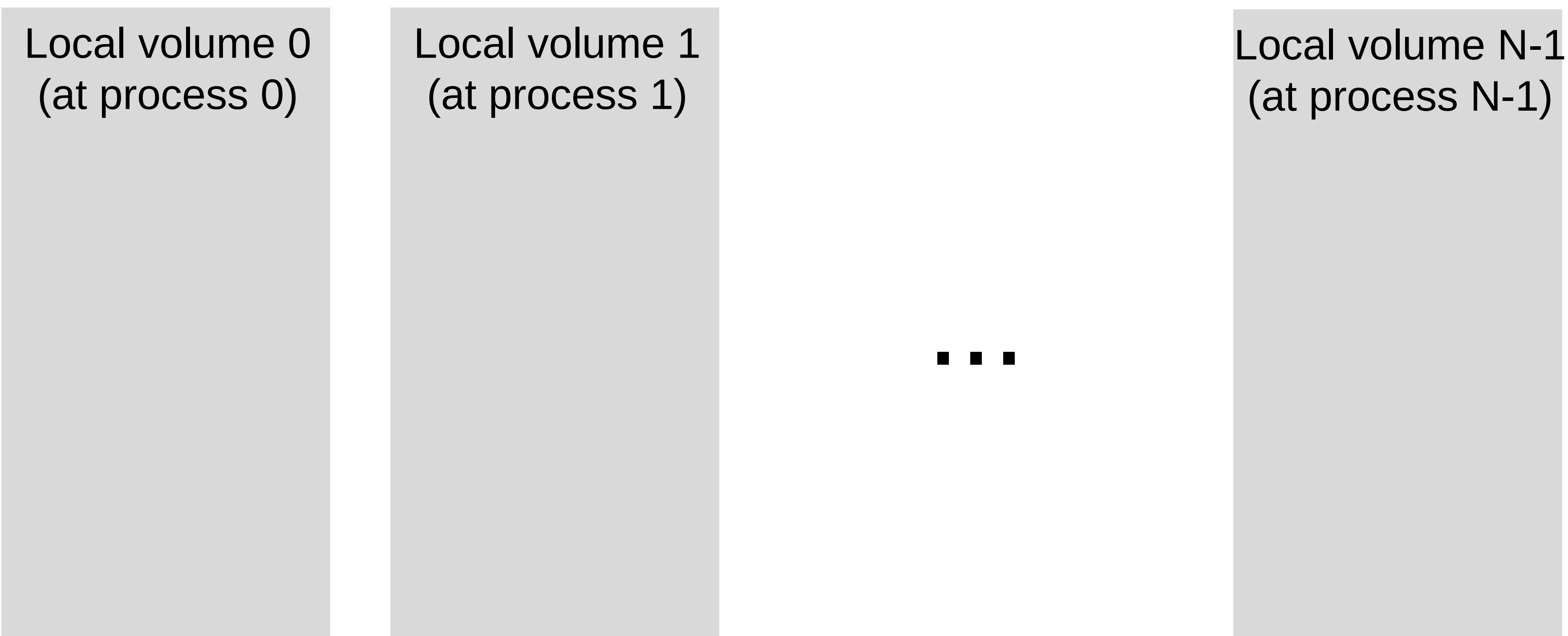


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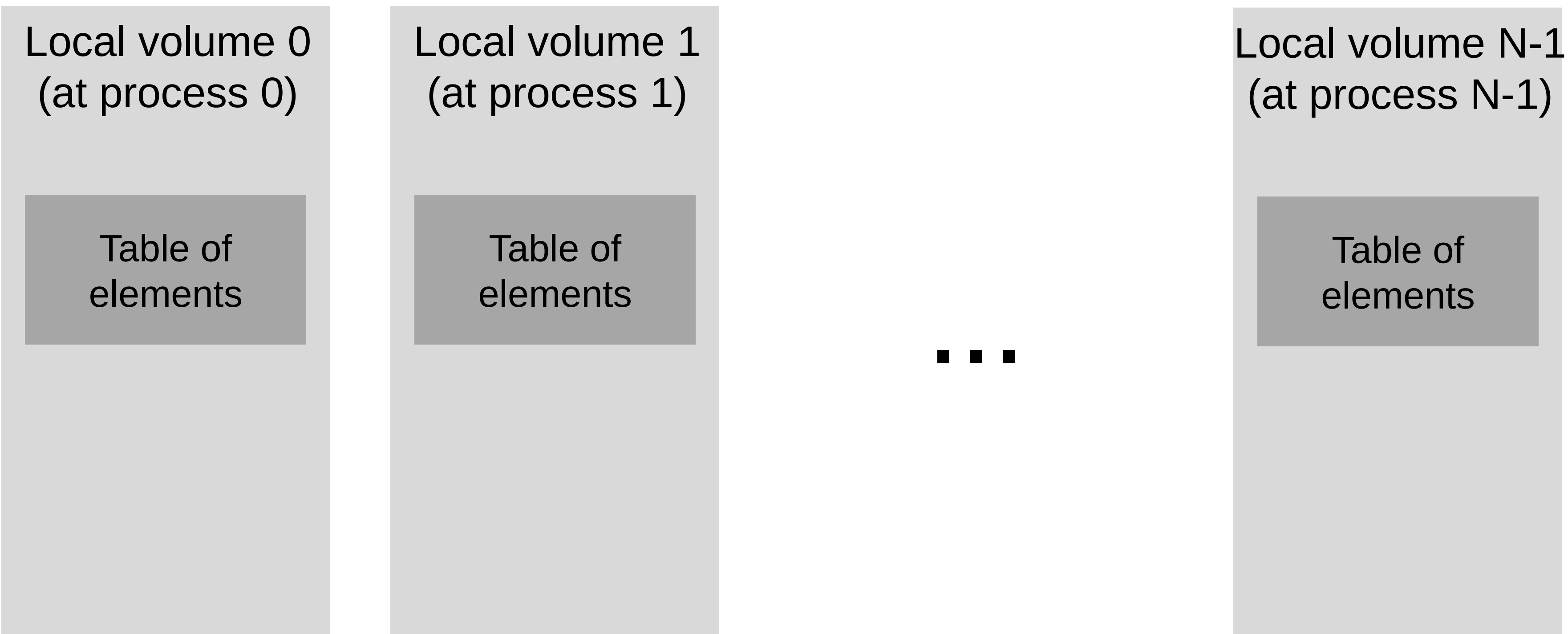


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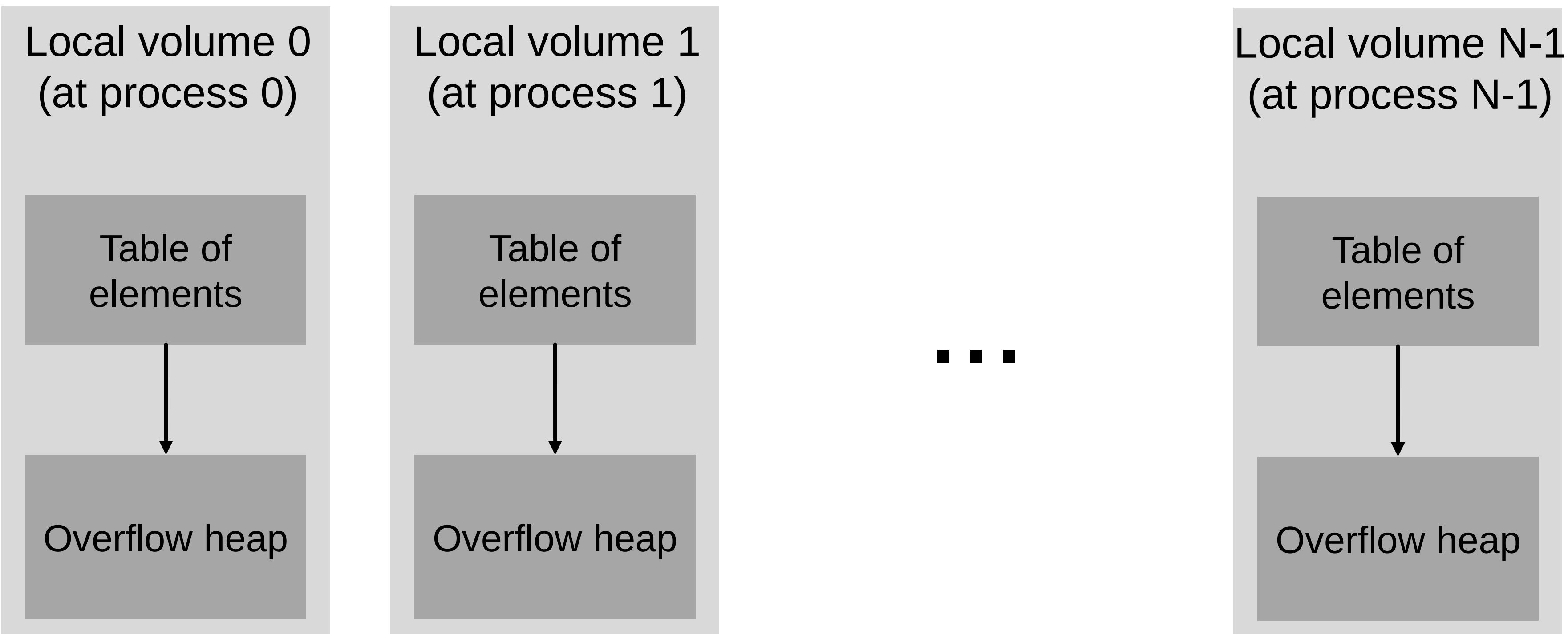


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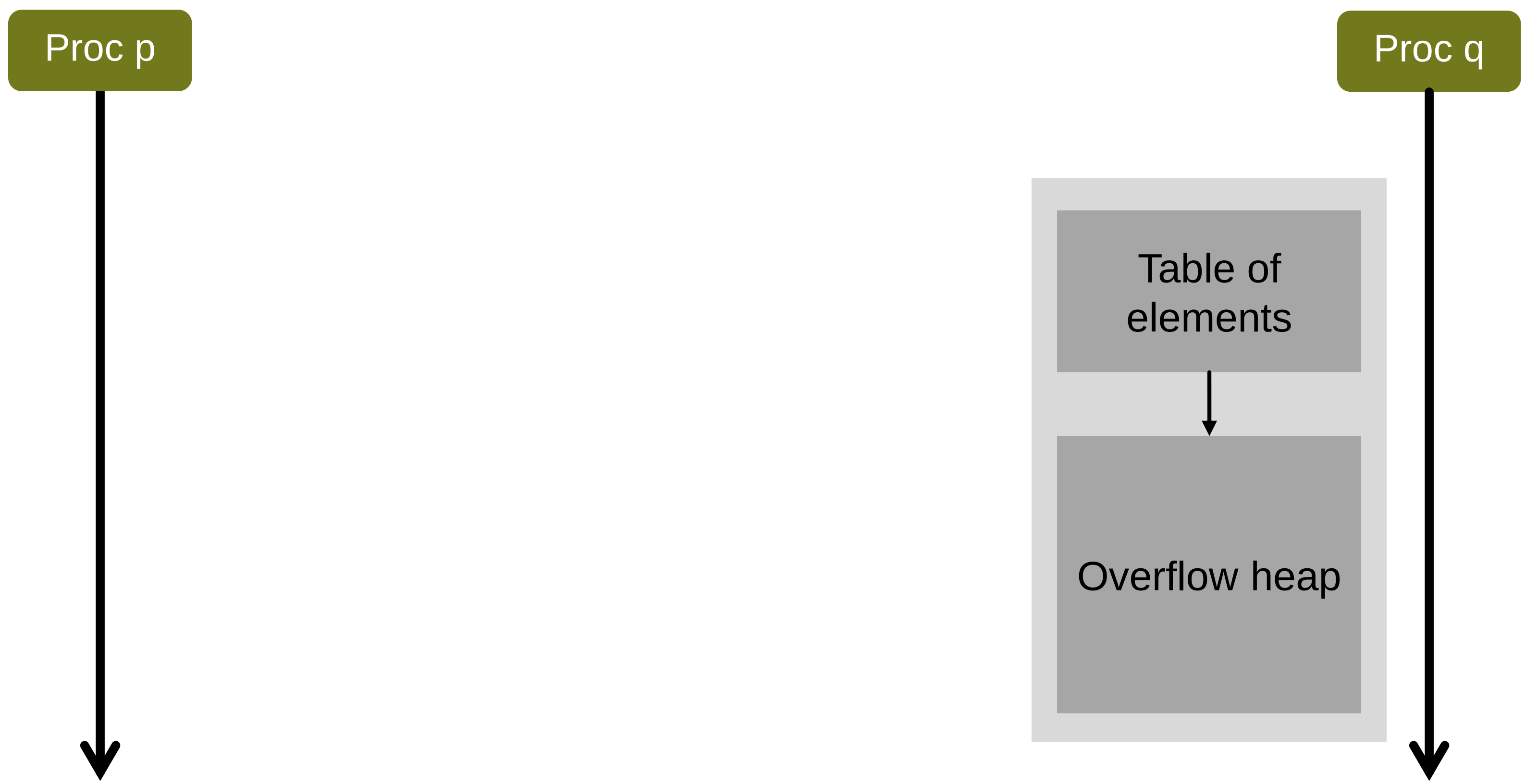

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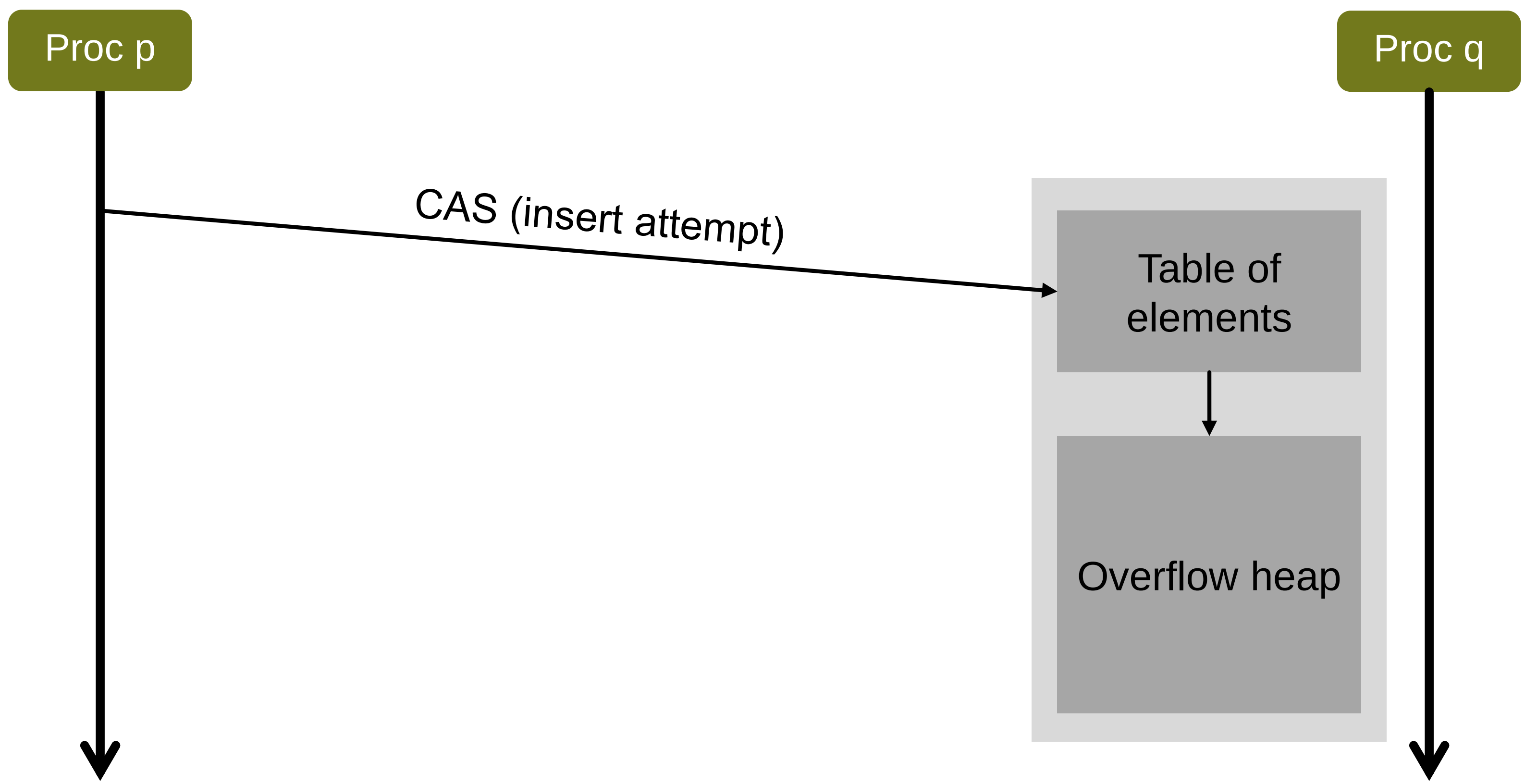

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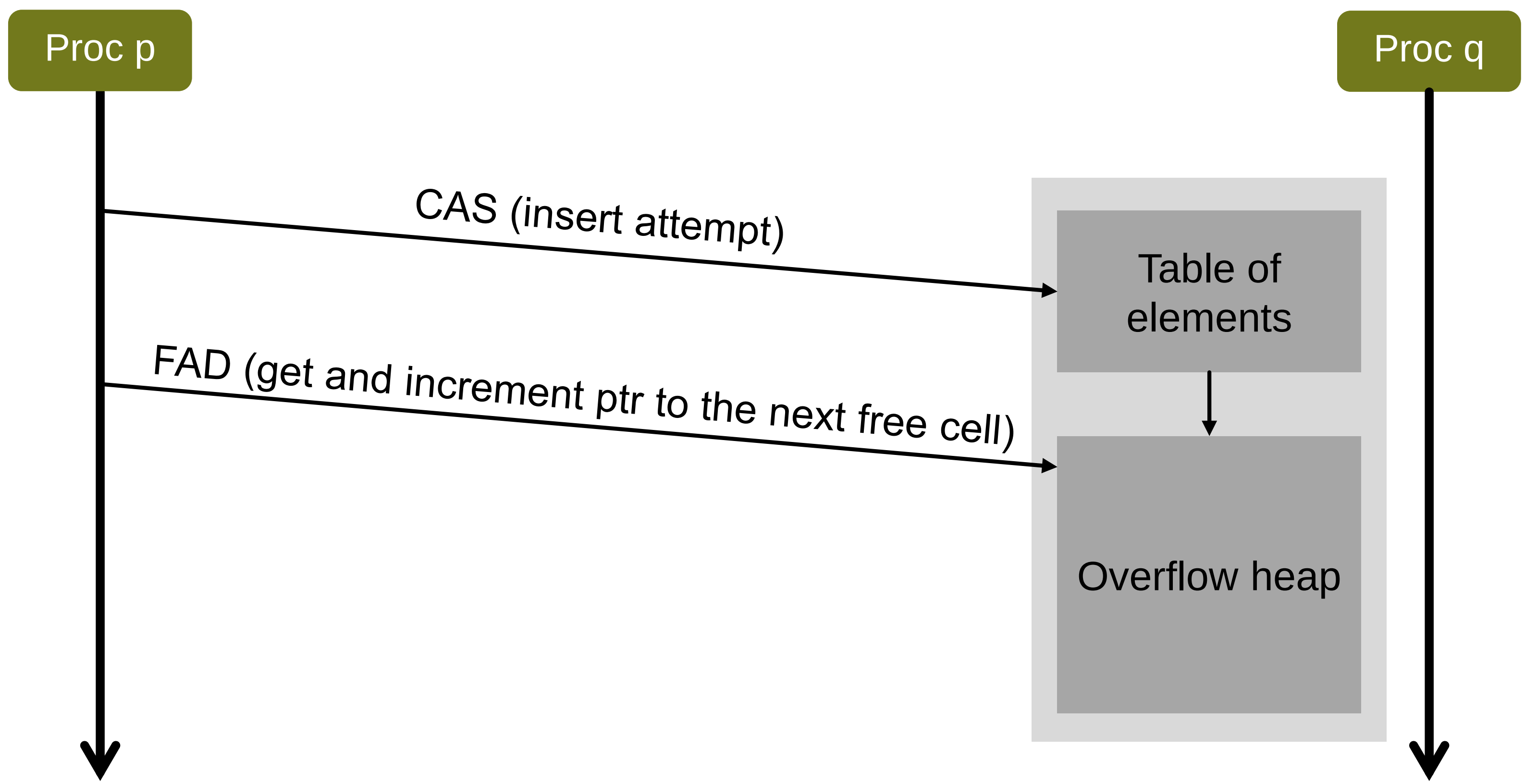

# Active Access Use-Cases

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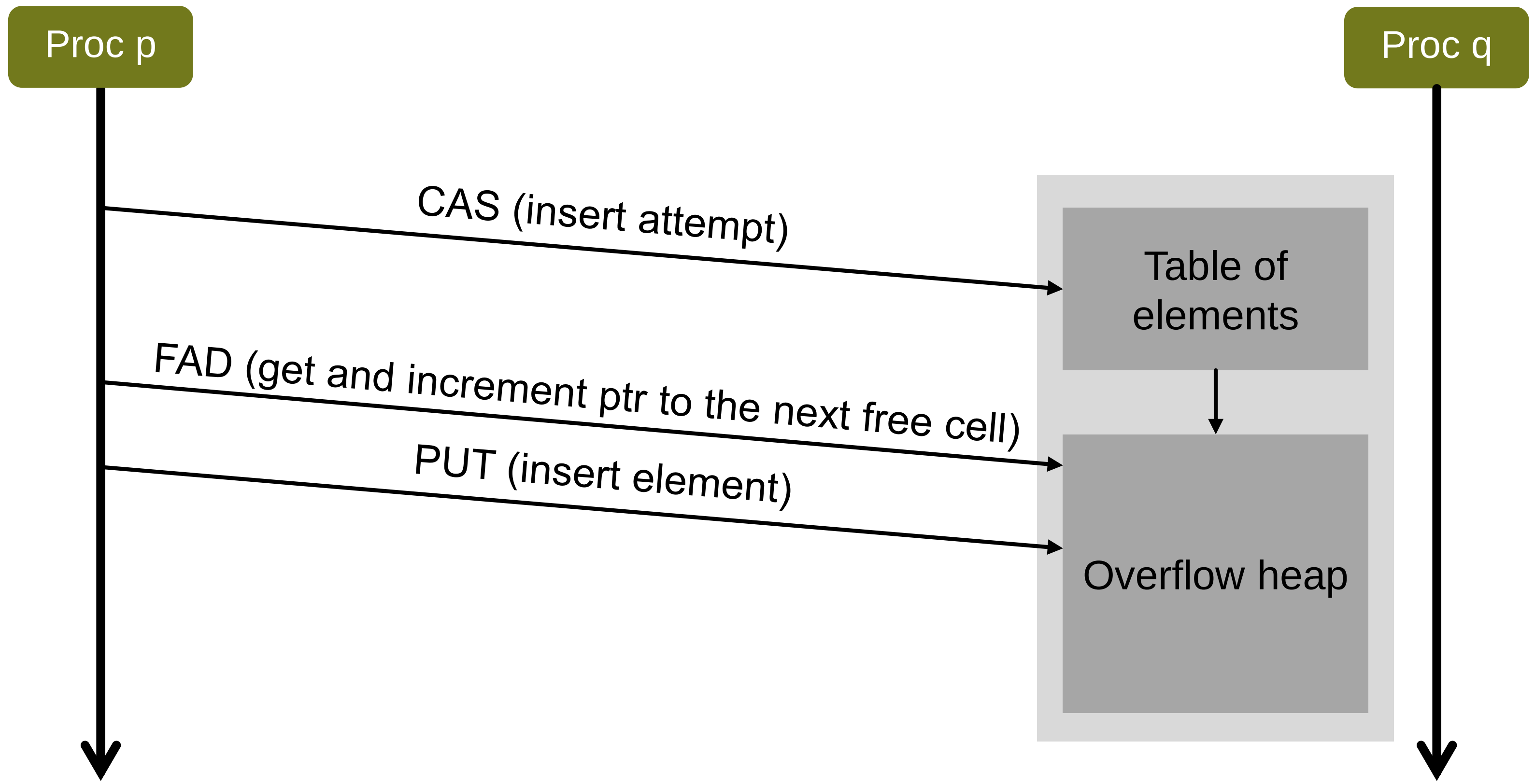

# ACTIVE ACCESS USE-CASES

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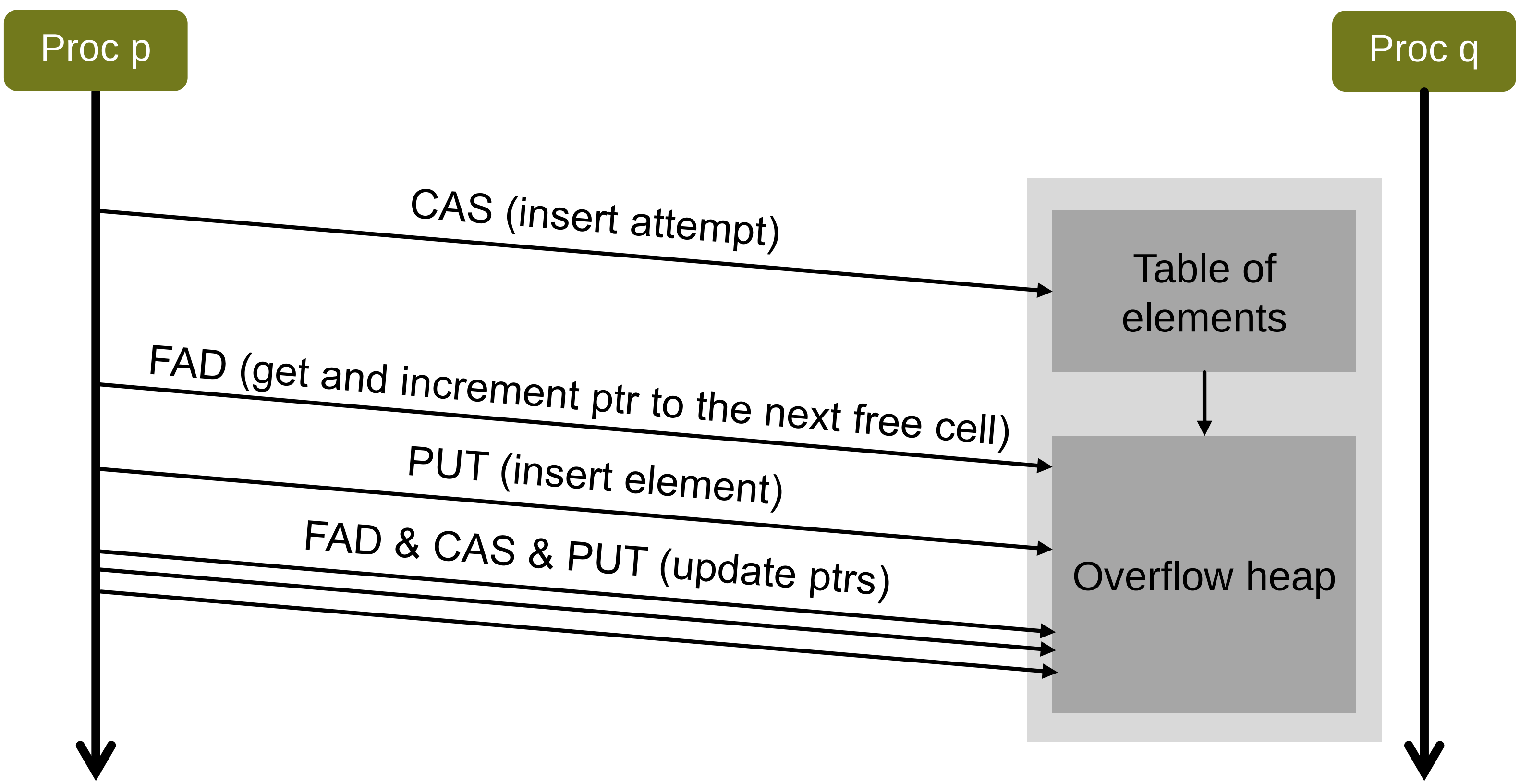

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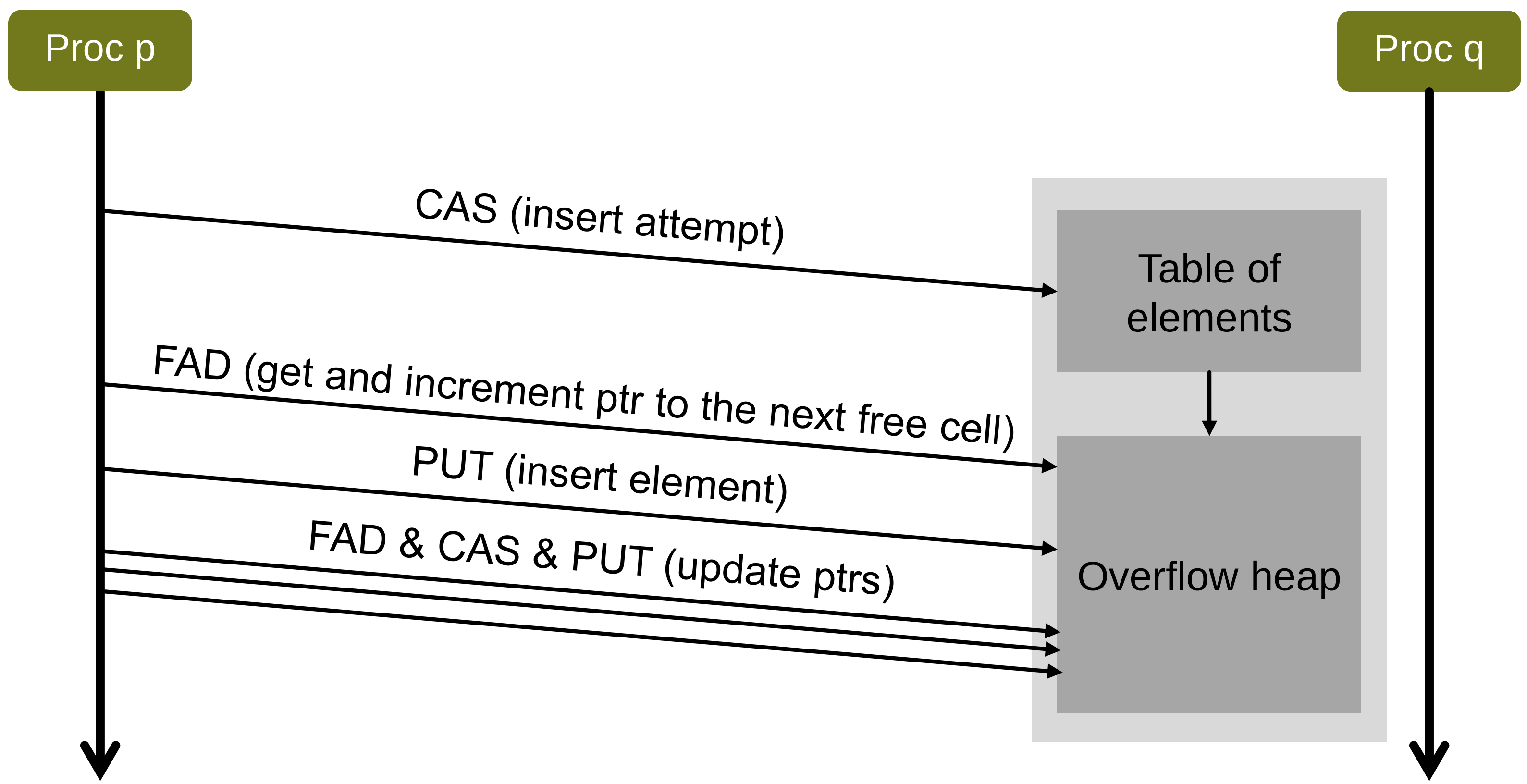
## Distributed Hashtable: Inserts (AA)



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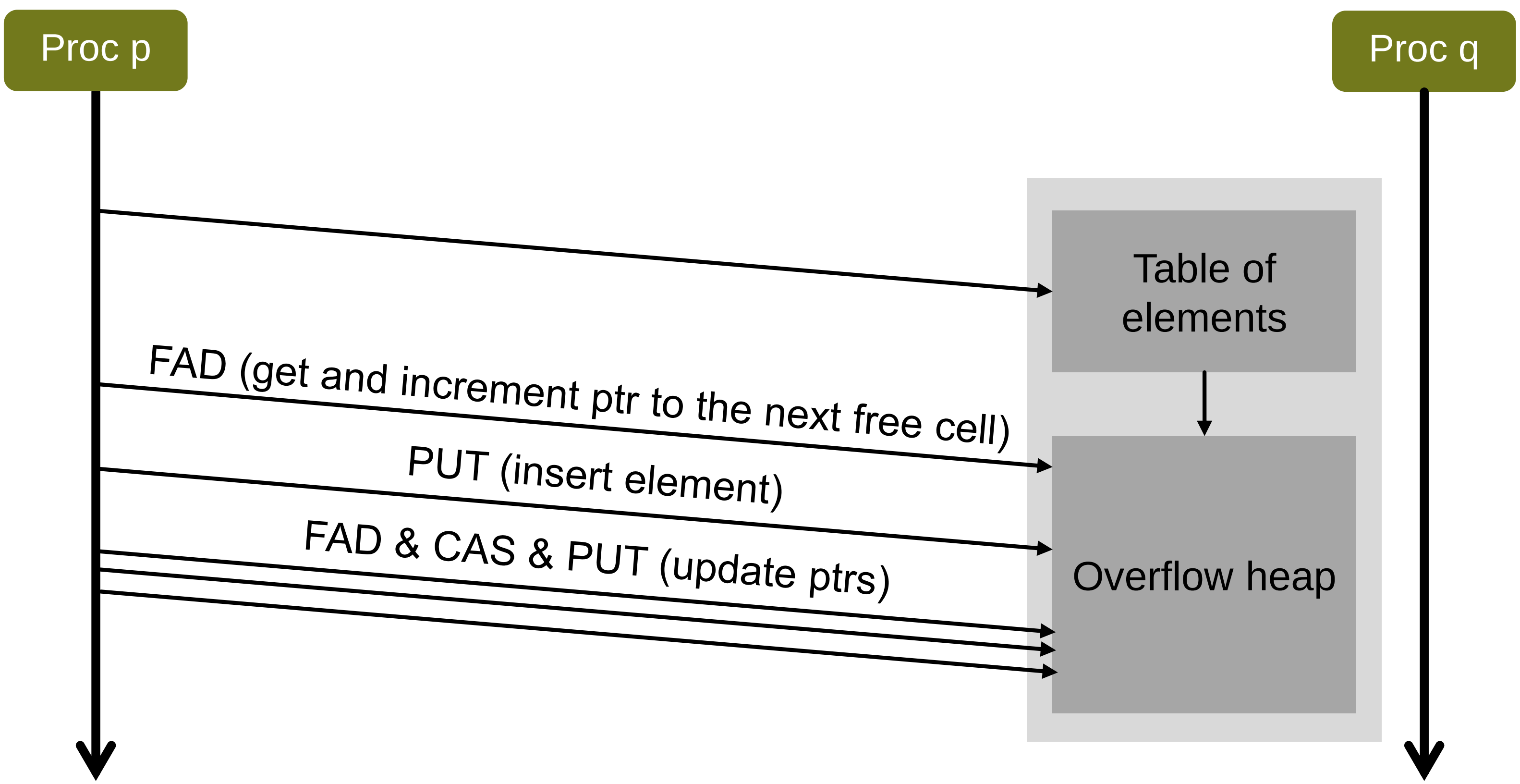

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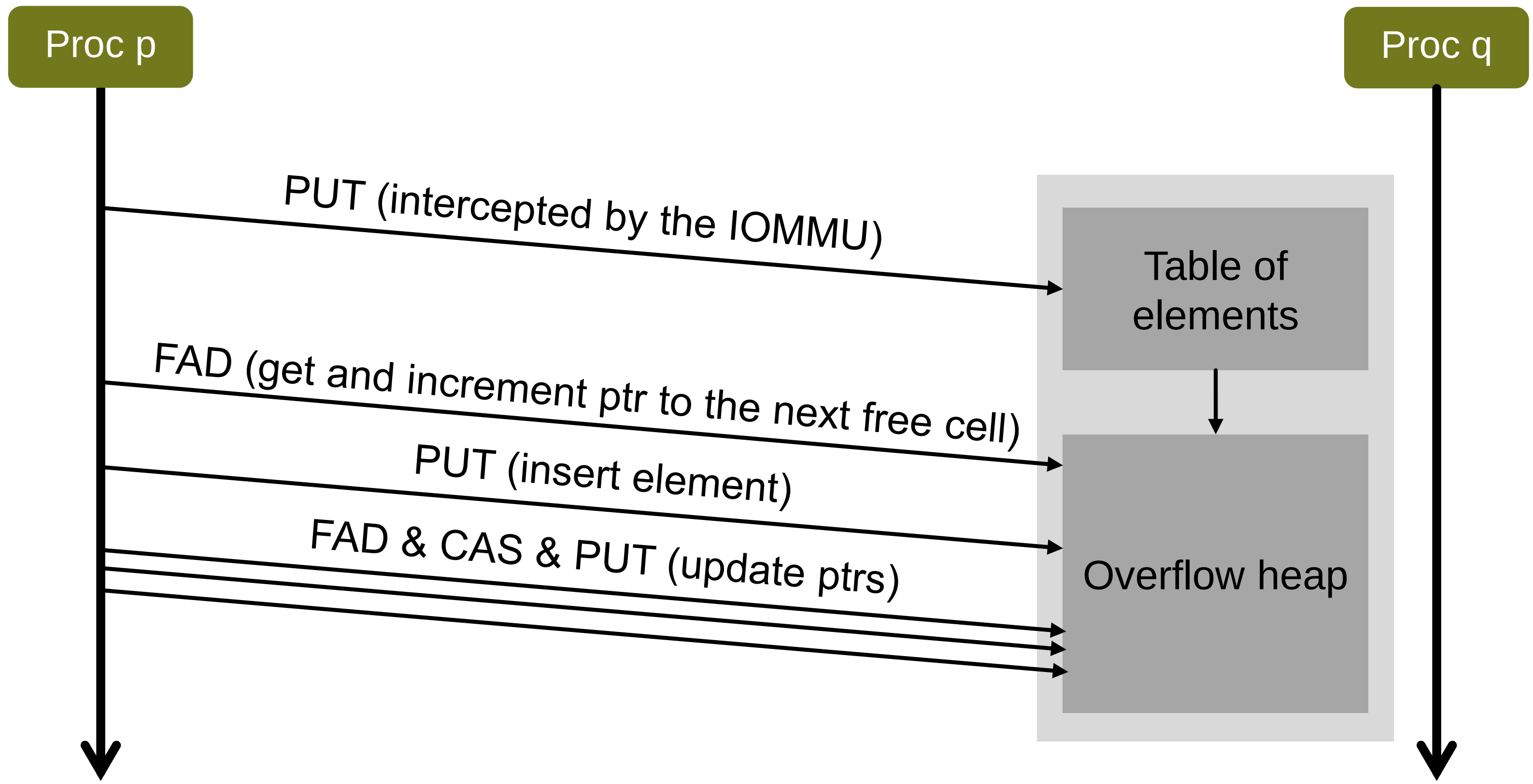

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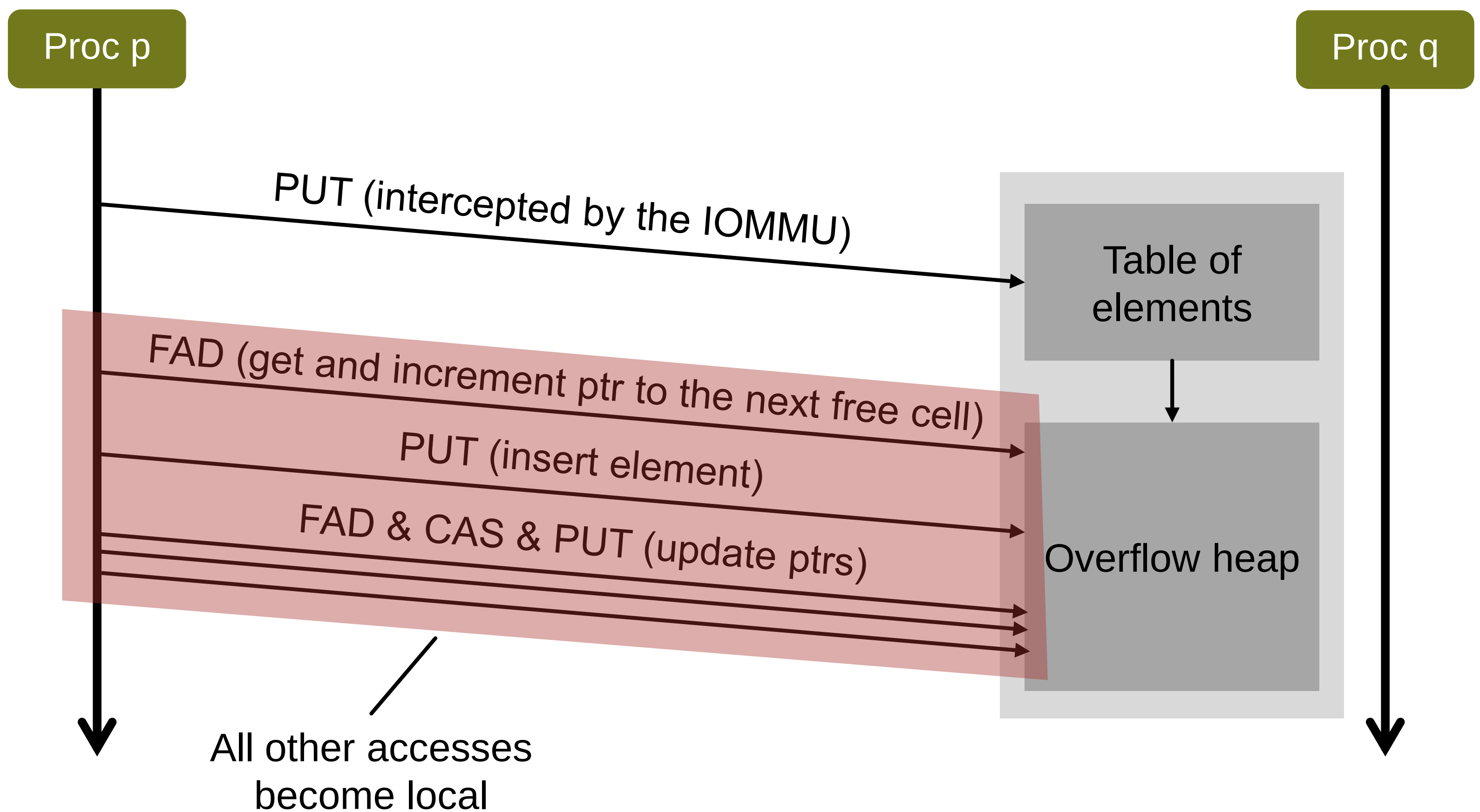

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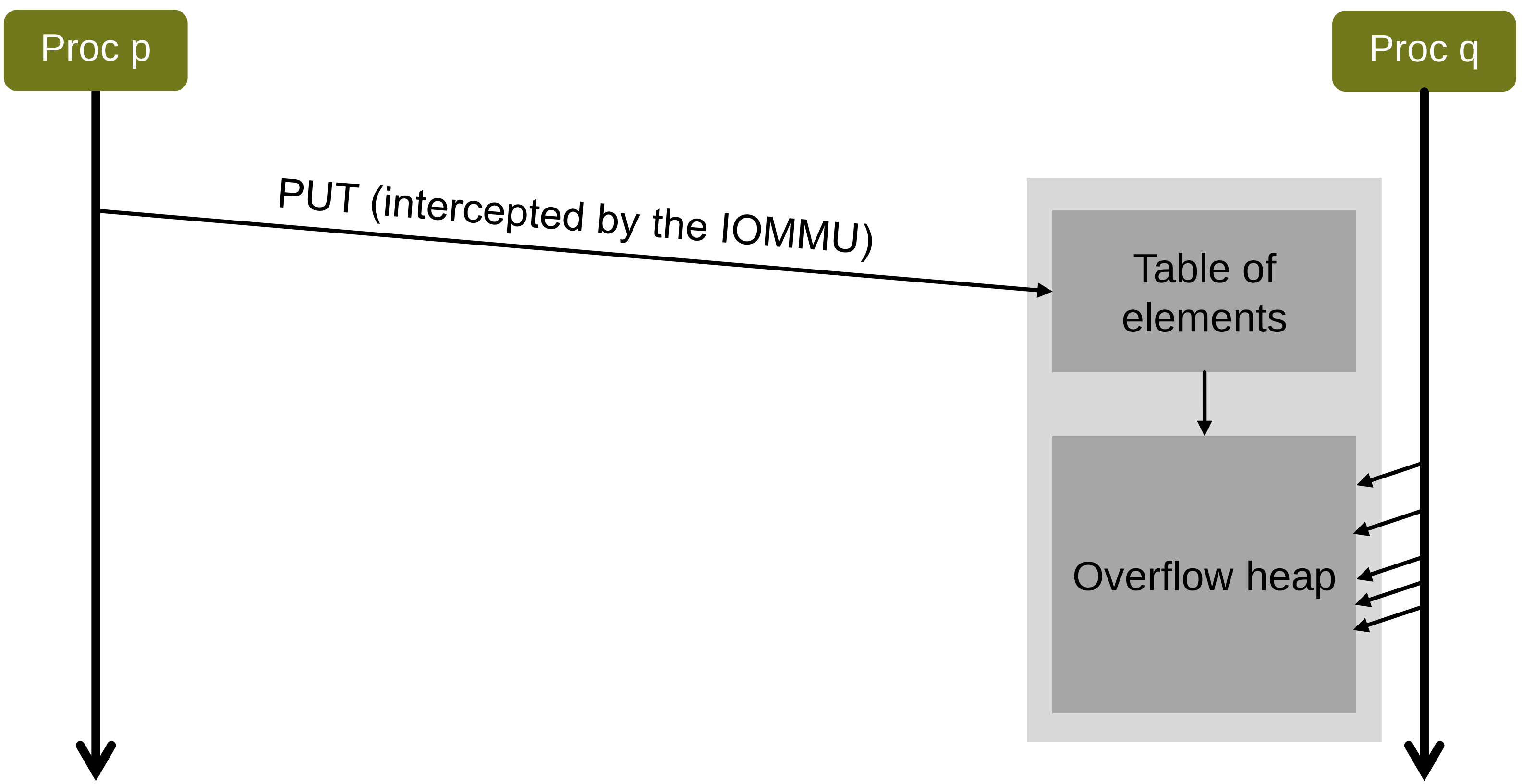
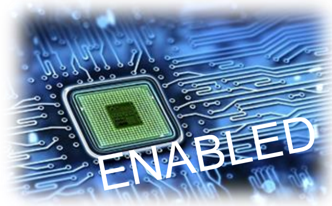


# Active Access Use-Cases

## Virtual Global Address Space (V-GAS)

# ACTIVE ACCESS USE-CASES

## VIRTUAL GLOBAL ADDRESS SPACE (V-GAS)



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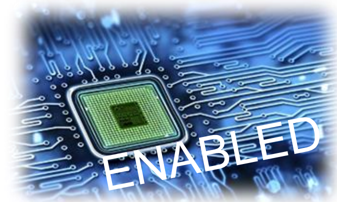


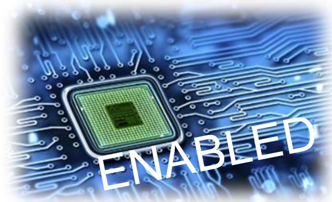

Machine 0

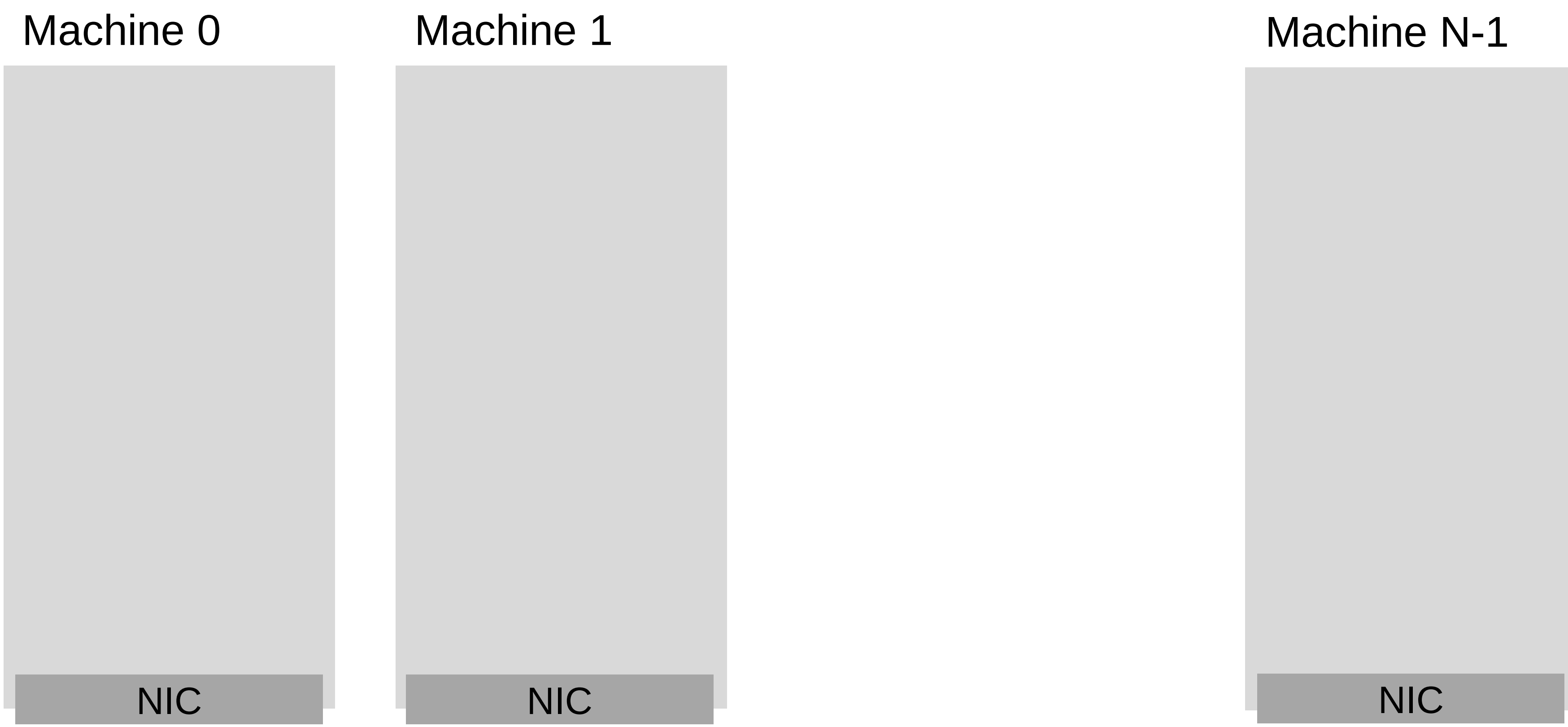
Machine 1

Machine N-1

# Active Access Use-Cases

## Virtual Global Address Space (V-GAS)



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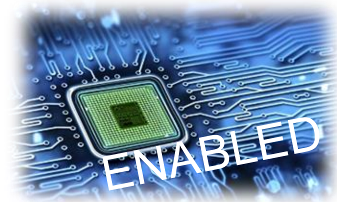


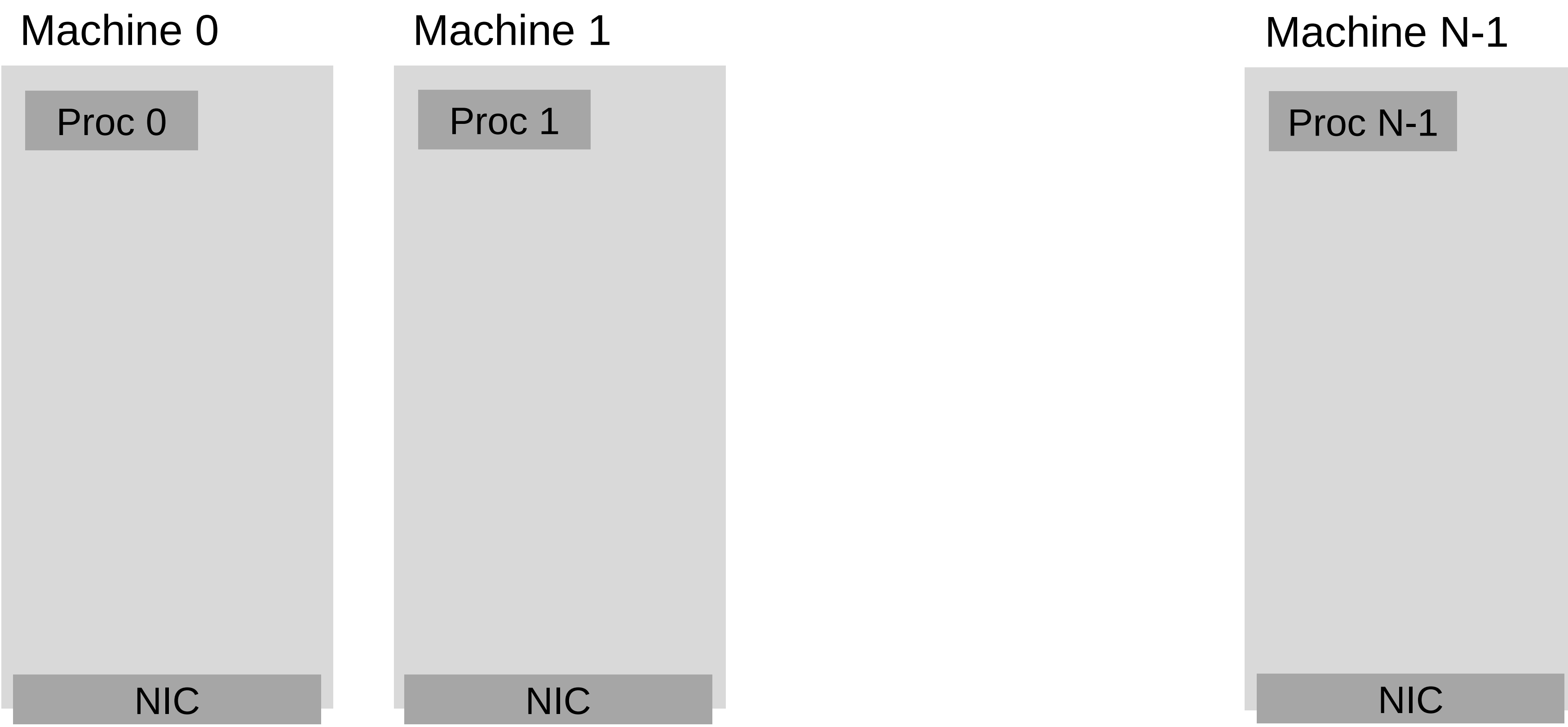

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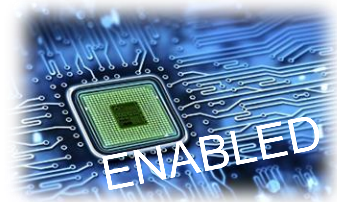


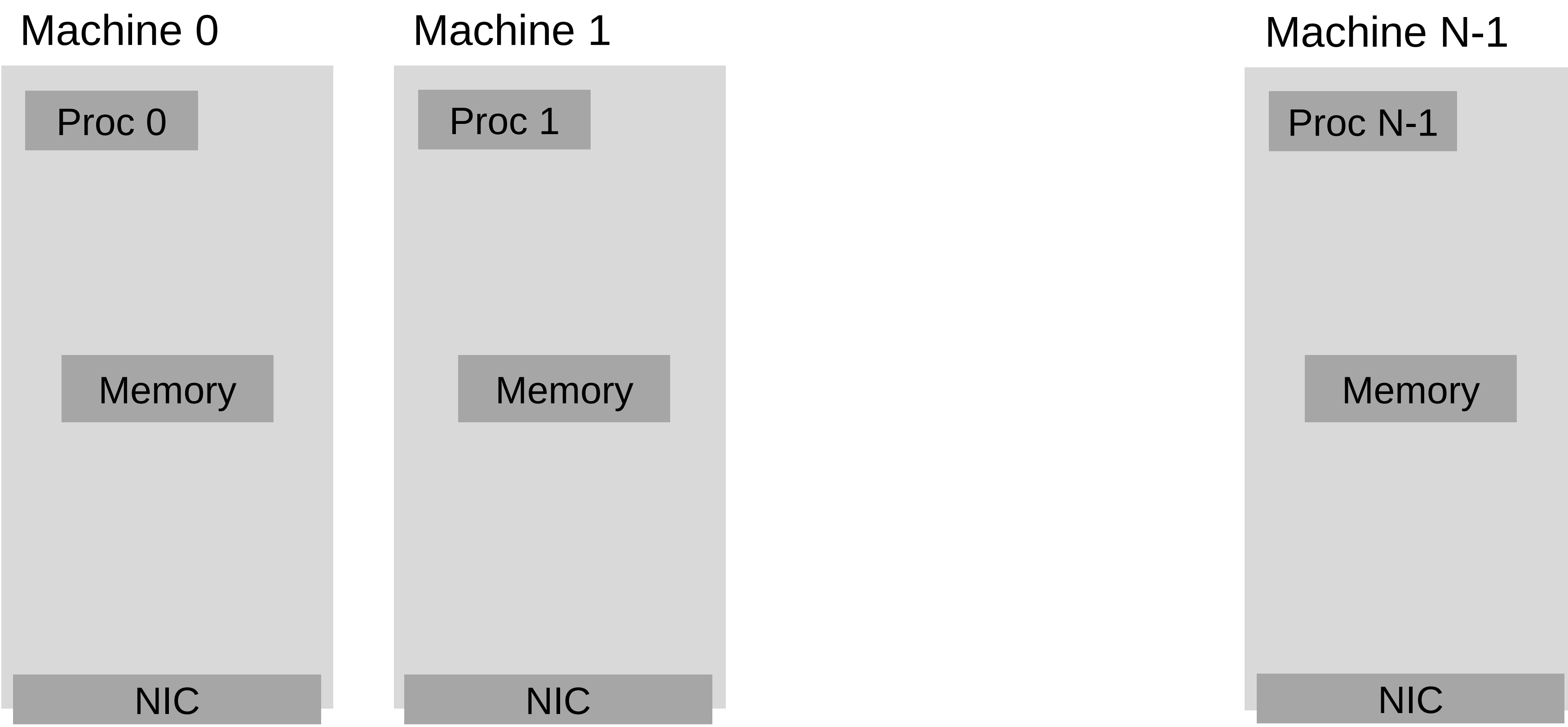

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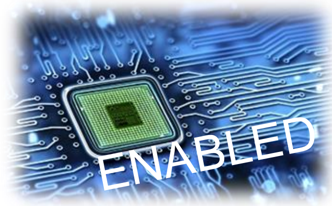


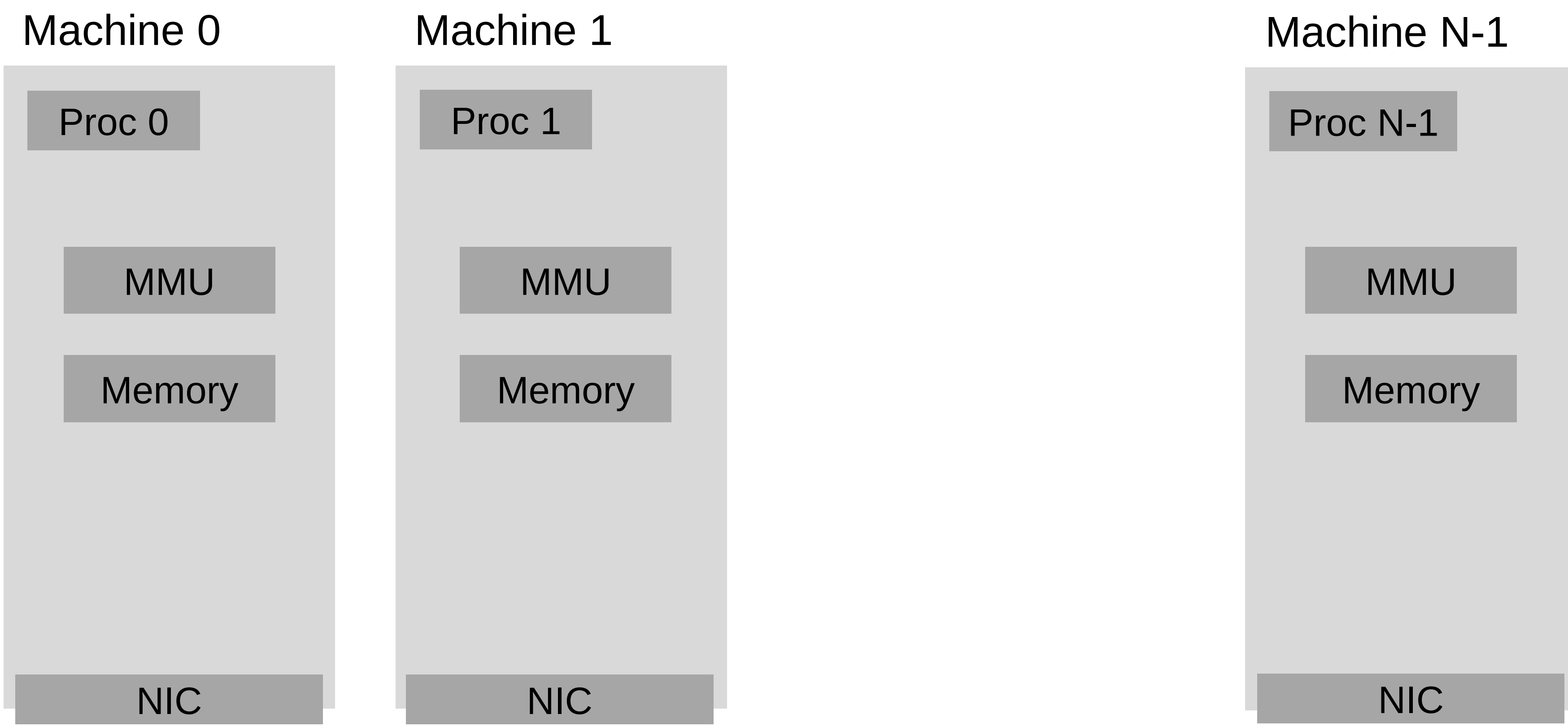

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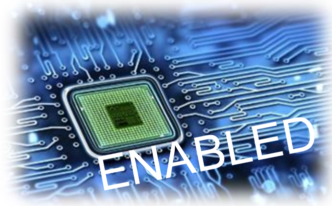


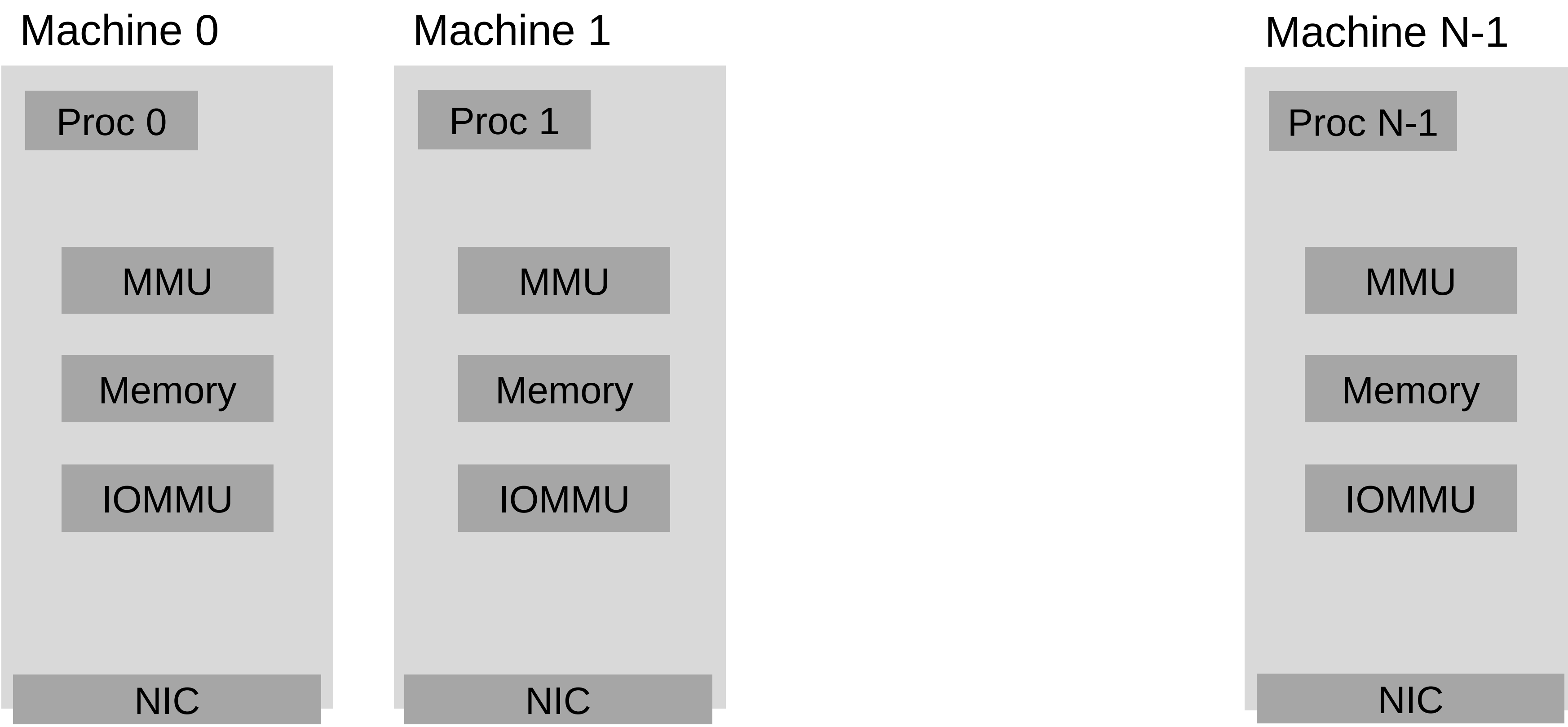

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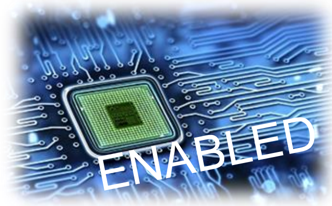


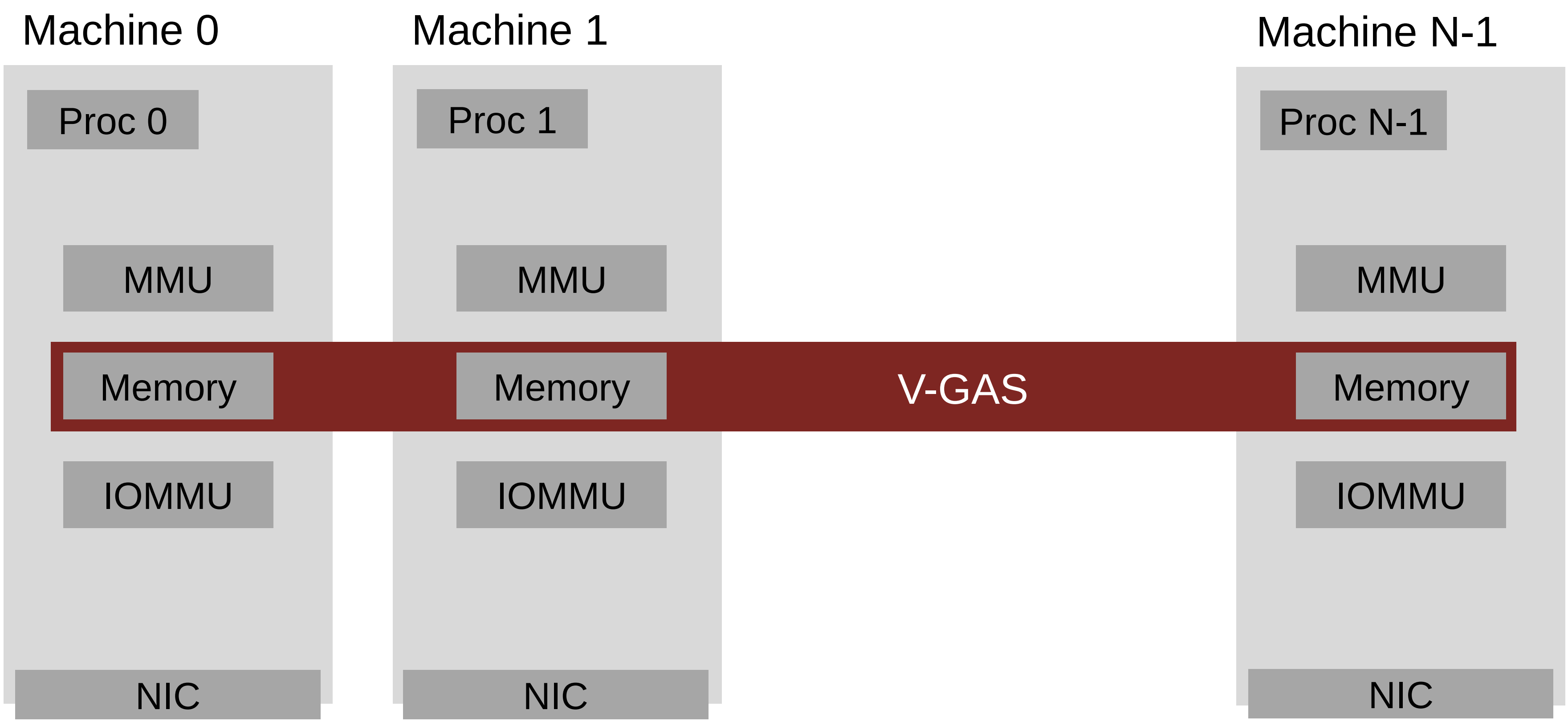

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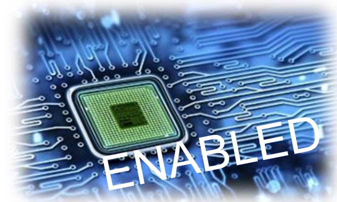


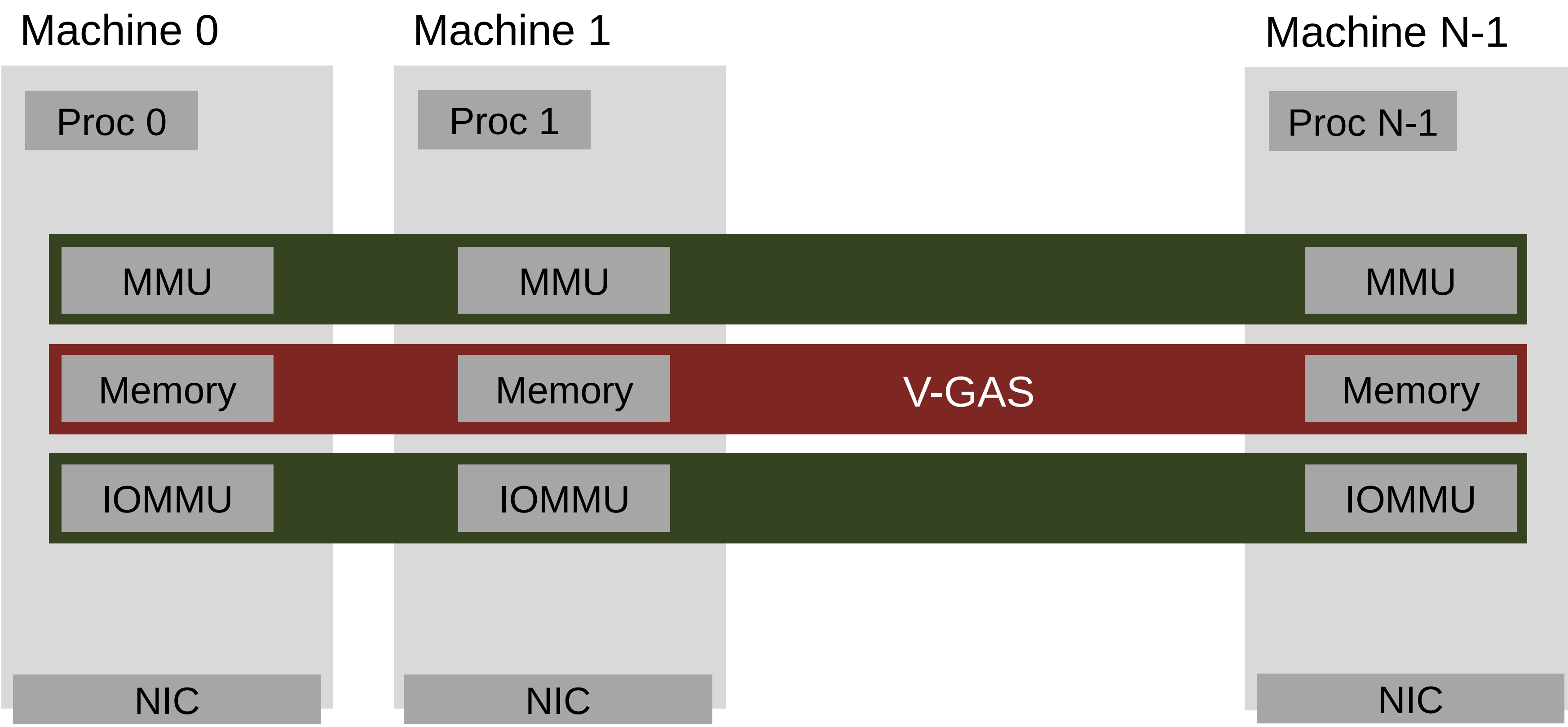

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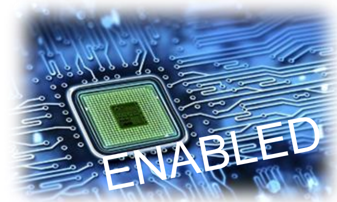


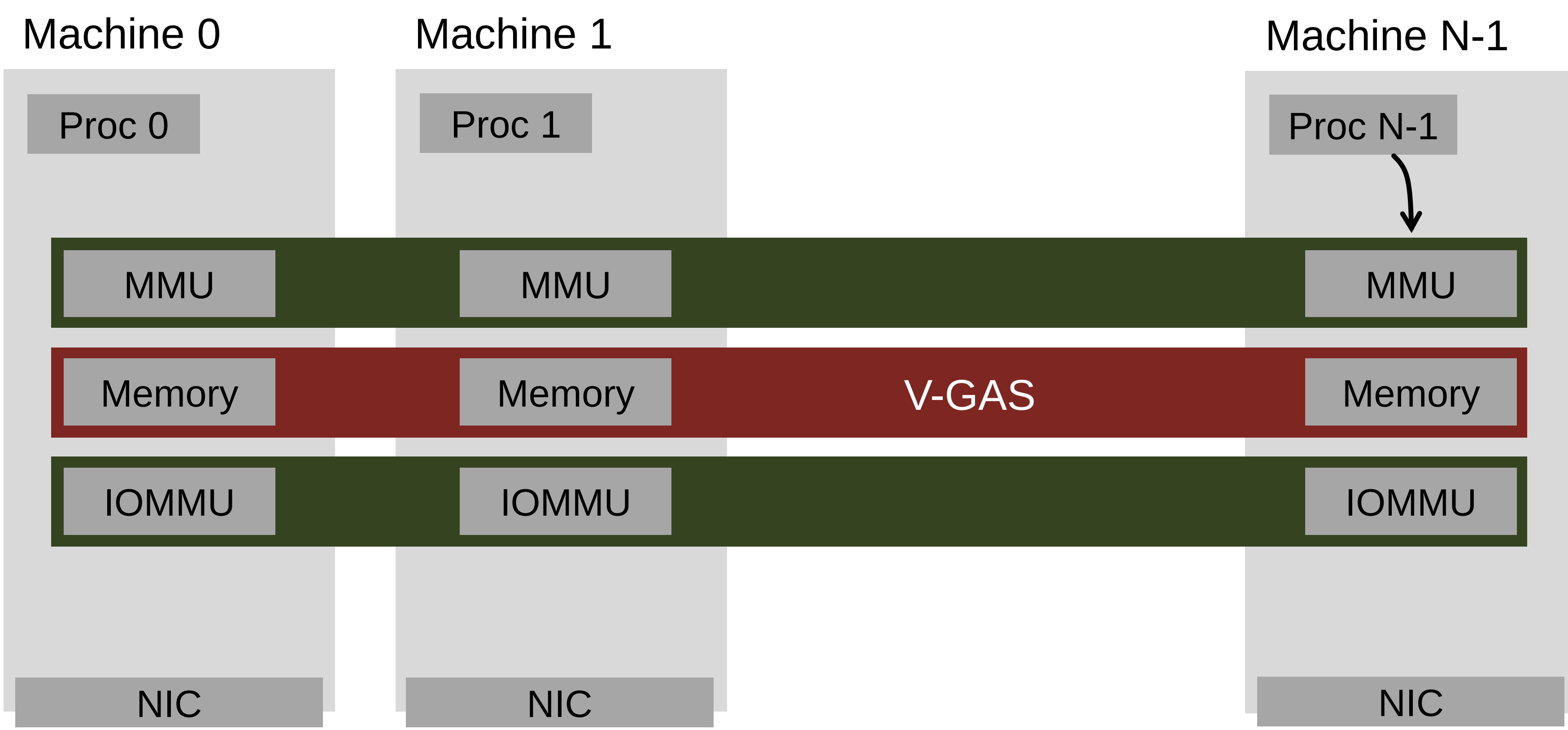

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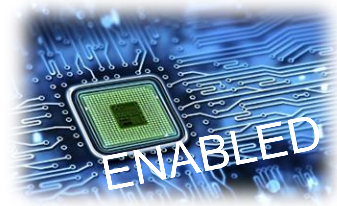


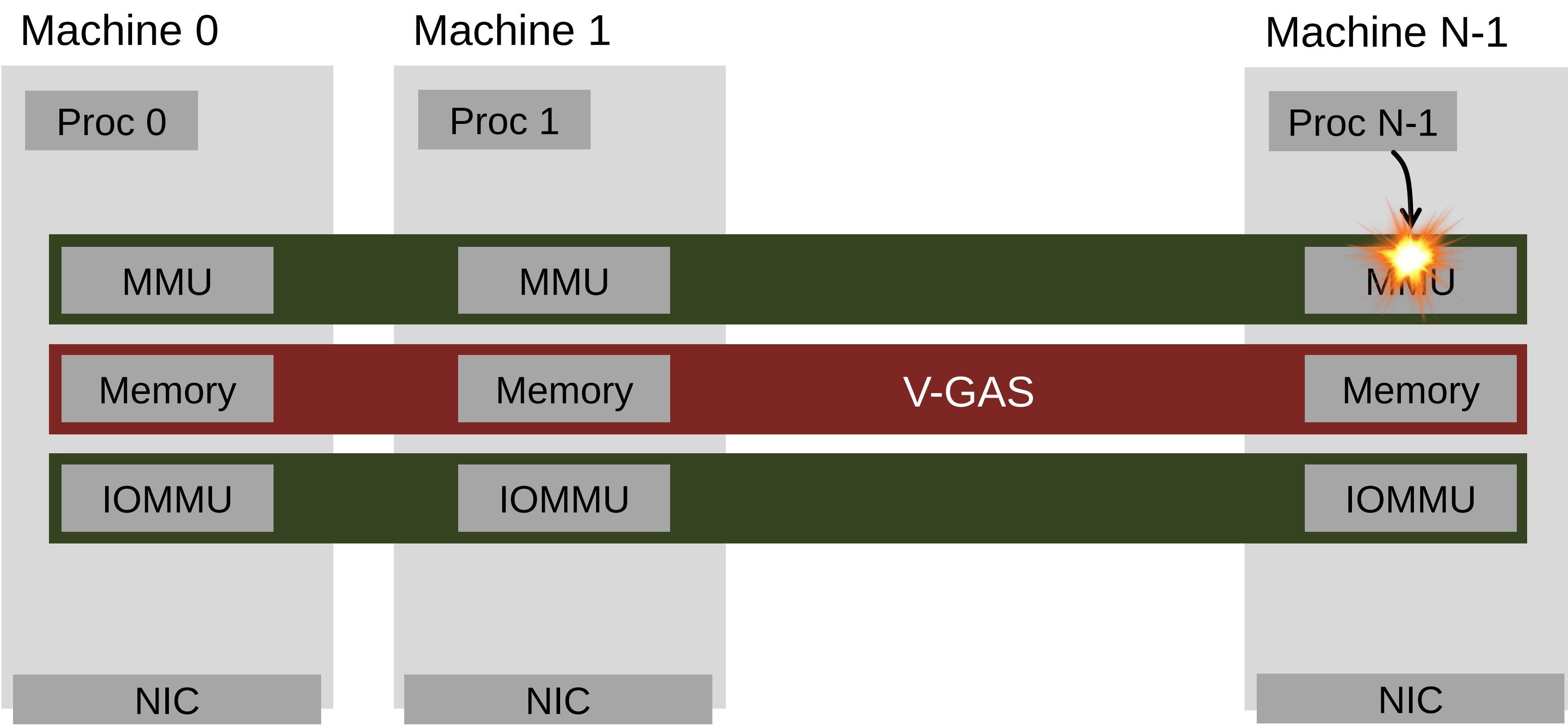

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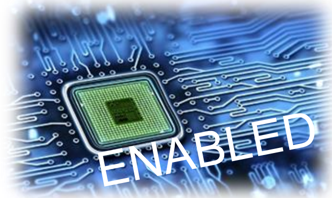


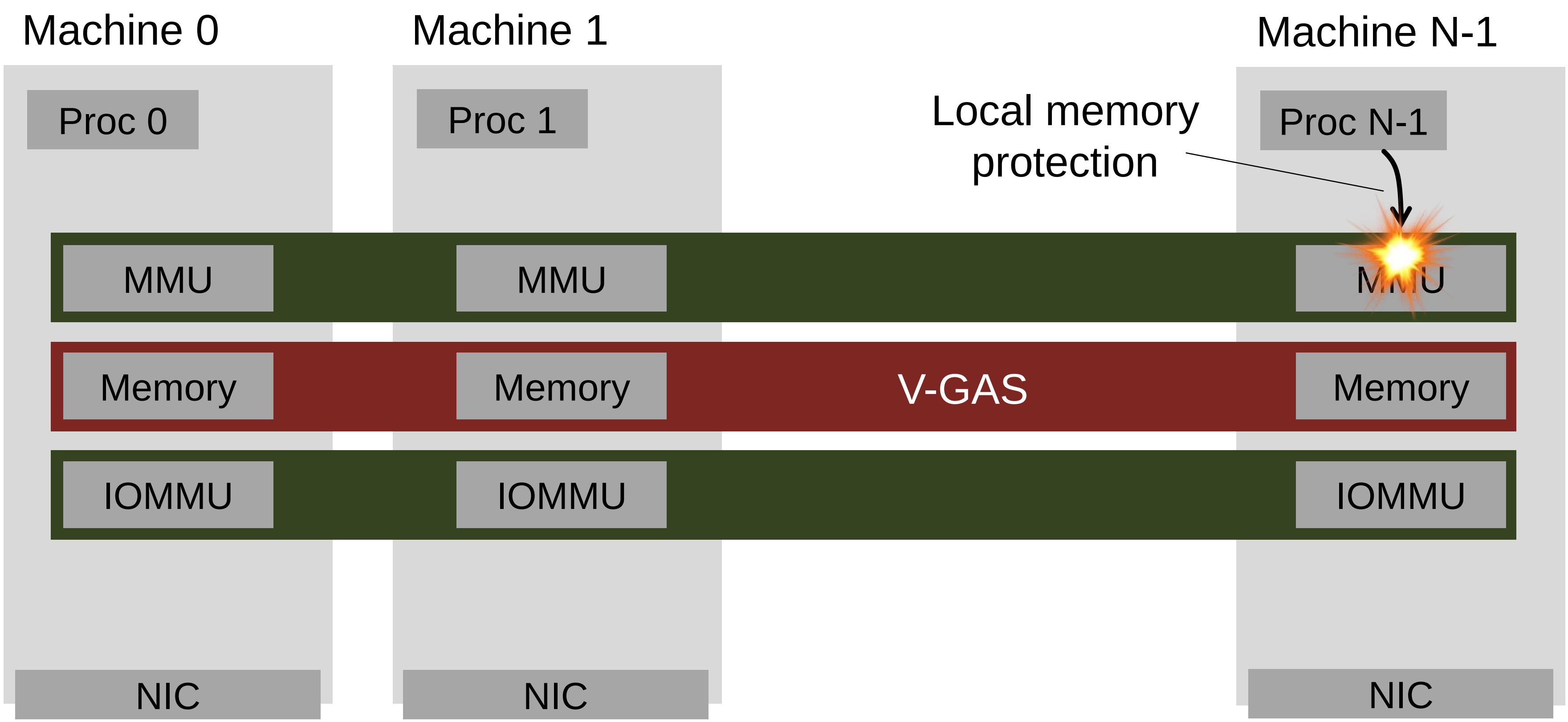

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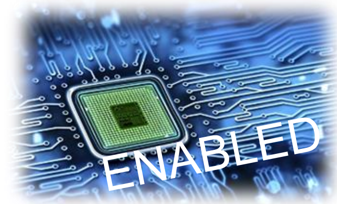


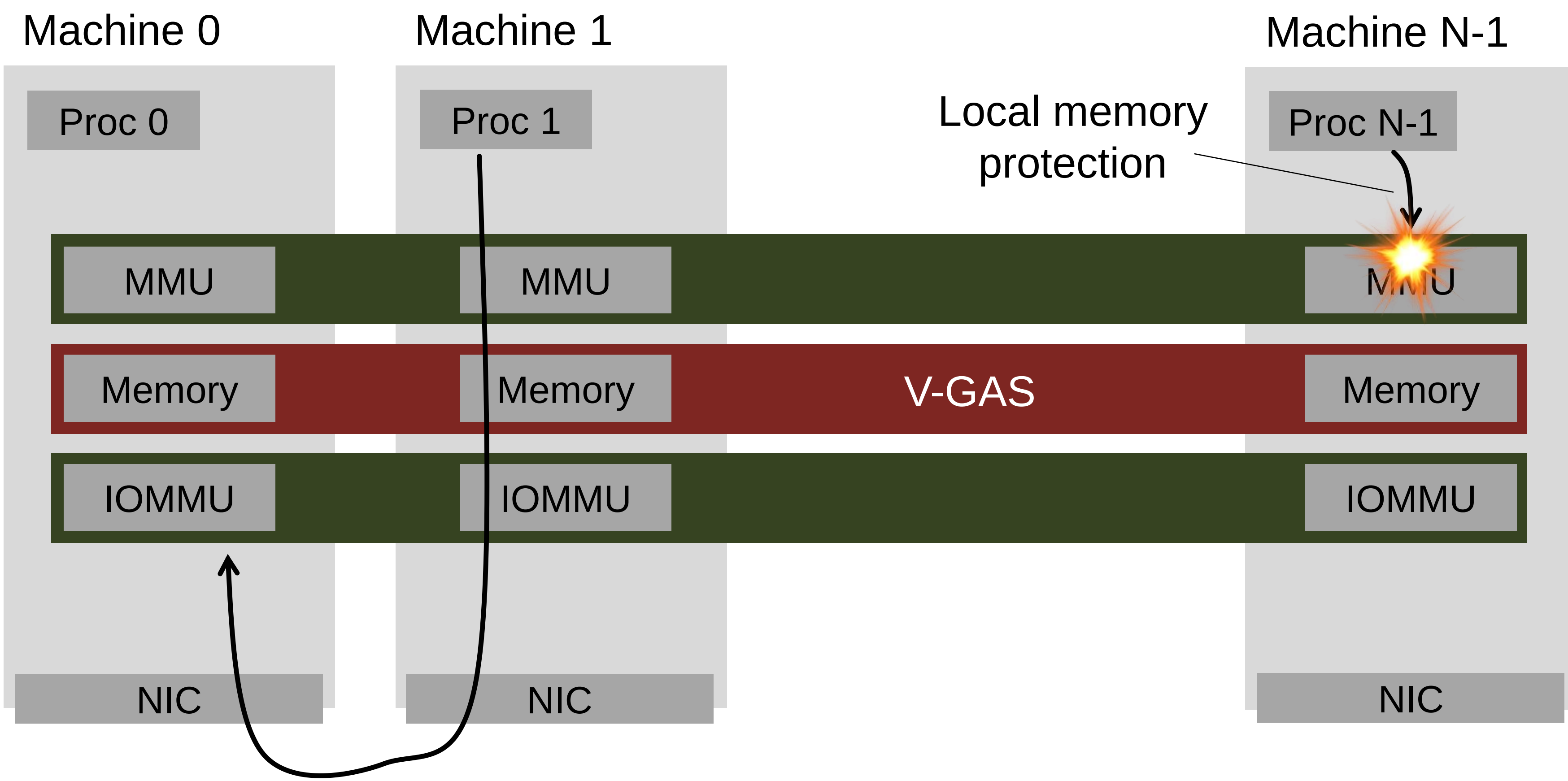

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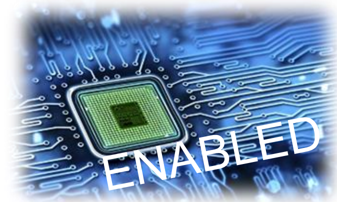


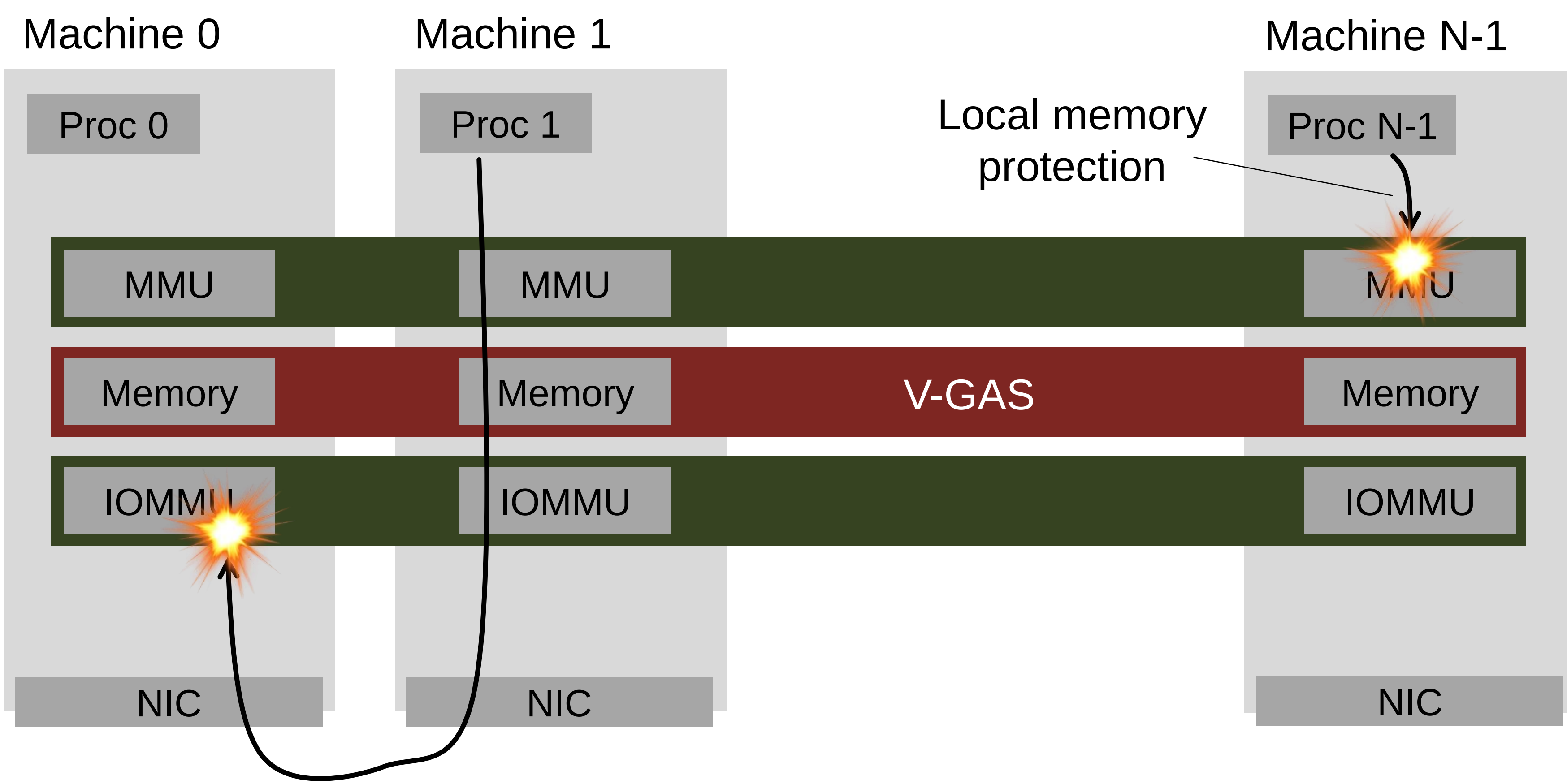

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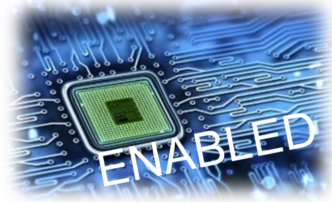


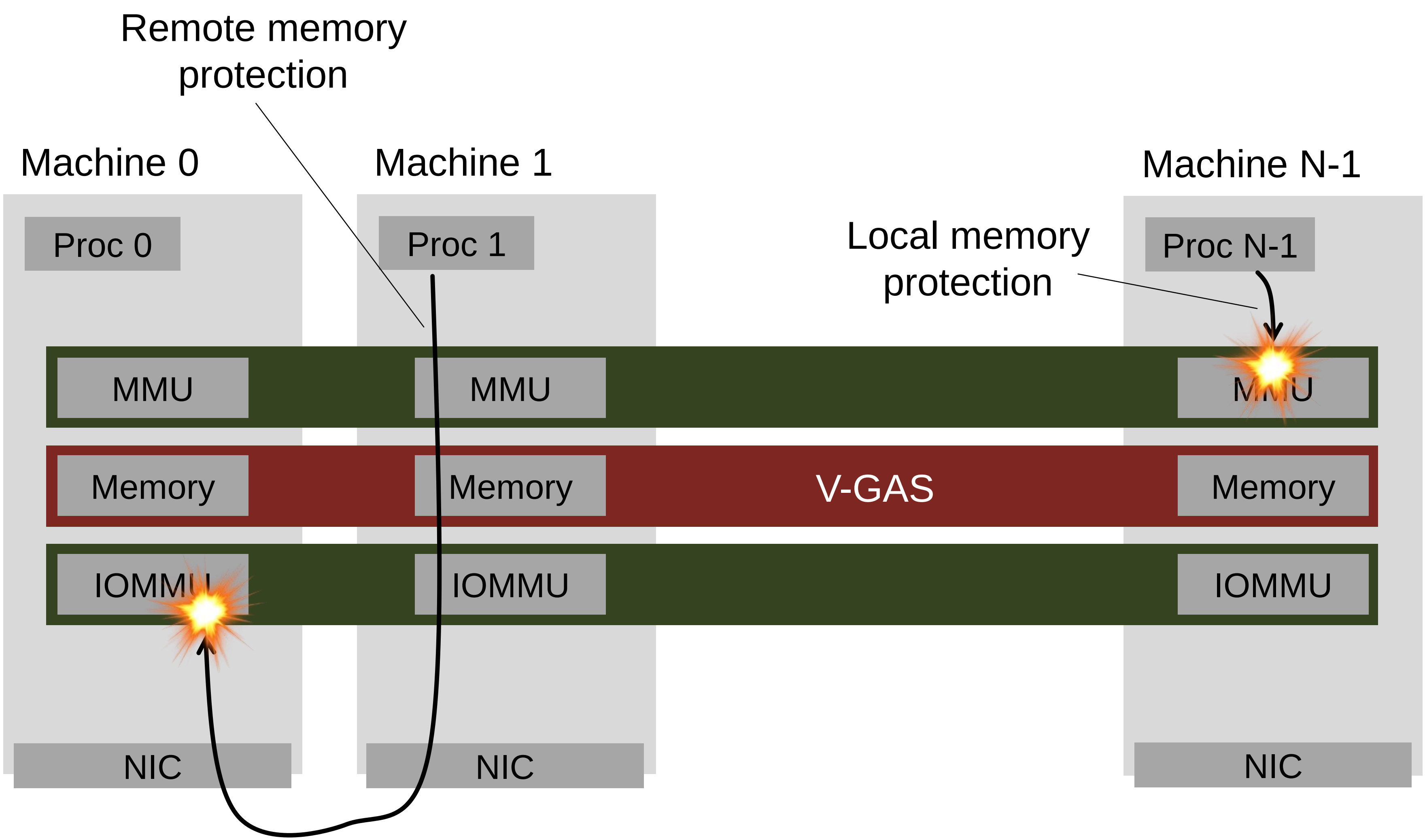

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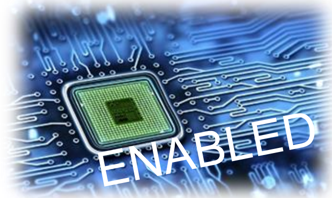


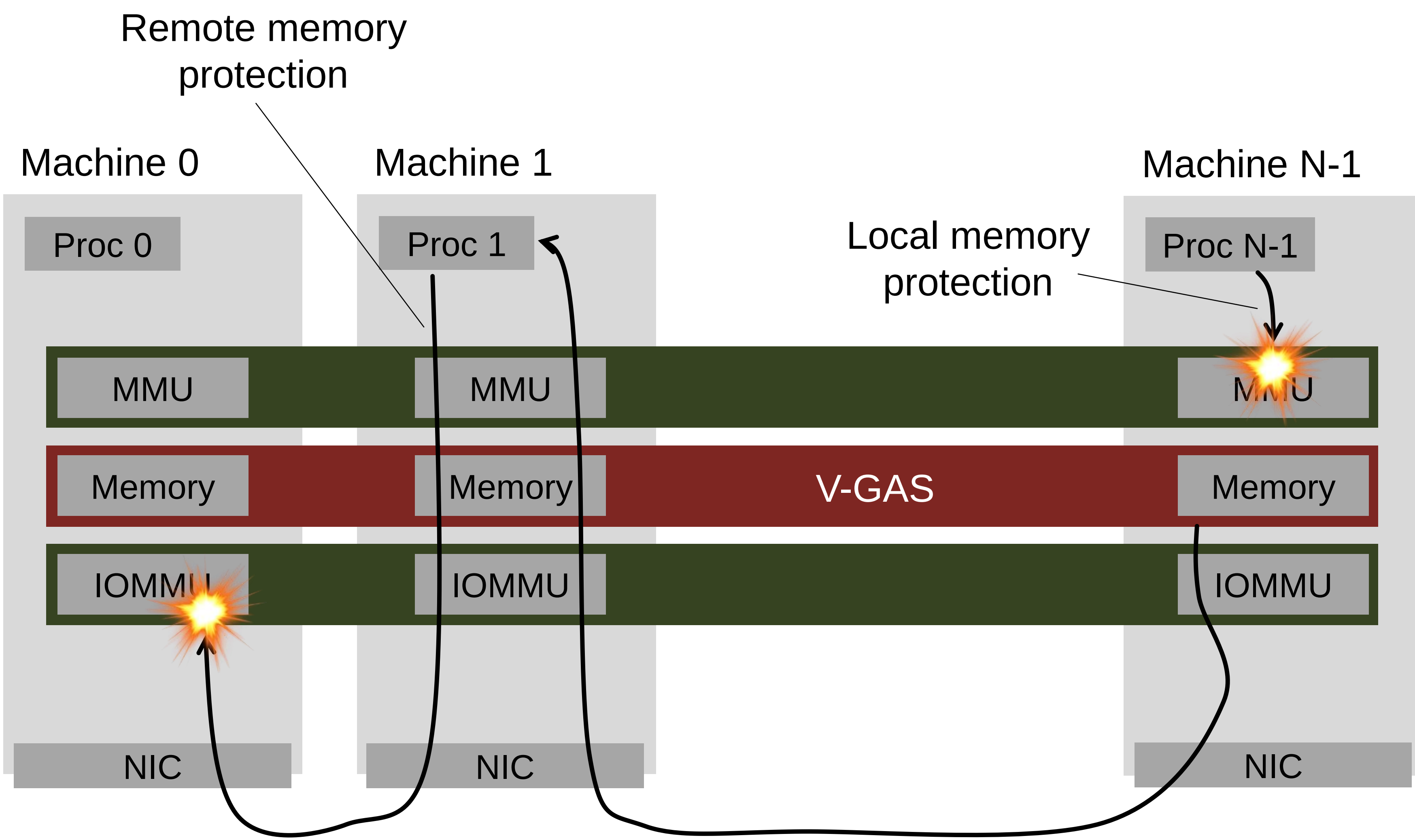

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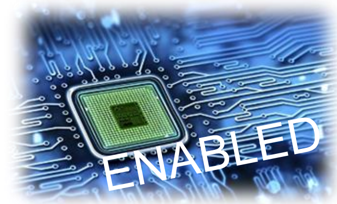
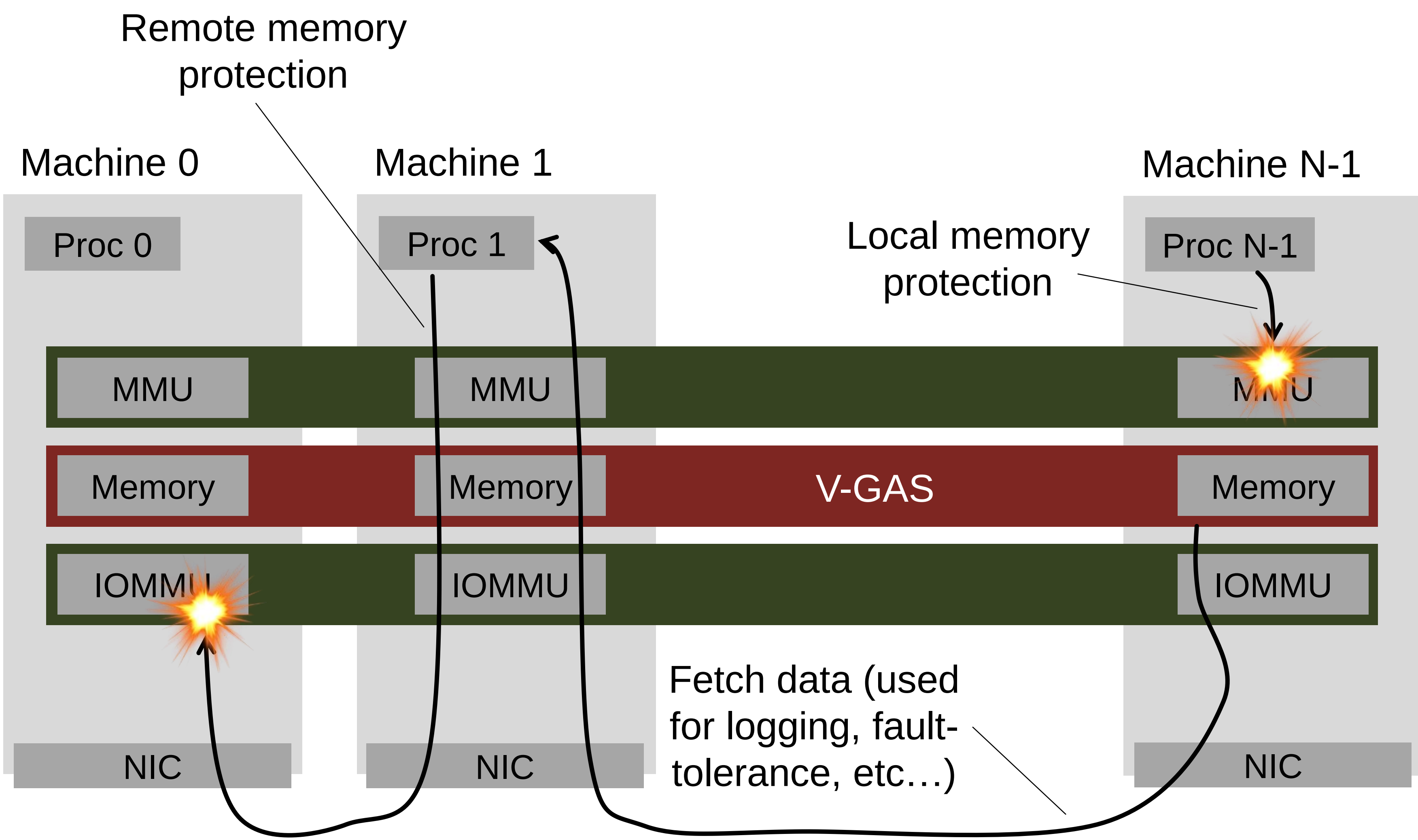
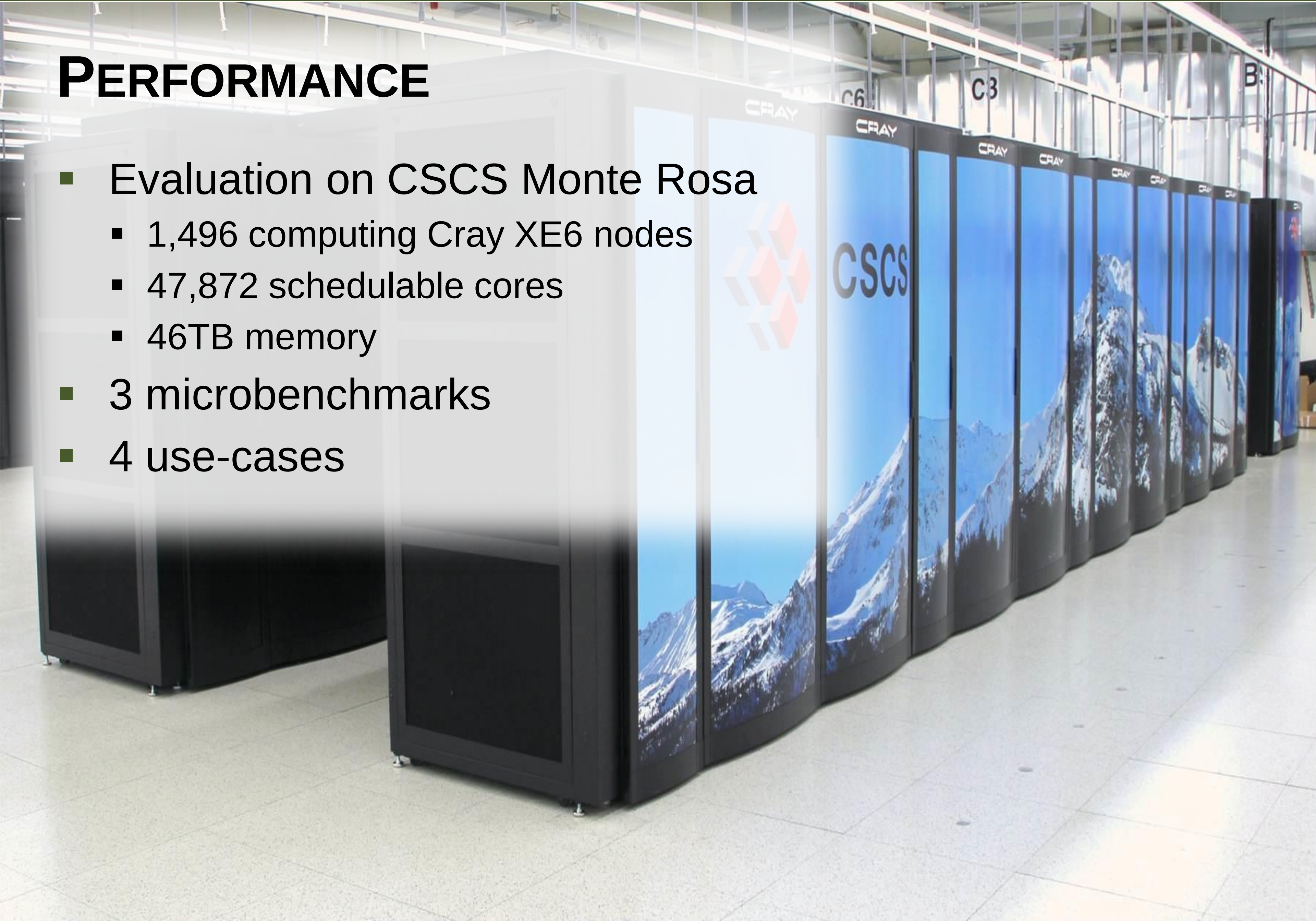


# PERFORMANCE

- Evaluation on CSCS Monte Rosa
  - 1,496 computing Cray XE6 nodes
  - 47,872 schedulable cores
  - 46TB memory
- 3 microbenchmarks
- 4 use-cases



# Performance: Microbenchmarks

## Raw Data Transfer

# PERFORMANCE: MICROBENCHMARKS
## RAW DATA TRANSFER

- Workload simulated with [1]:

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## RAW DATA TRANSFER

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# Performance: Microbenchmarks
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- Workload simulated with [1]:

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gem5

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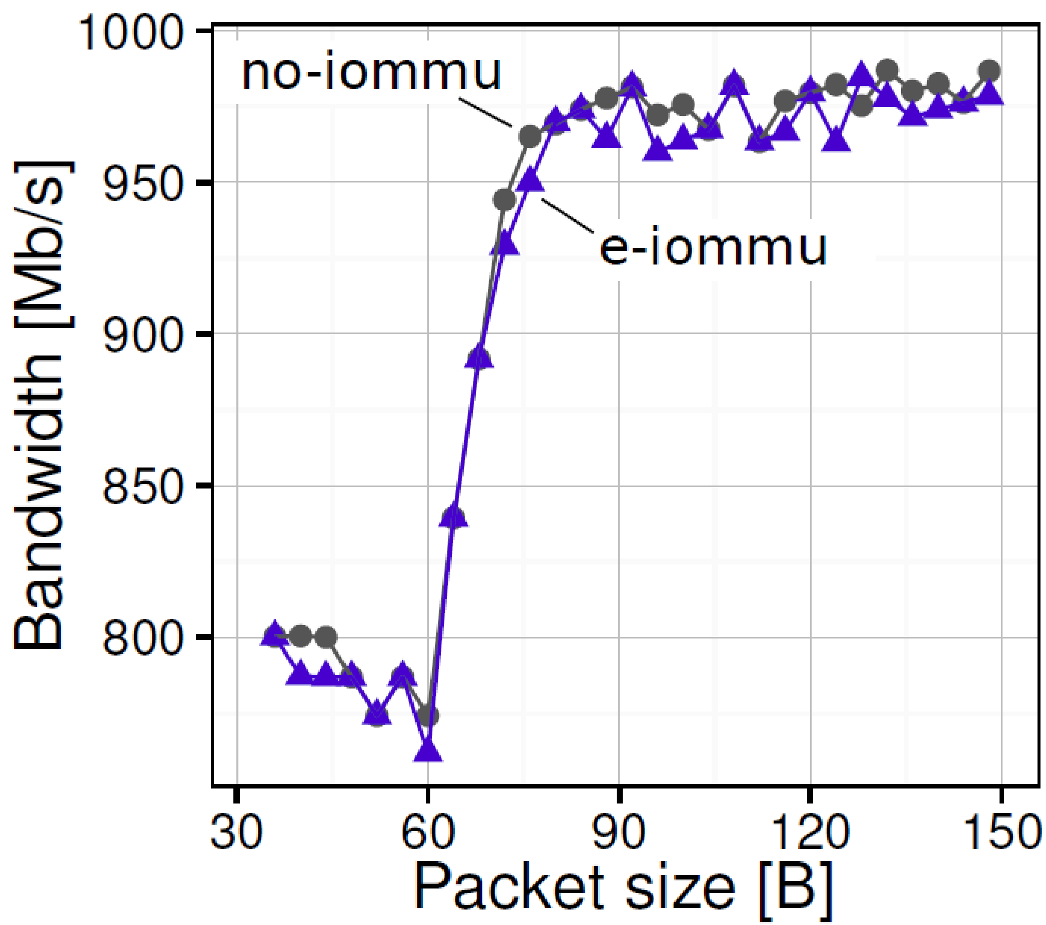


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# Performance: Large-Scale Codes

## Comparison Targets

# Performance: Large-Scale Codes

## Comparison Targets

Active Access

# Performance: Large-Scale Codes

## Comparison Targets

Active Access

AA-Int

# Performance: Large-Scale Codes

## Comparison Targets

Active Access

AA-Poll

AA-Int

# Performance: Large-Scale Codes
## Comparison Targets

Active Access

AA-Poll

AA-Int

AA-SP

# Performance: Large-Scale Codes

## Comparison Targets

Active Access

AA-Poll

AA-Int

AA-SP

RMA

# Performance: Large-Scale Codes

## Comparison Targets

Active Access

AA-Poll

AA-Int

AA-SP

RMA

CRAY

DMAPP

# Performance: Large-Scale Codes

## Comparison Targets

Active Access

AA-Poll

AA-Int

AA-SP

RMA

CRAY

DMAPP

InfiniBand

# Performance: Large-Scale Codes

## Comparison Targets

Active Access

AA-Poll

AA-Int

AA-SP

RMA

IBM Cell

CRAY DMAPP

InfiniBand

# Performance: Large-Scale Codes

## Comparison Targets

Active Access

AA-Poll

AA-Int

AA-SP

RMA

IBM Cell

CRAY DMAPP

InfiniBand

Mellanox Technologies RoCE

# Performance: Large-Scale Codes

## Comparison Targets

Active Access

AA-Poll

AA-Int

AA-SP

RMA

IBM Cell

CRAY DMAPP

InfiniBand

Mellanox Technologies RoCE

Active Messages

# Performance: Large-Scale Codes

## Comparison Targets

Active Access

AA-Poll

AA-Int

AA-SP

Active Messages

AM

RMA

IBM

Cell

CRAY

DMAPP

InfiniBand

Mellanox Technologies

RoCE

# Performance: Large-Scale Codes

## Comparison Targets

Active Access

AA-Poll

AA-Int

AA-SP

RMA

IBM Cell

Cray DMAPP

InfiniBand

Mellanox Technologies RoCE

Active Messages

AM

AM-Exp

# Performance: Large-Scale Codes

## Comparison Targets

Active Access

AA-Poll

AA-Int

AA-SP

RMA

IBM Cell

CRAY DMAPP

InfiniBand

Mellanox Technologies RoCE

Active Messages

AM AM-Onload

AM-Exp

# Performance: Large-Scale Codes

## Comparison Targets

Active Access

AA-Poll

AA-Int

AA-SP

Active Messages

AM AM-Onload

AM-Exp AM-Ints

RMA

Cell

DMAPP

RoCE

# Performance: Large-Scale Codes
## Comparison Targets

Active Access

AA-Poll
AA-Int
AA-SP

Active Messages

AM AM-Onload
AM-Exp AM-Ints

IBM
DCMF LAPI
PAMI

RMA

IBM
Cell

CRAY
DMAPP

InfiniBand

Mellanox Technologies
RoCE

# Performance: Large-Scale Codes

## Comparison Targets

Active Access

AA-Poll

AA-Int

AA-SP

Active Messages

AM AM-Onload

AM-Exp AM-Ints

IBM DCMF LAPI PAMI

Myricom MX

RMA

IBM Cell

Cray DMAPP

InfiniBand

Mellanox Technologies RoCE

# Performance: Large-Scale Codes

## Comparison Targets

**Active Access**

AA-Poll

AA-Int

AA-SP

**Active Messages**

AM

AM-Onload

AM-Exp

AM-Ints

DCMF

LAPI

PAMI

MX

AM++

GASNet

**RMA**

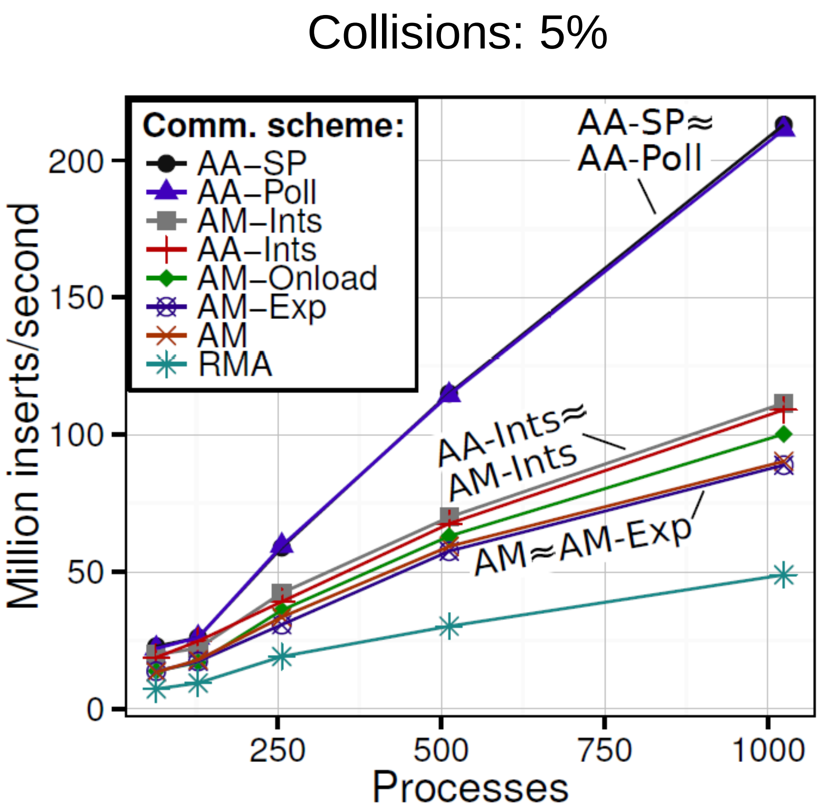
DMAPP

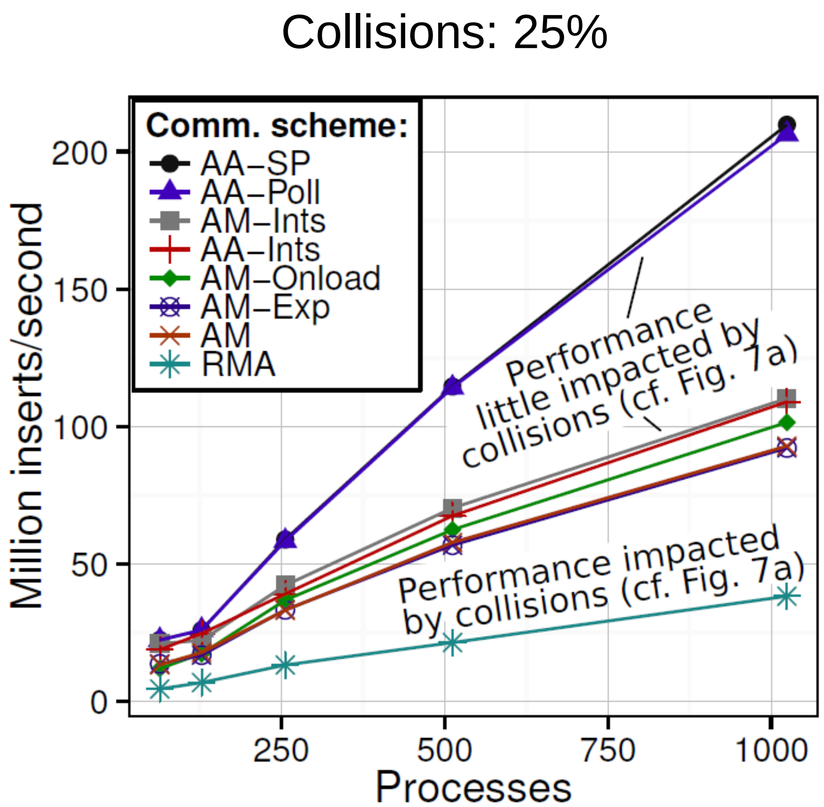
Cell

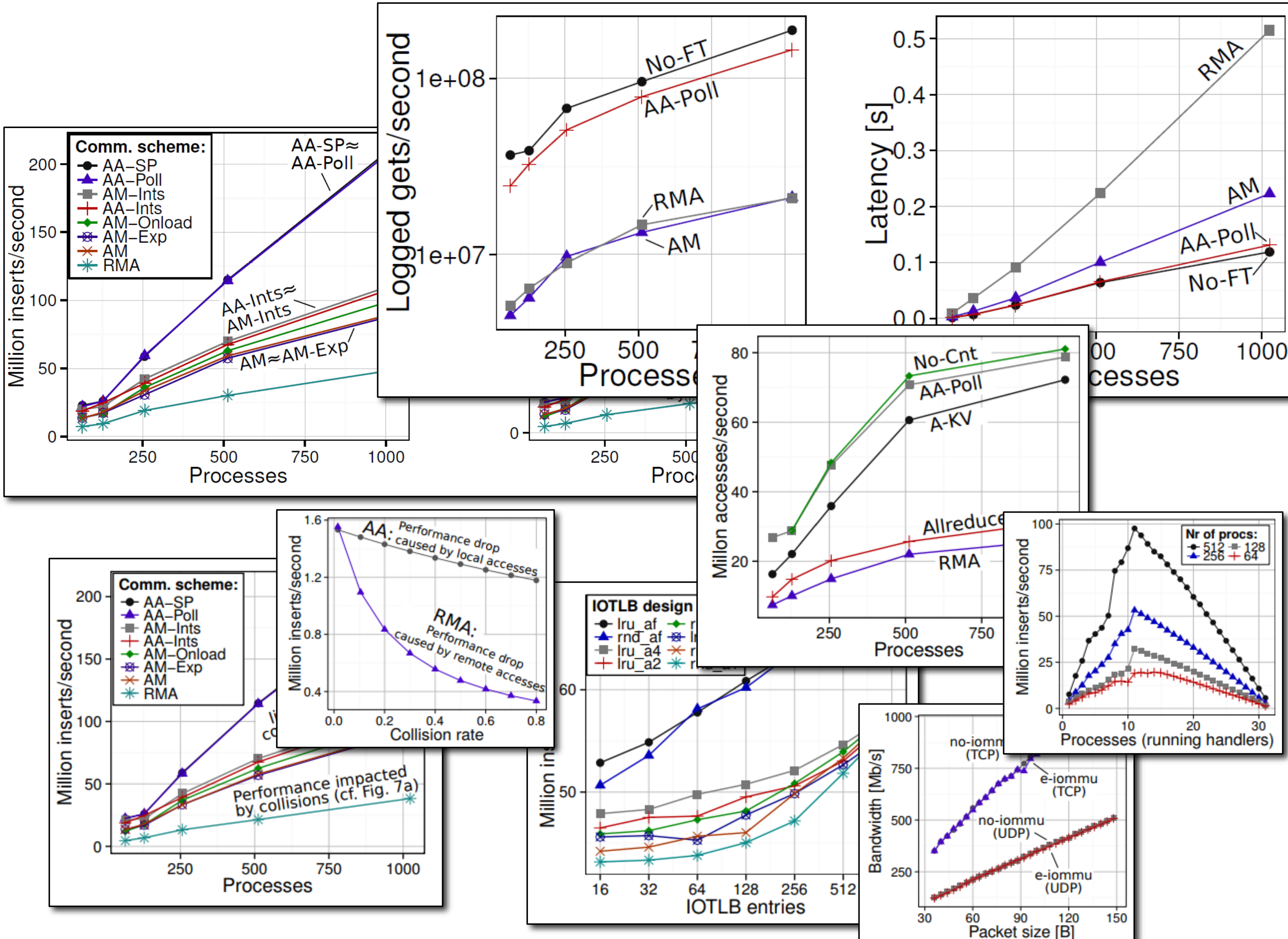
RoCE

# Performance: Large-Scale Codes

## Distributed Hashtable



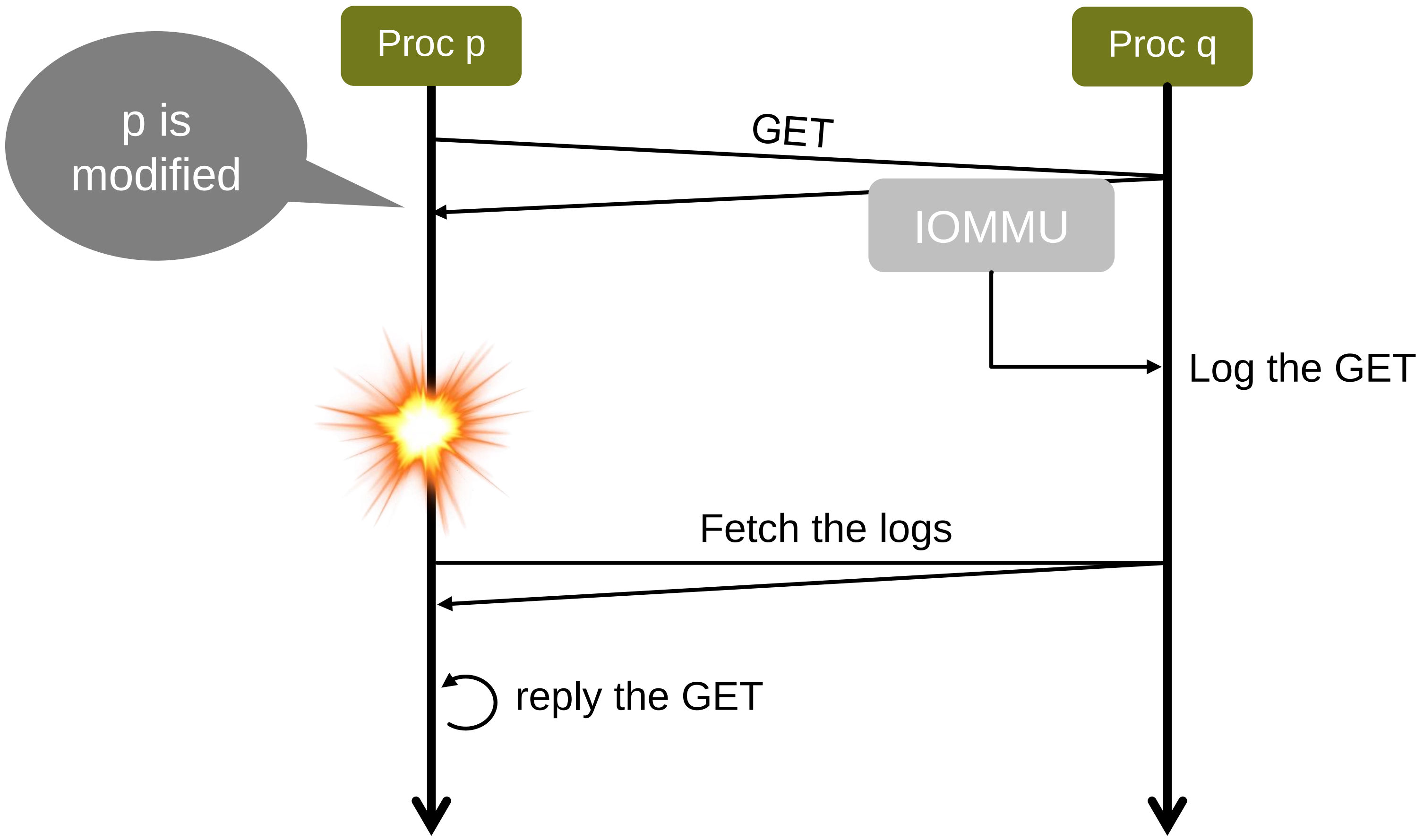




Comm. scheme:
AA–SP
AA–Poll
AM–Ints
AA–Ints
AM–Onload
AM–Exp
AM
RMA
AA-SP≈
AA-Poll
AA-Ints≈
AM-Ints
AM≈AM-Exp
Million inserts/second
Processes
Logged gets/second
No-FT
AA-Poll
RMA
AM
Latency [s]
Million accesses/second
No-Cnt
A-KV
Allreduce
AA: Performance drop caused by local accesses
RMA: Performance drop caused by remote accesses
Collision rate
Performance impacted by collisions (cf. Fig. 7a)
IOTLB design
lru_af
rnd_af
lru_a4
lru_a2
IOTLB entries
Nr of procs:
Processes (running handlers)
Bandwidth [Mb/s]
no-iommu (TCP)
e-iommu (TCP)
no-iommu (UDP)
e-iommu (UDP)
Packet size [B]

# ACTIVE ACCESS USE-CASES

## ACCELERATING LOGGING FOR RMA

- Logging gets (AA):



# CONCLUSIONS

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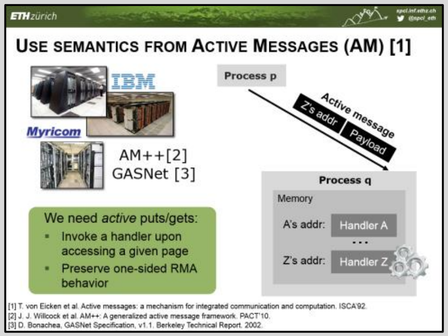
## Active Access

# CONCLUSIONS

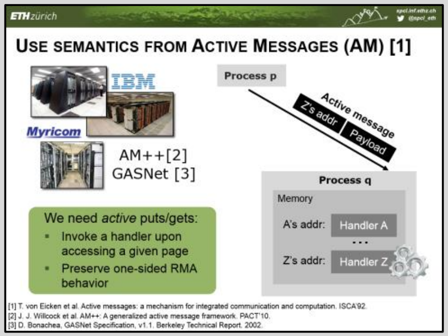
## Active Access




Alleviates RMA's problems with AMs
while preserving one-sided semantics

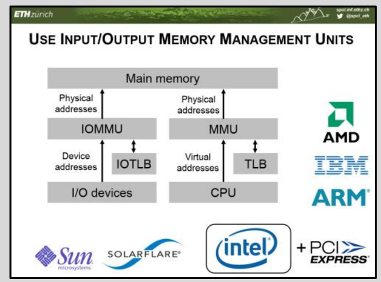
# Conclusions

## Active Access



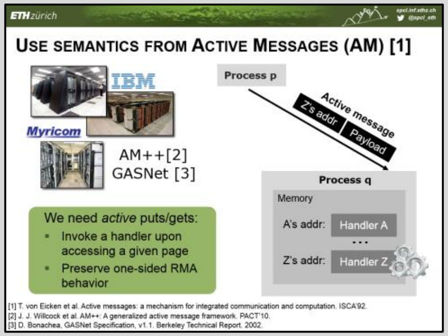

Alleviates RMA's problems with AMs while preserving one-sided semantics

Uses commodity & common IOMMUs



# Conclusions

## Active Access

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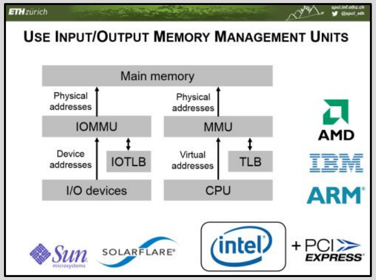
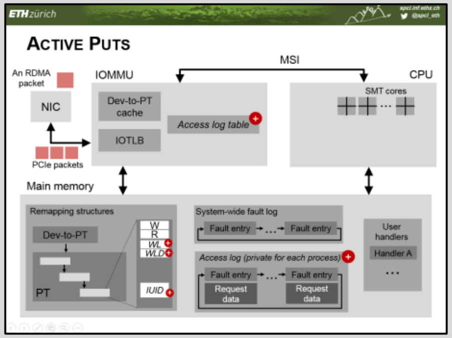
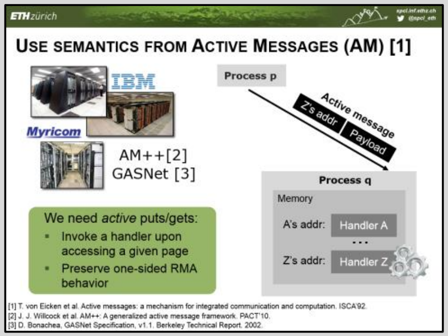



Extends paging capabilities in a distributed environment

# Conclusions

## Active Access

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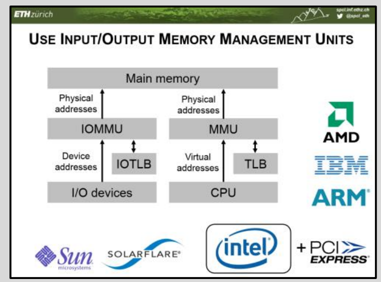
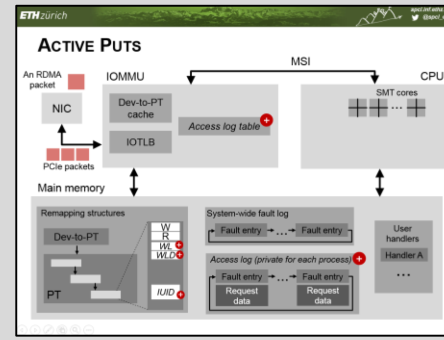


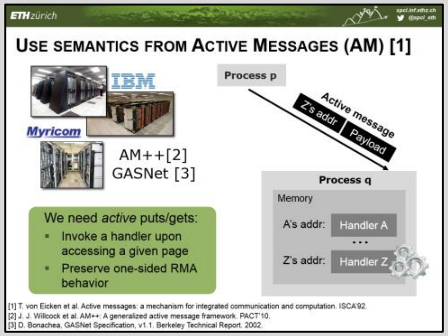




Extends paging capabilities in a distributed environment

## Data-centric programming

# Conclusions

## Active Access

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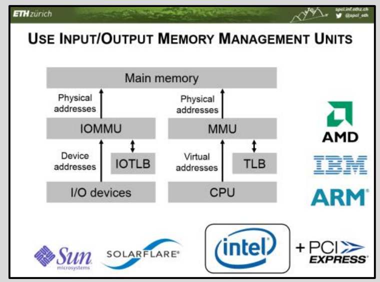


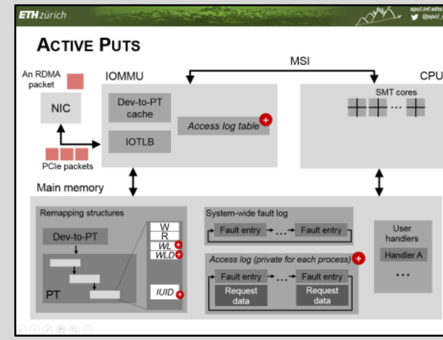


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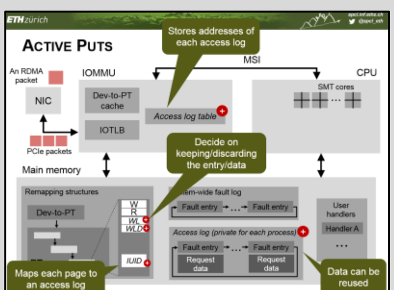


Addresses of pages guide the execution of handlers

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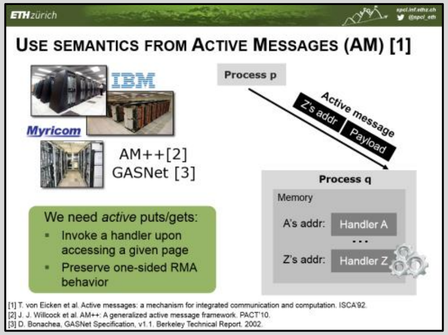


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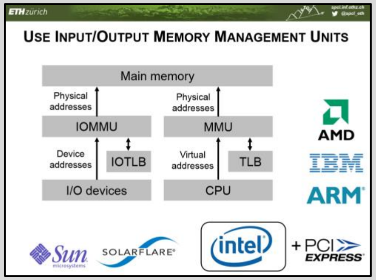


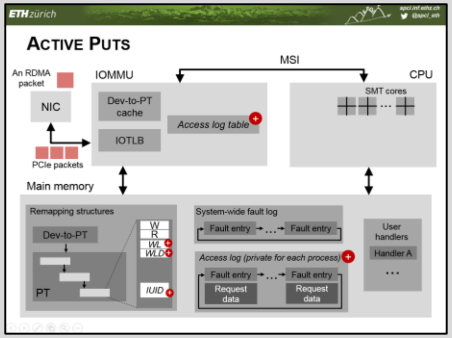


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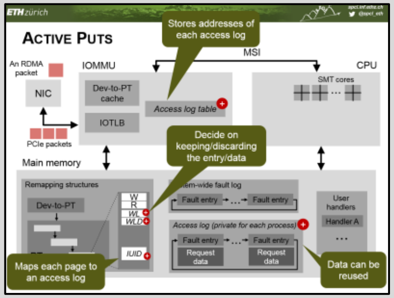


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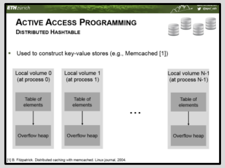


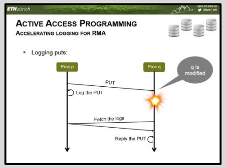


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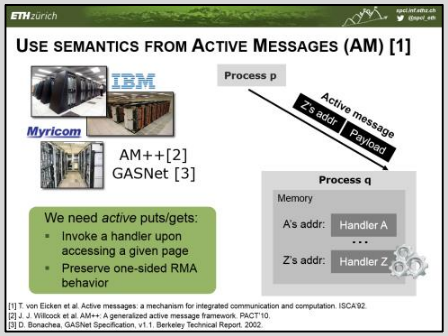


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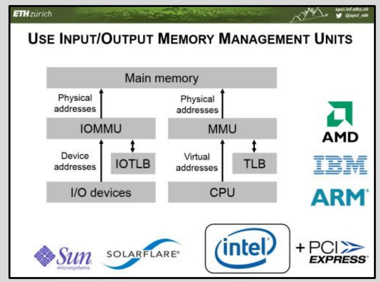


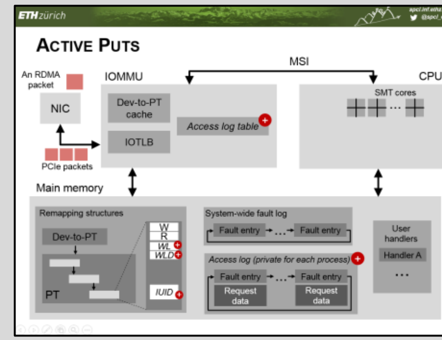


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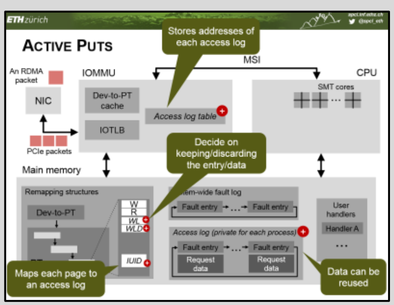


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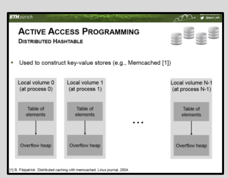


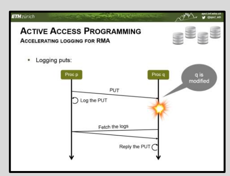


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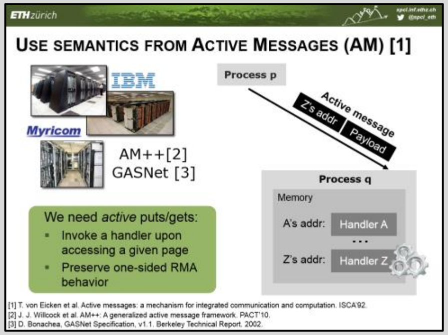


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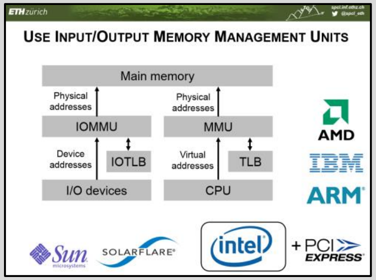


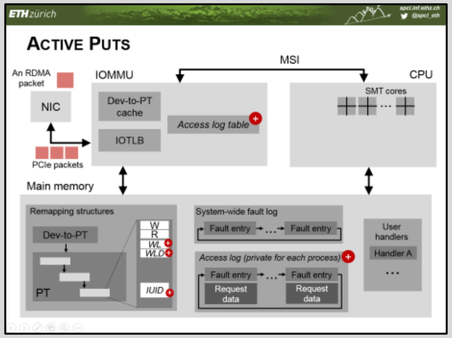


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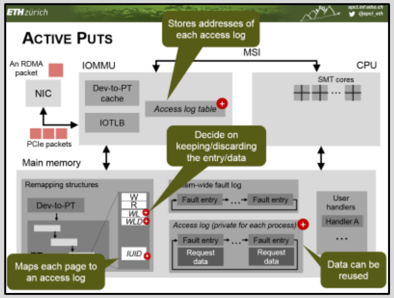


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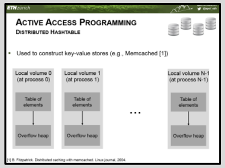


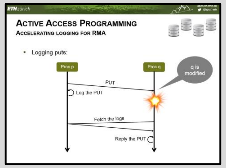


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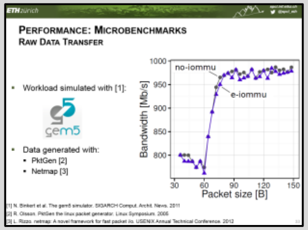
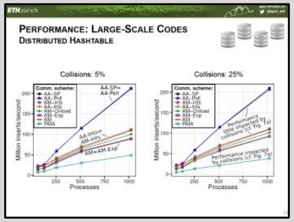
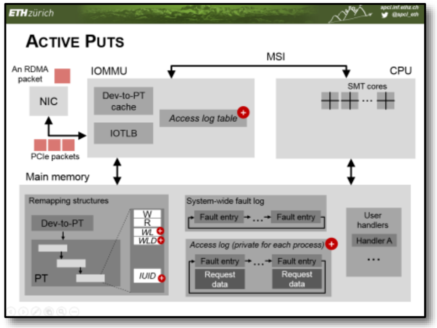
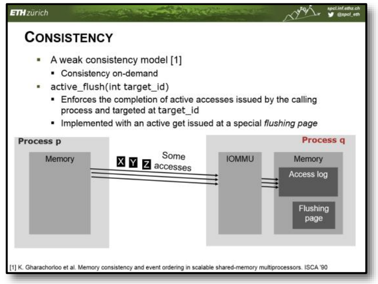
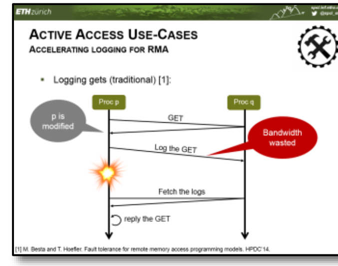


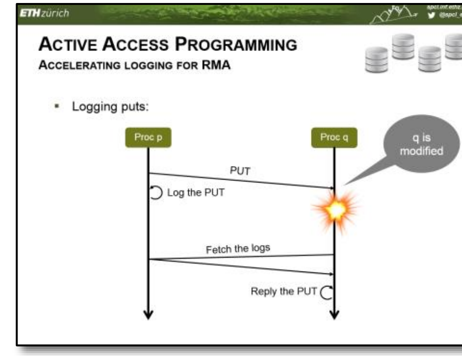



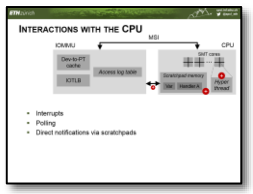

Accelerates various distributed codes

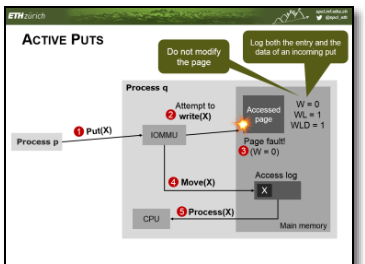


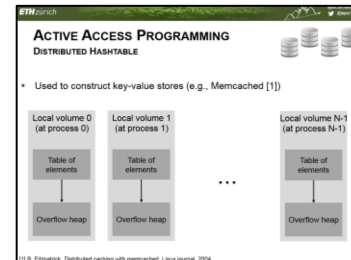



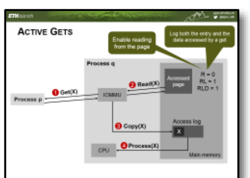



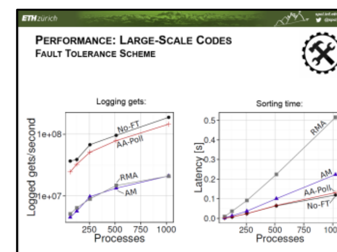



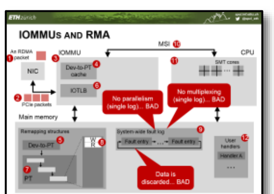




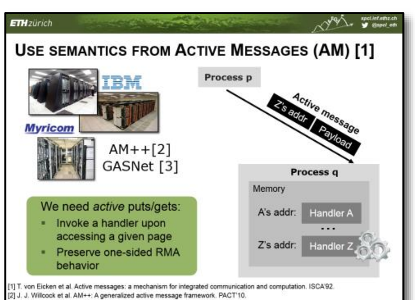

# Thank you for your attention

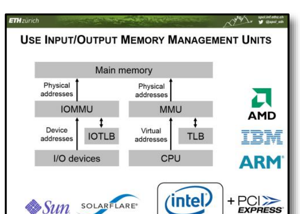


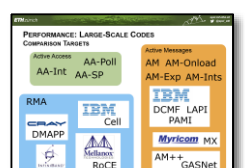



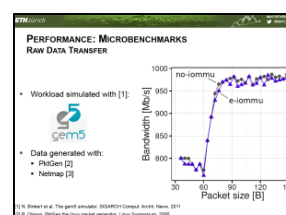



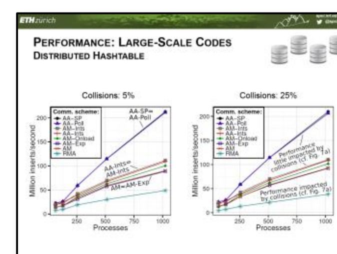




# Active Access Use-Cases

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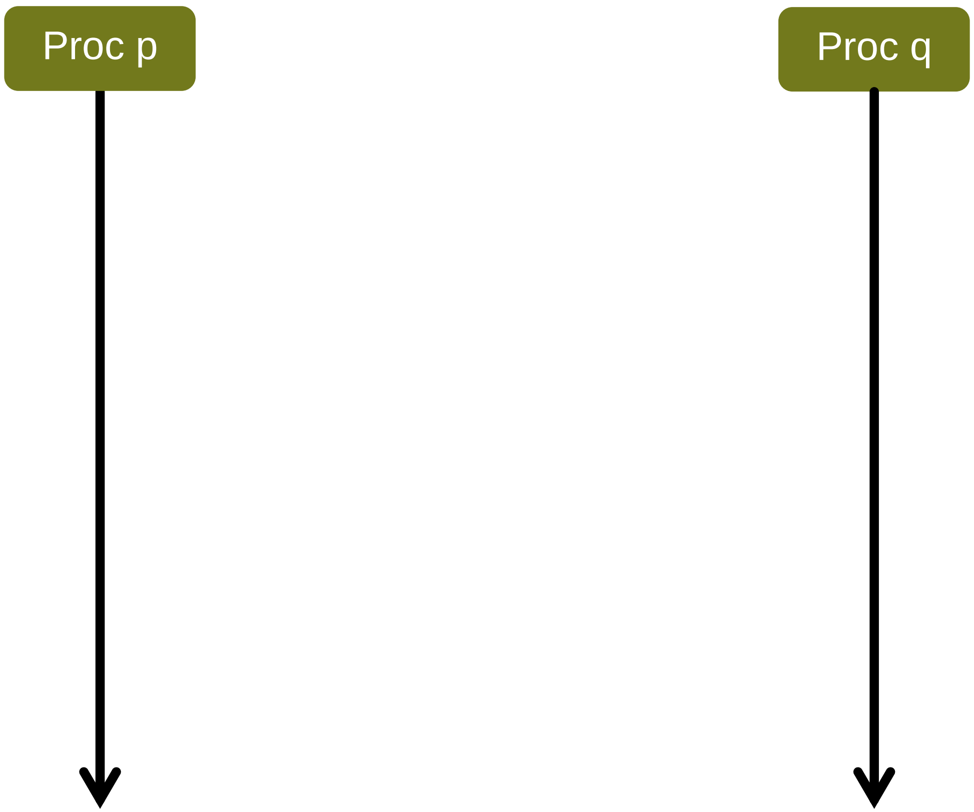

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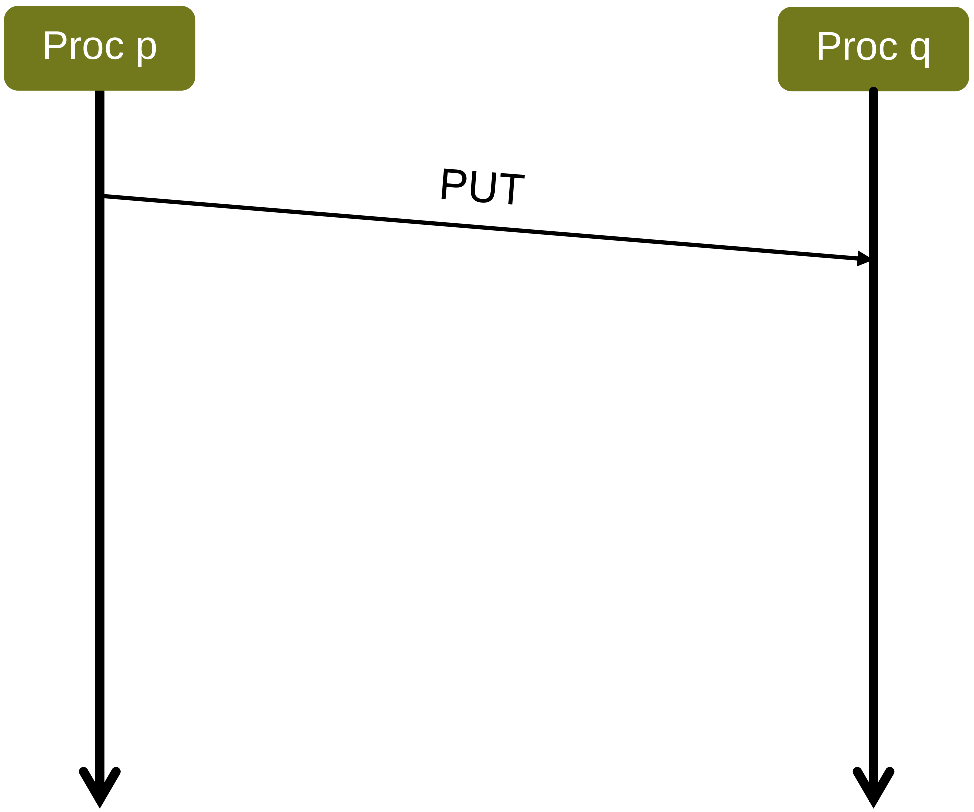

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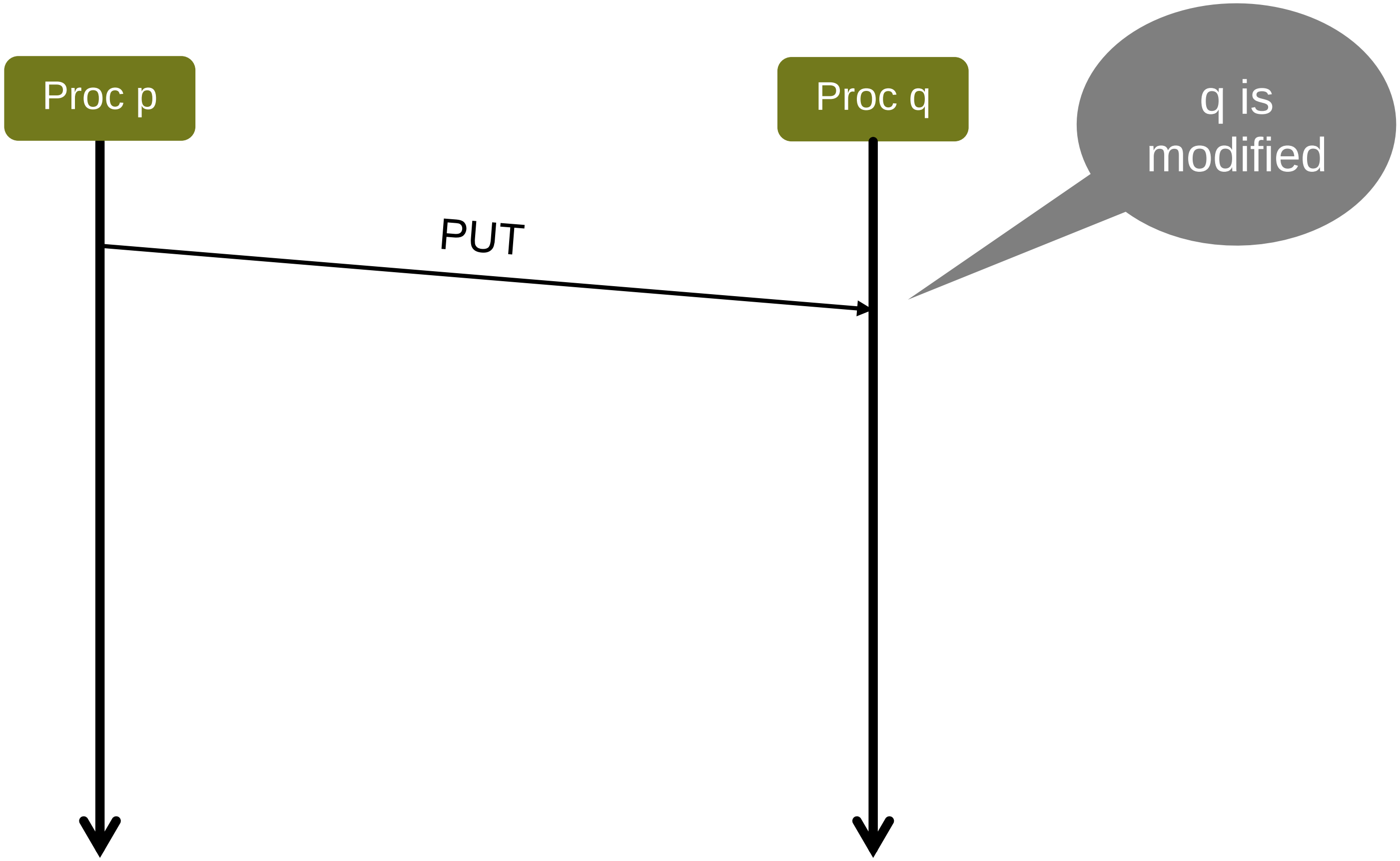

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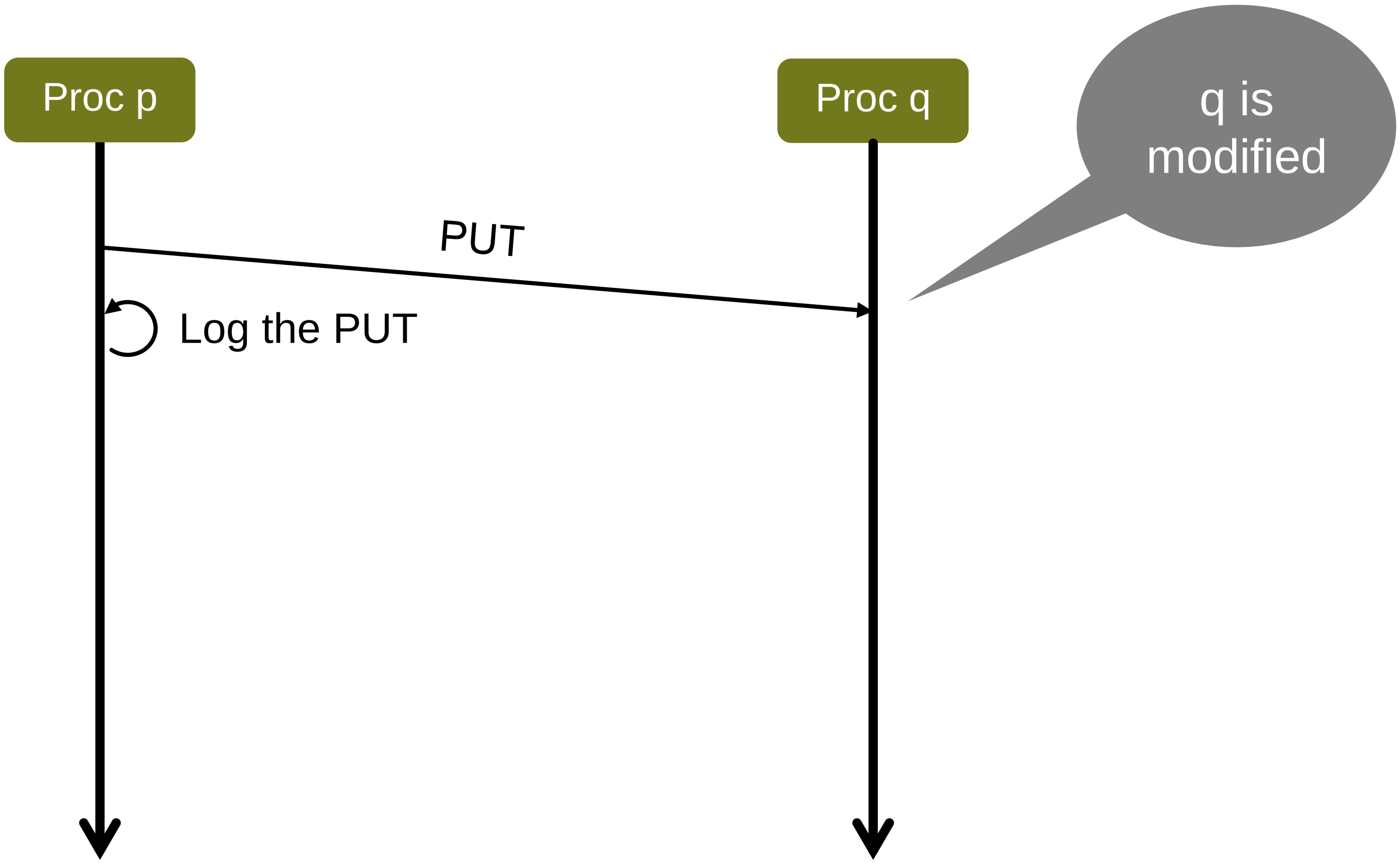

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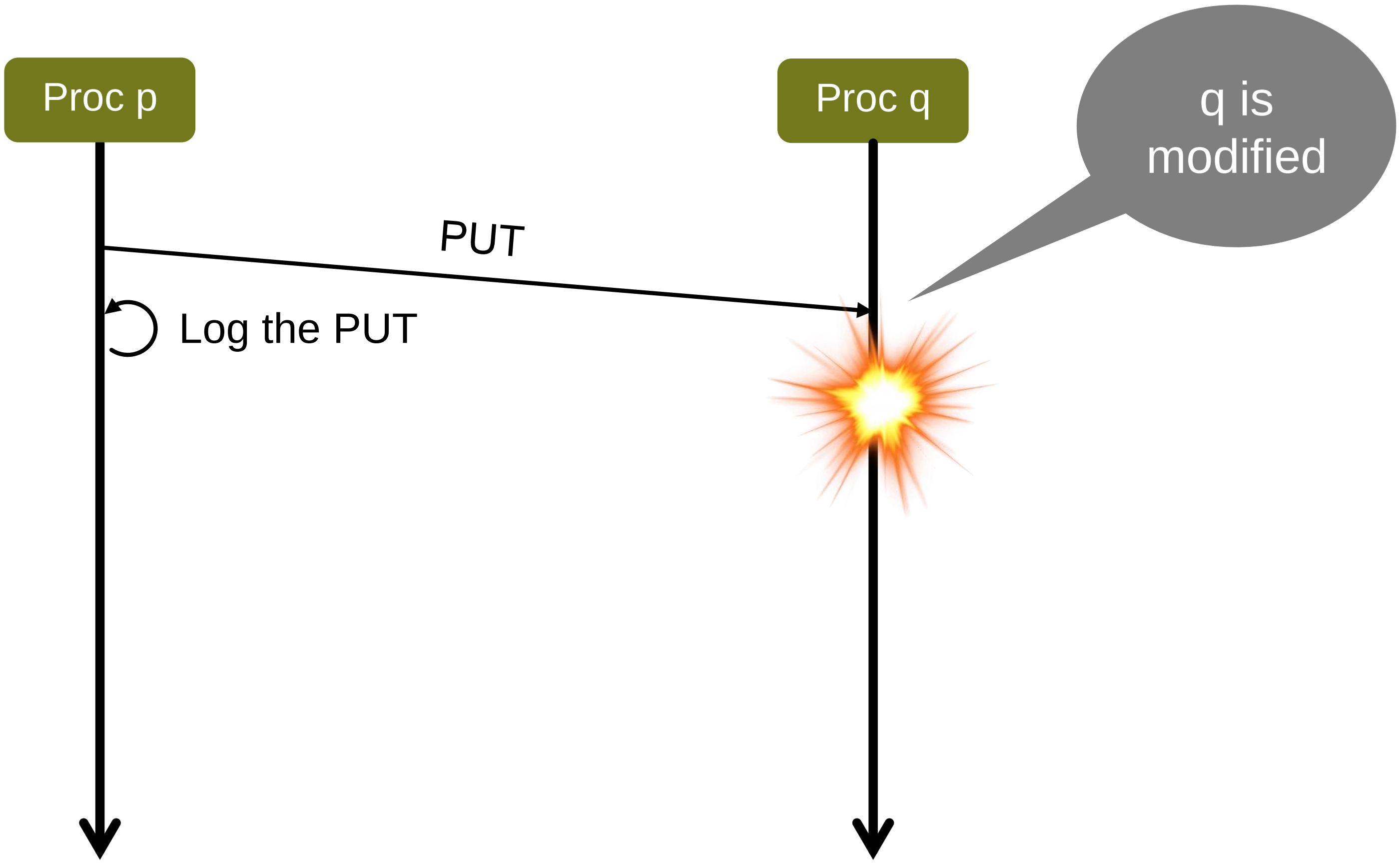

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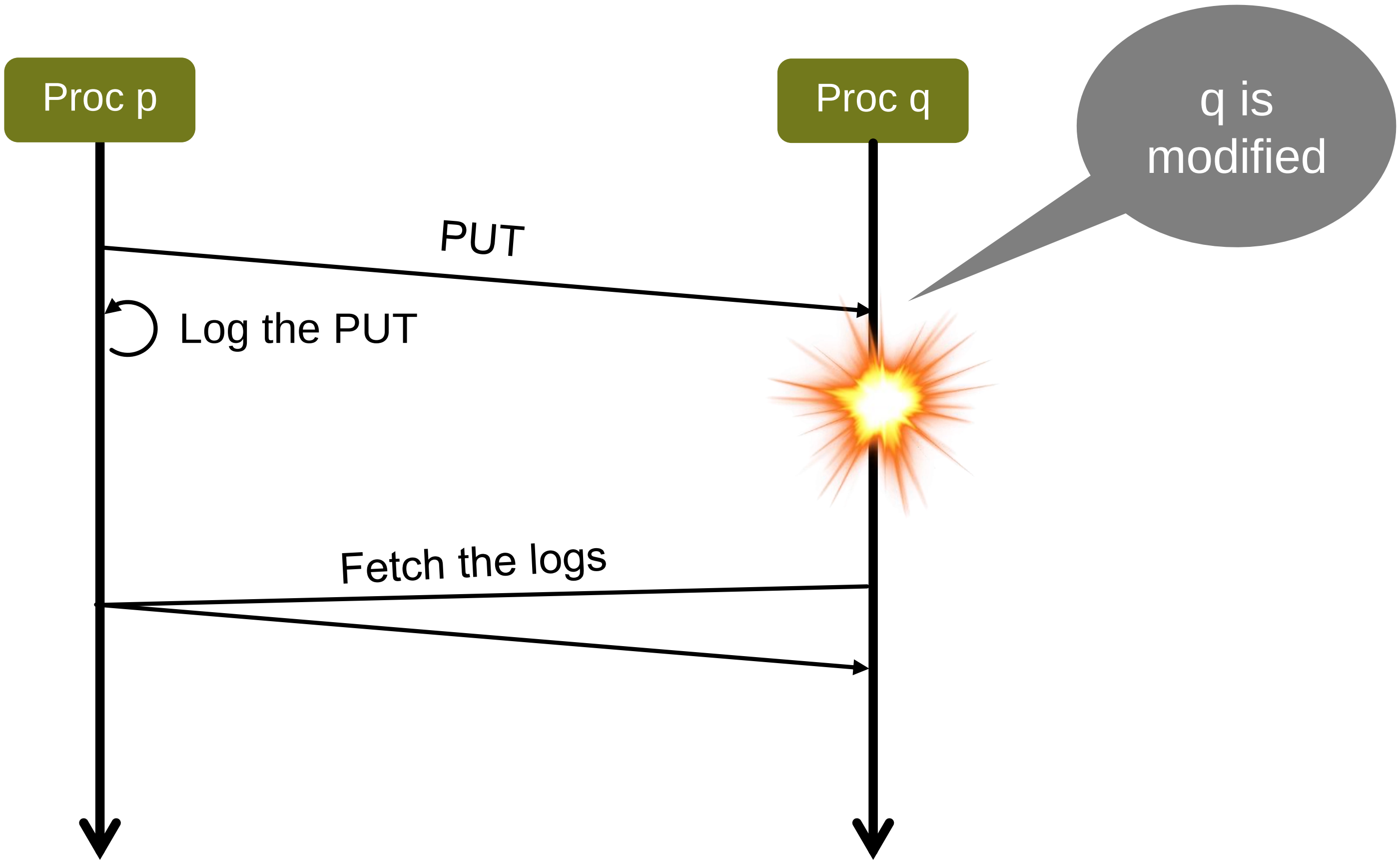

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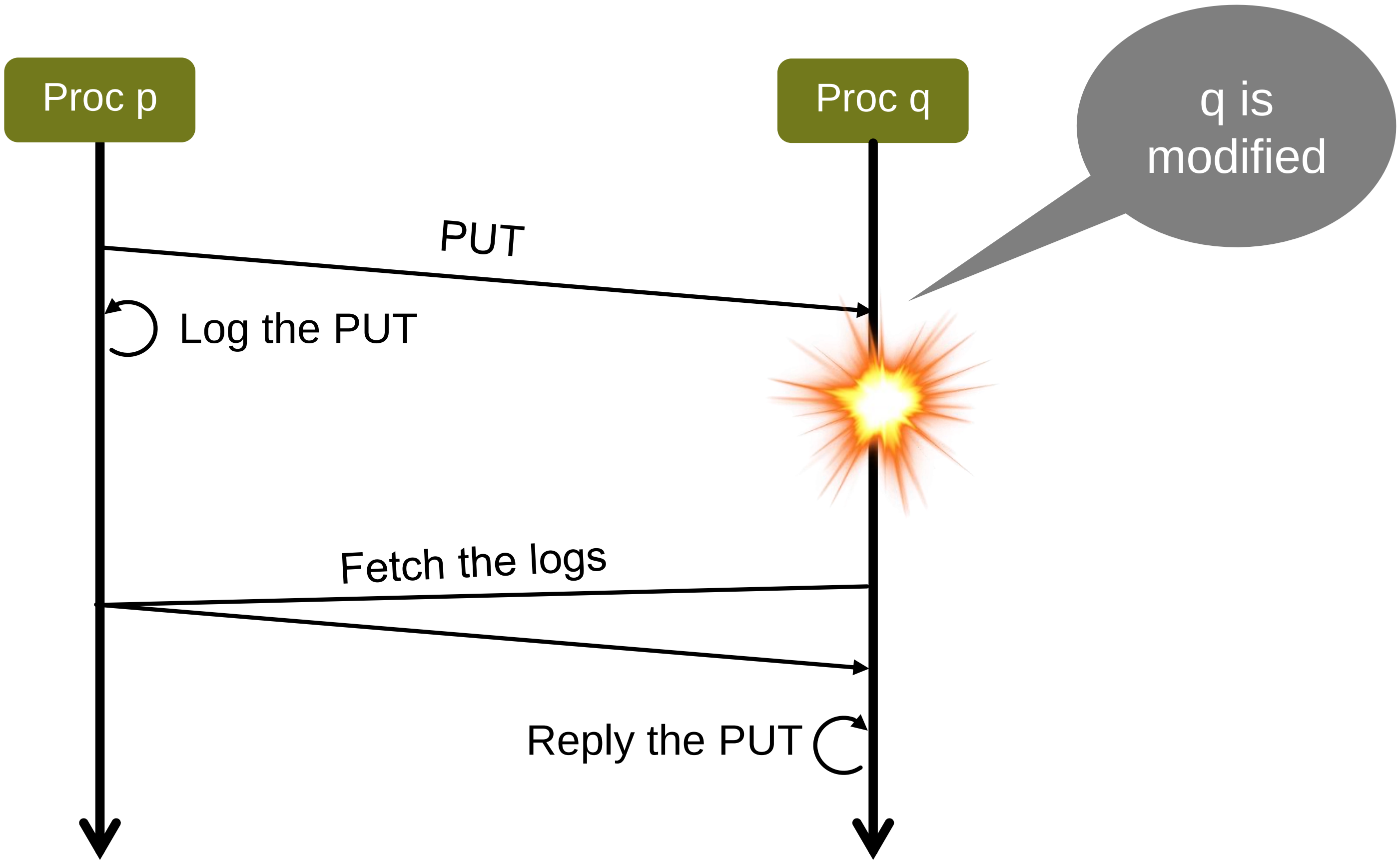

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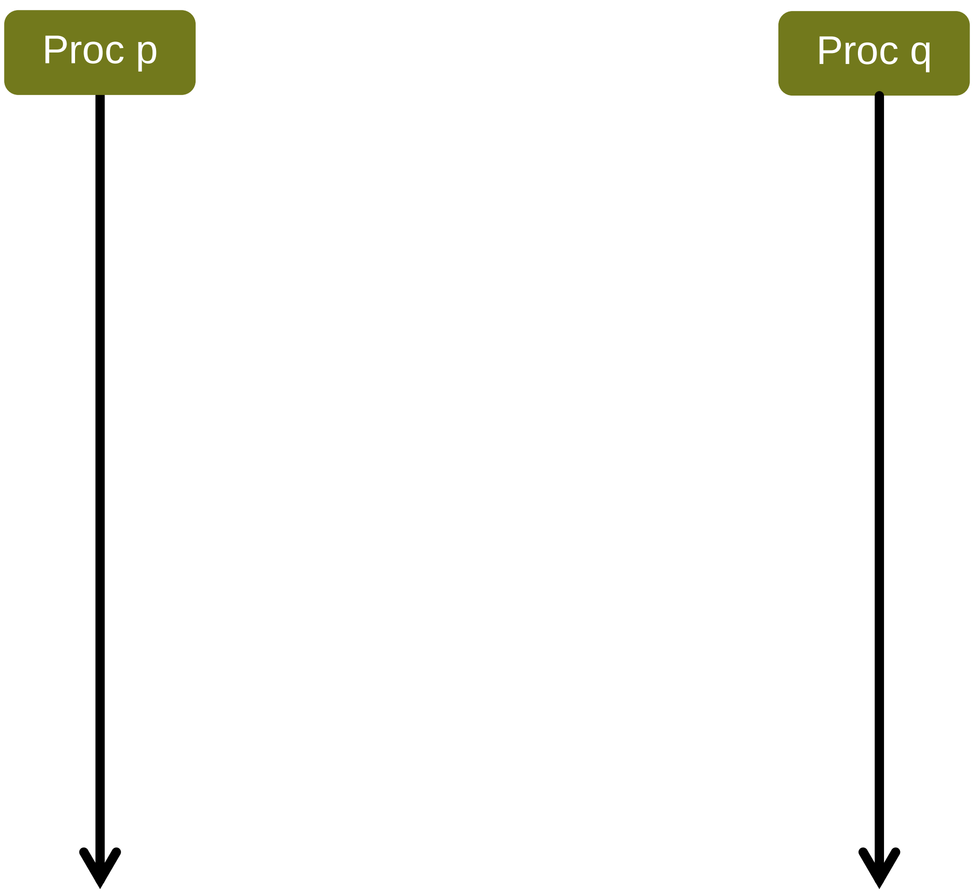

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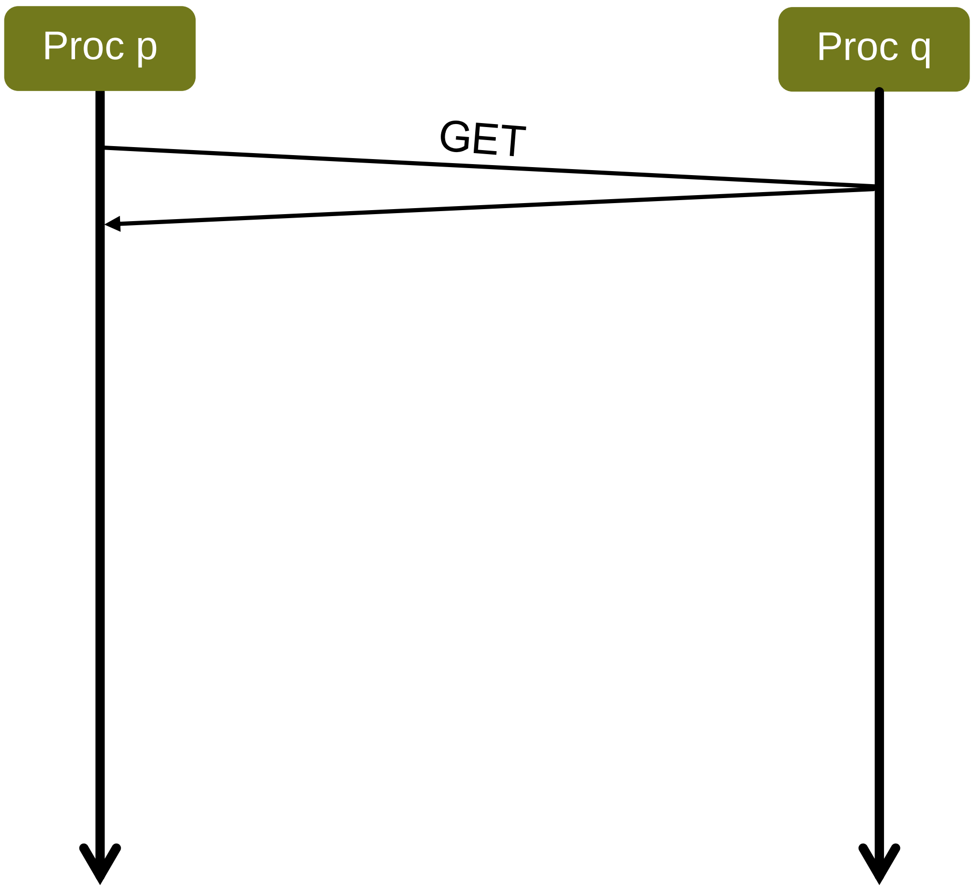

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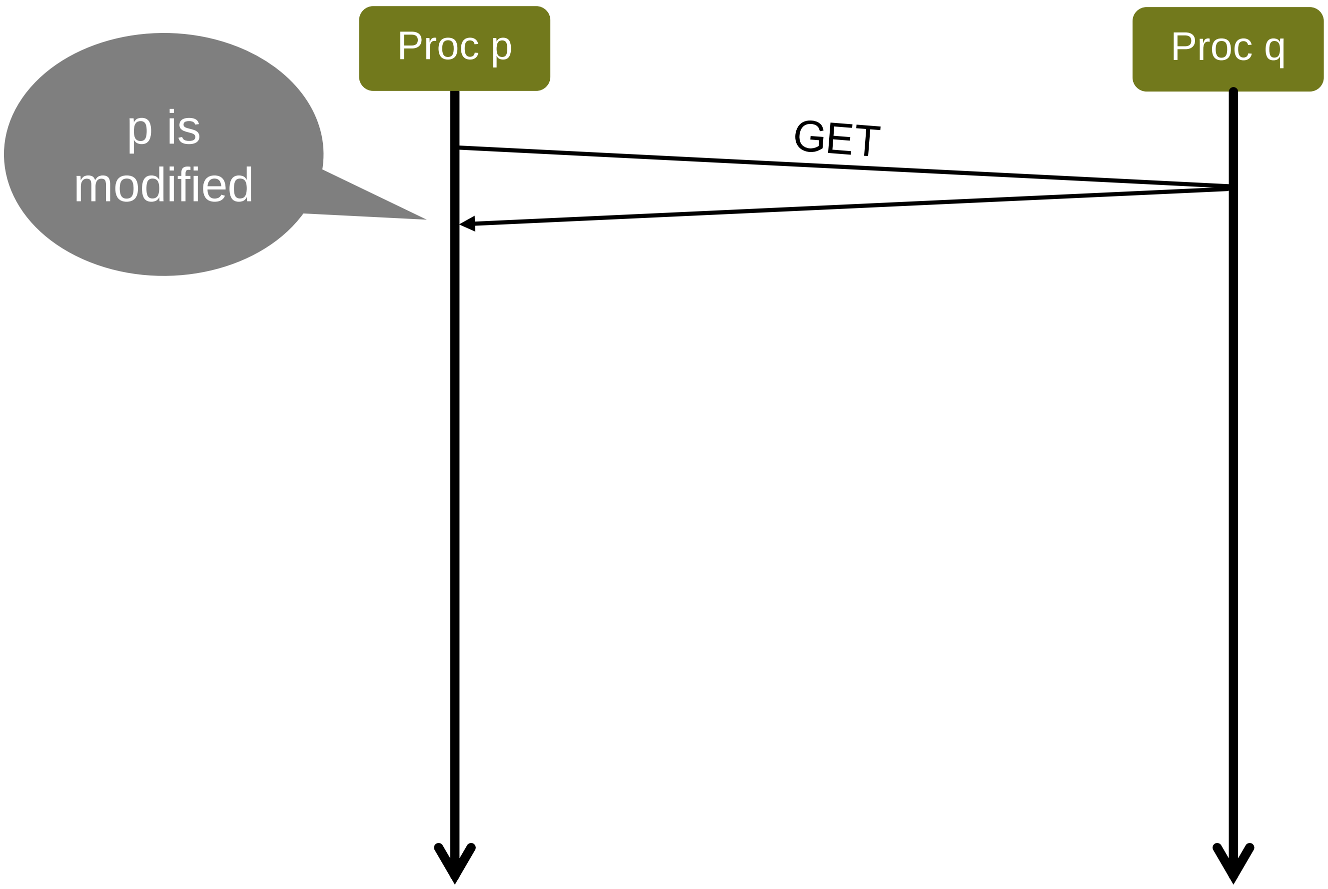

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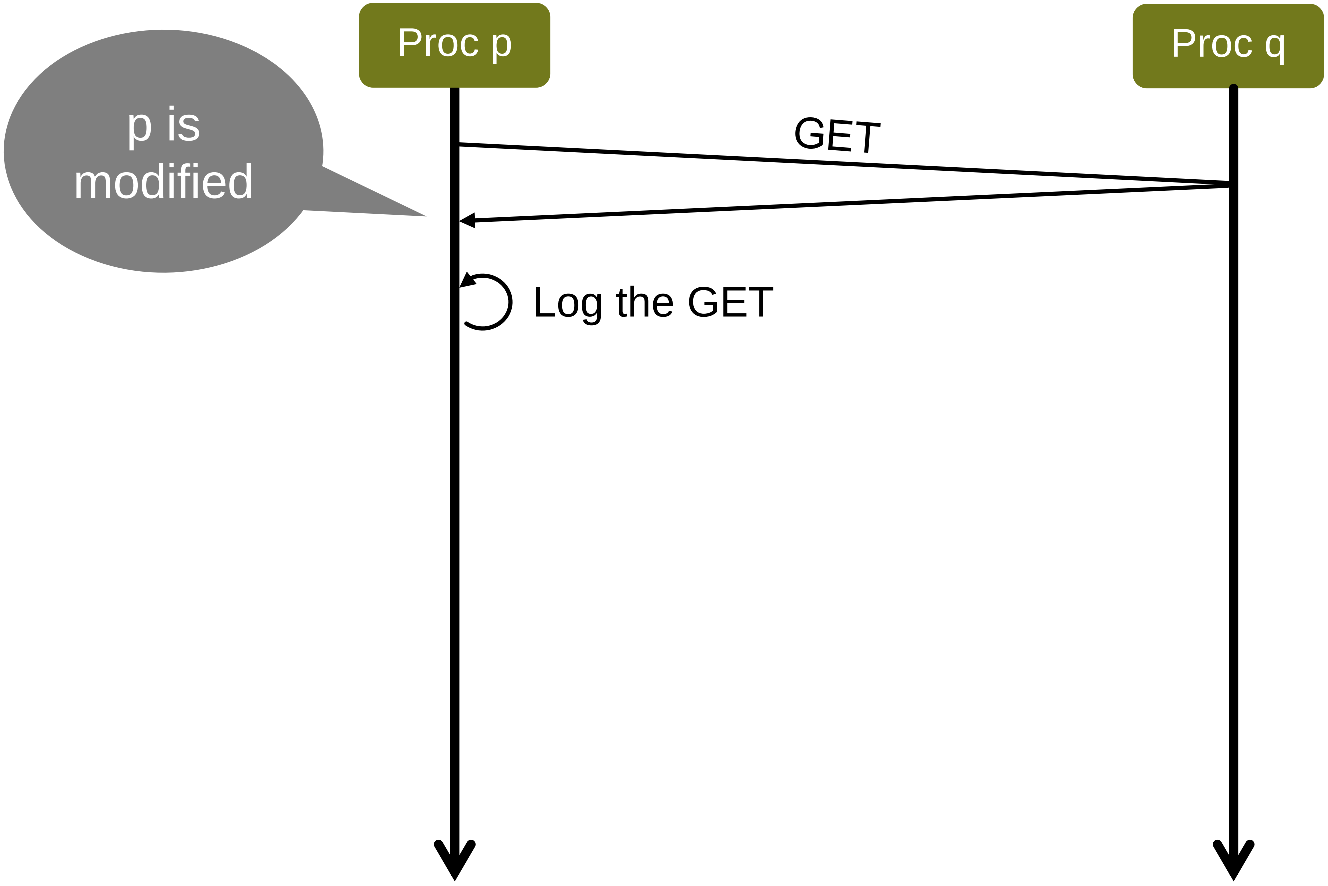

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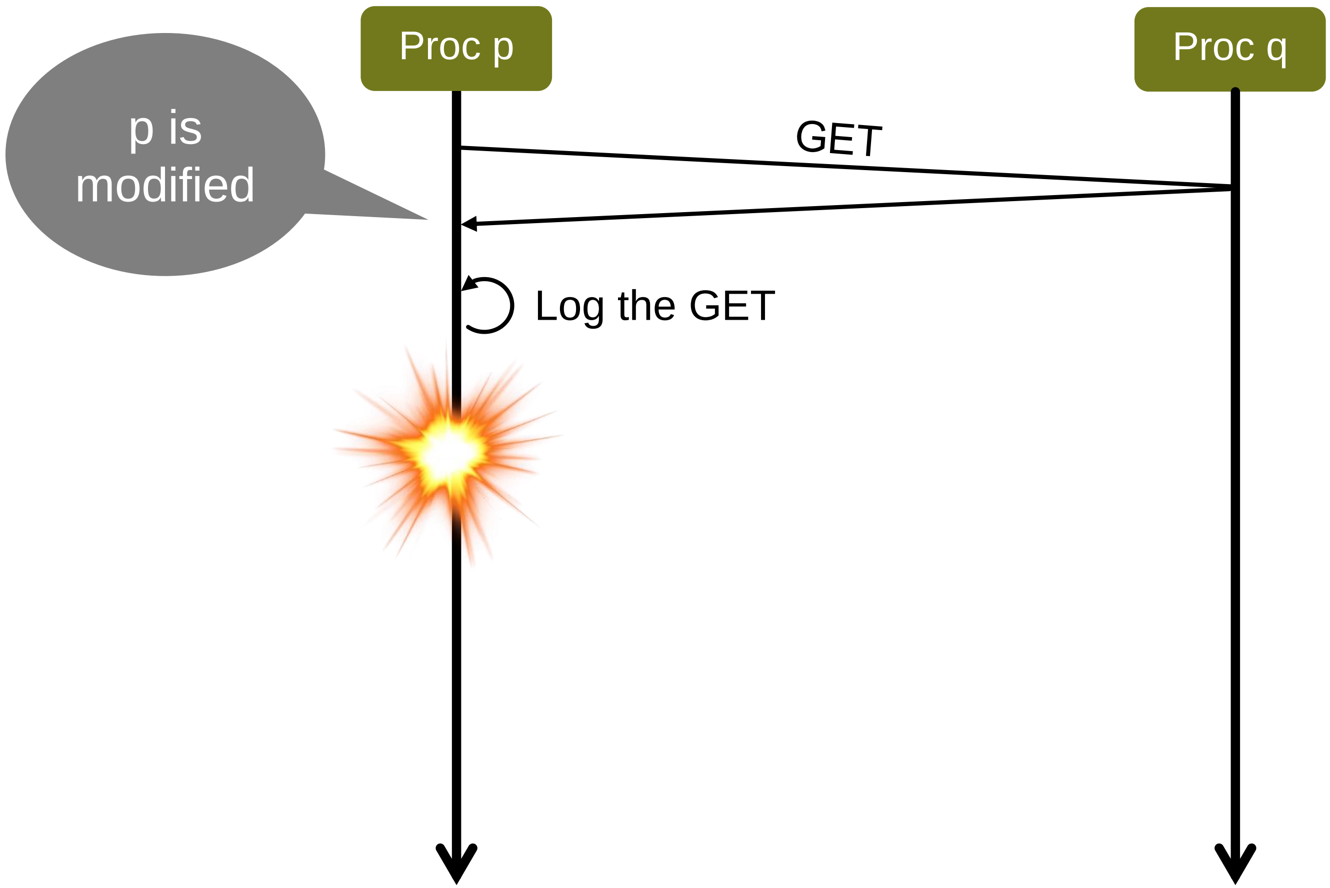

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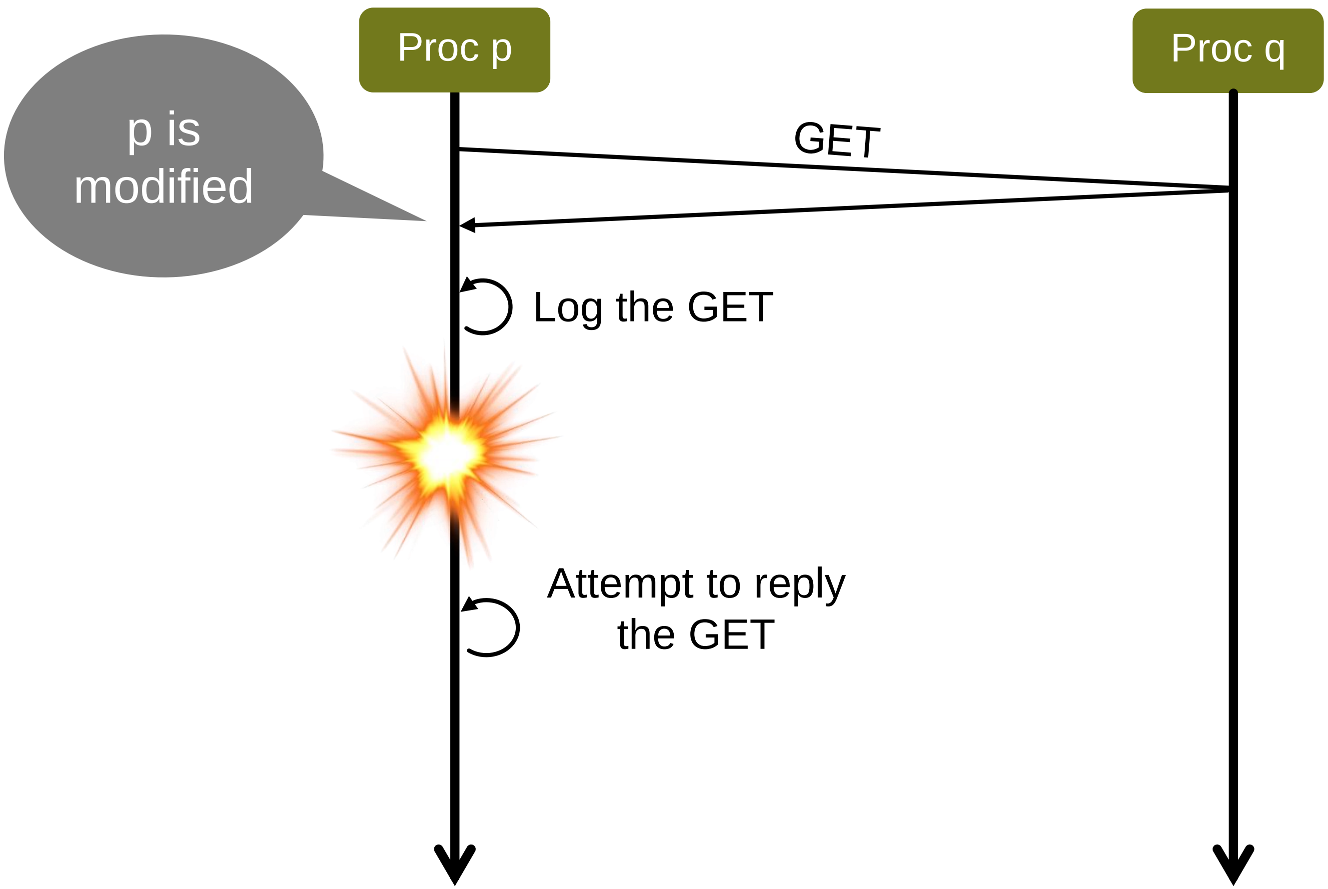

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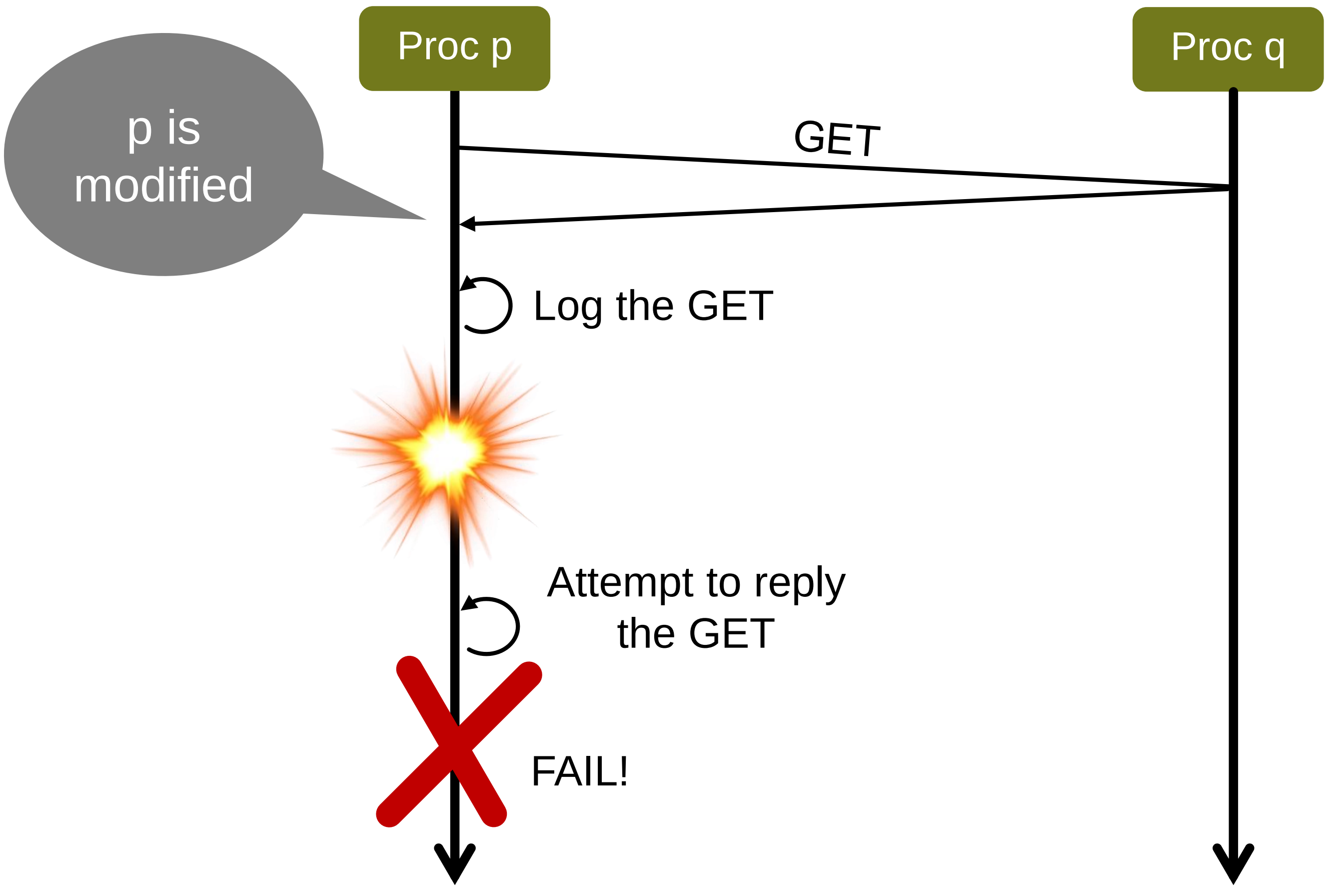

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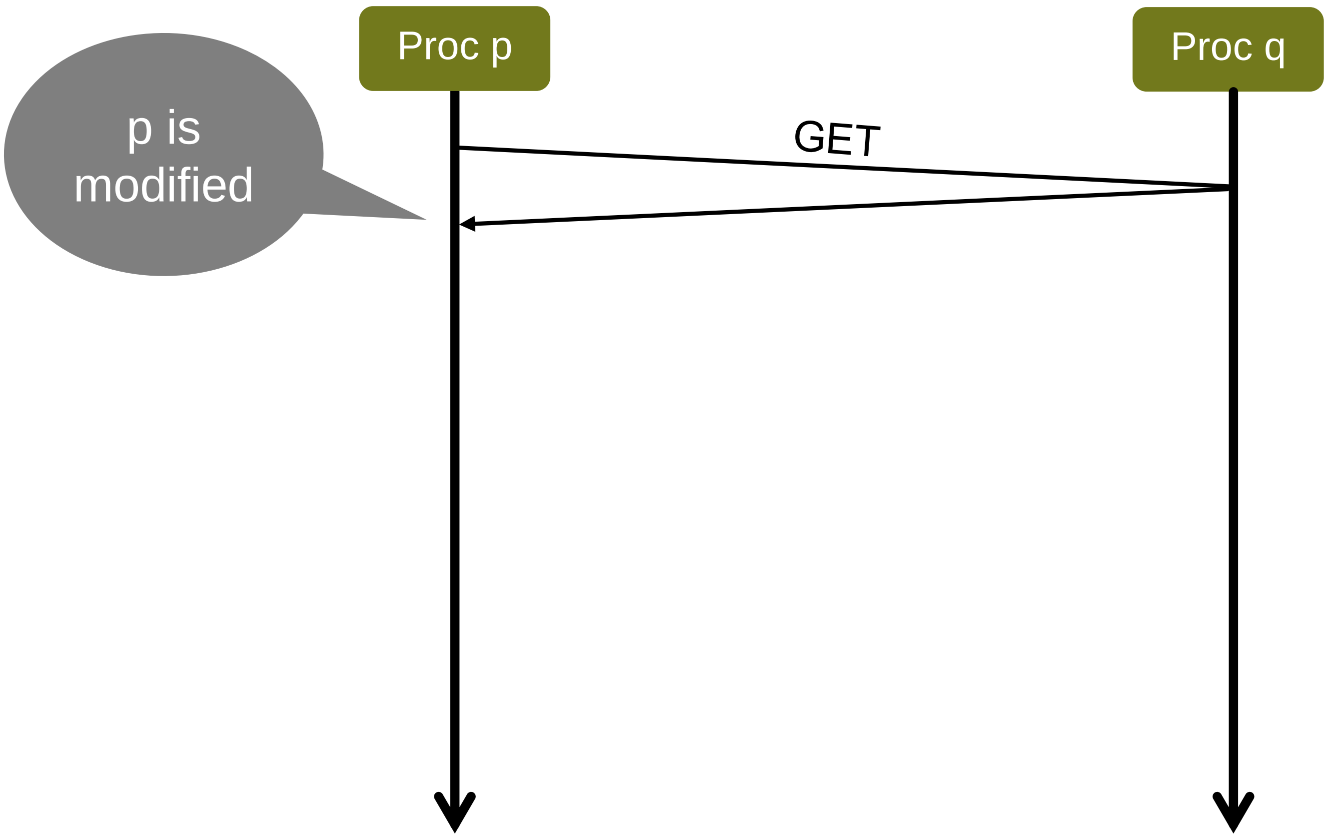


[1] M. Besta and T. Hoefler. Fault tolerance for remote memory access programming models. HPDC'14.

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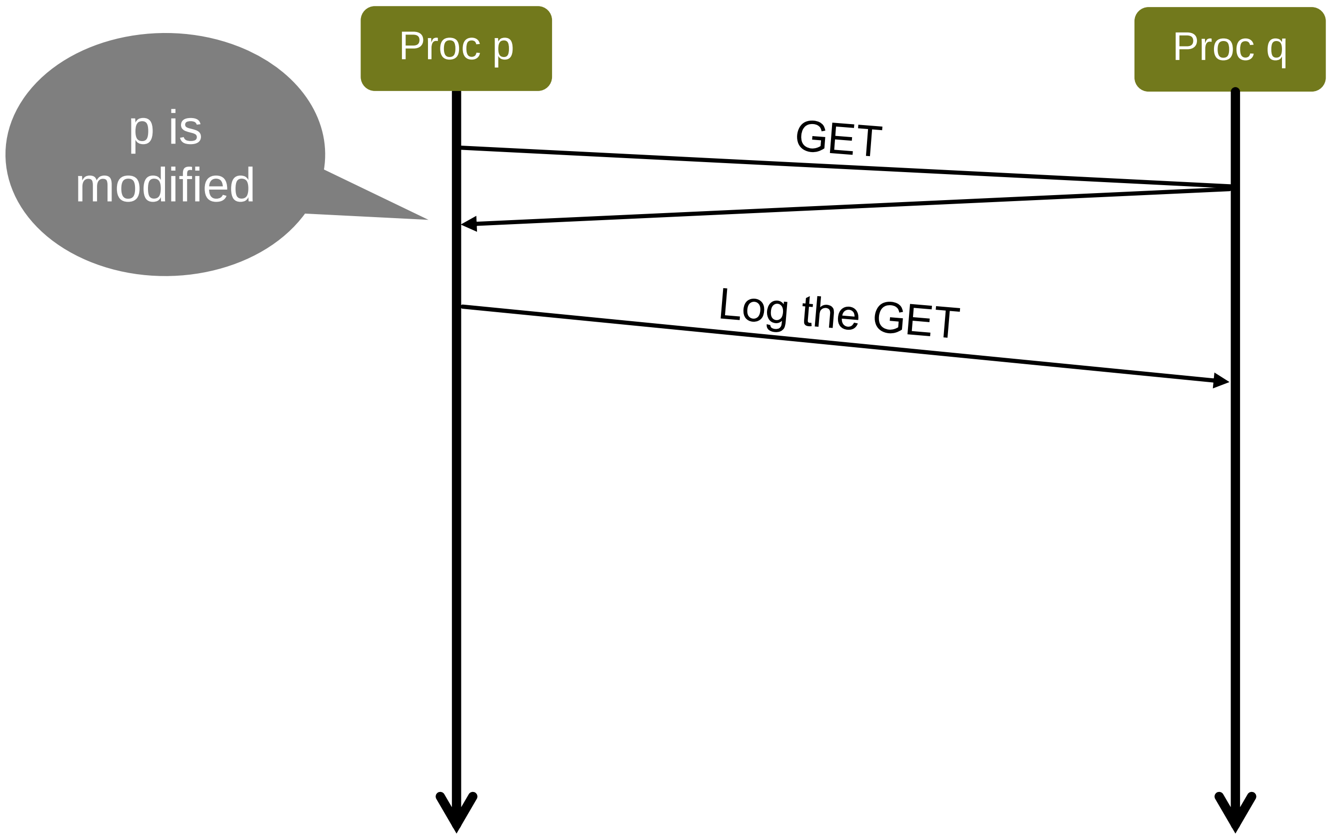


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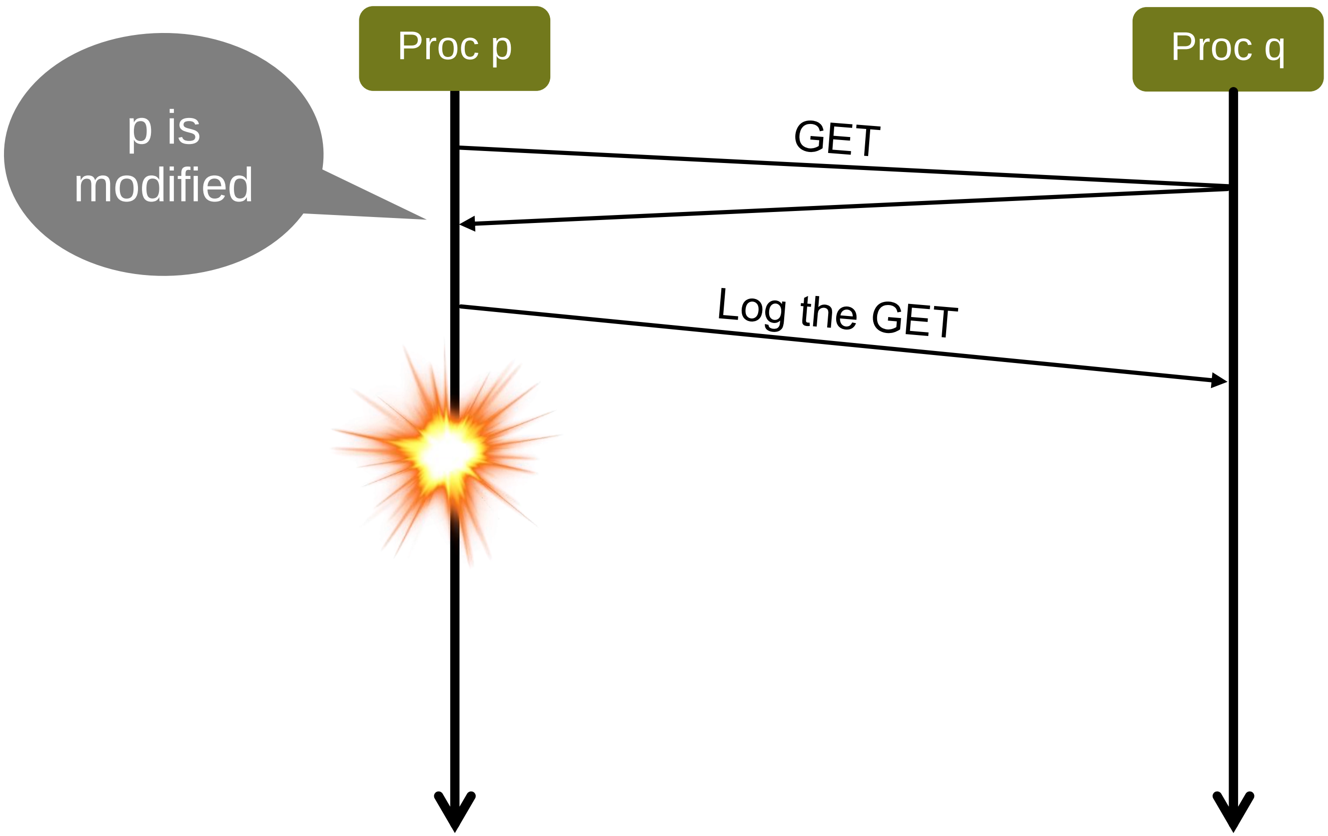


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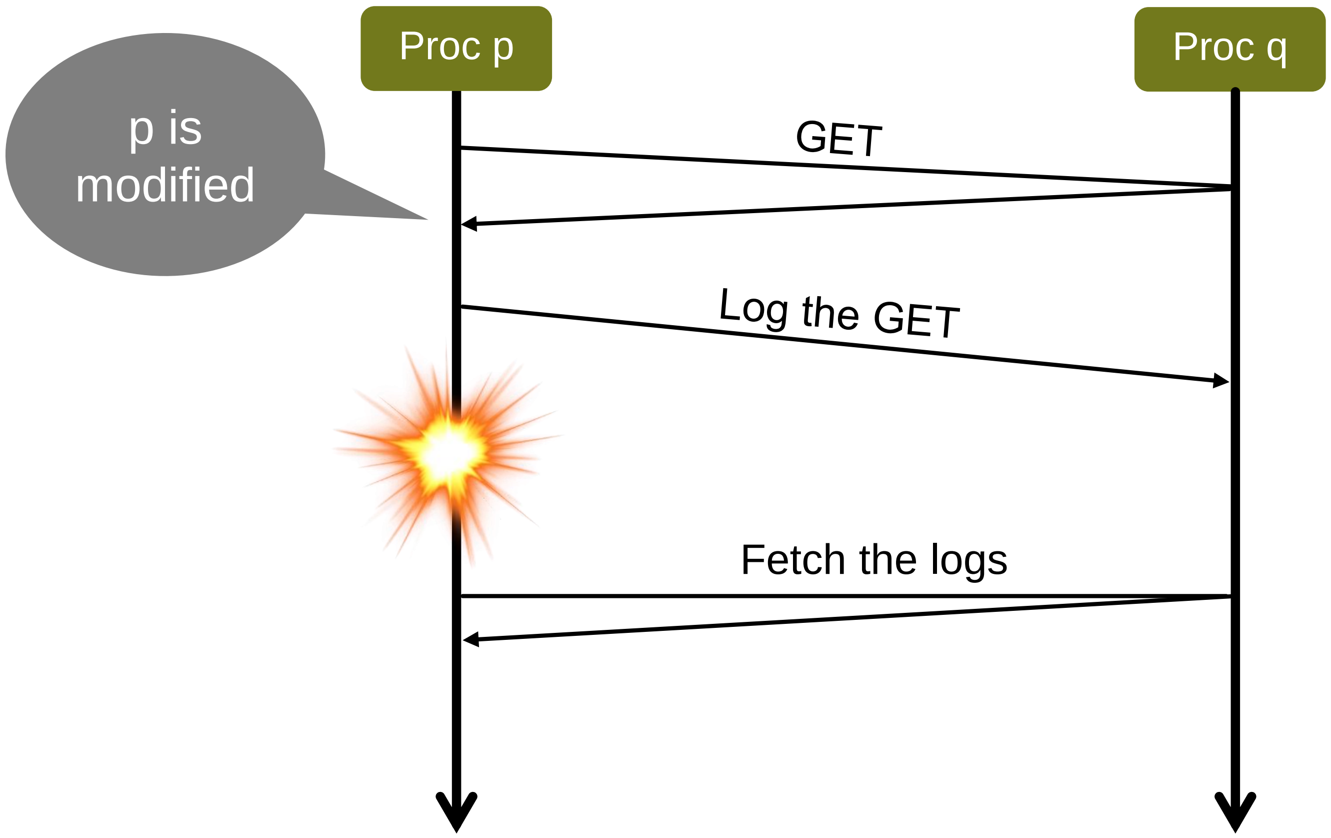


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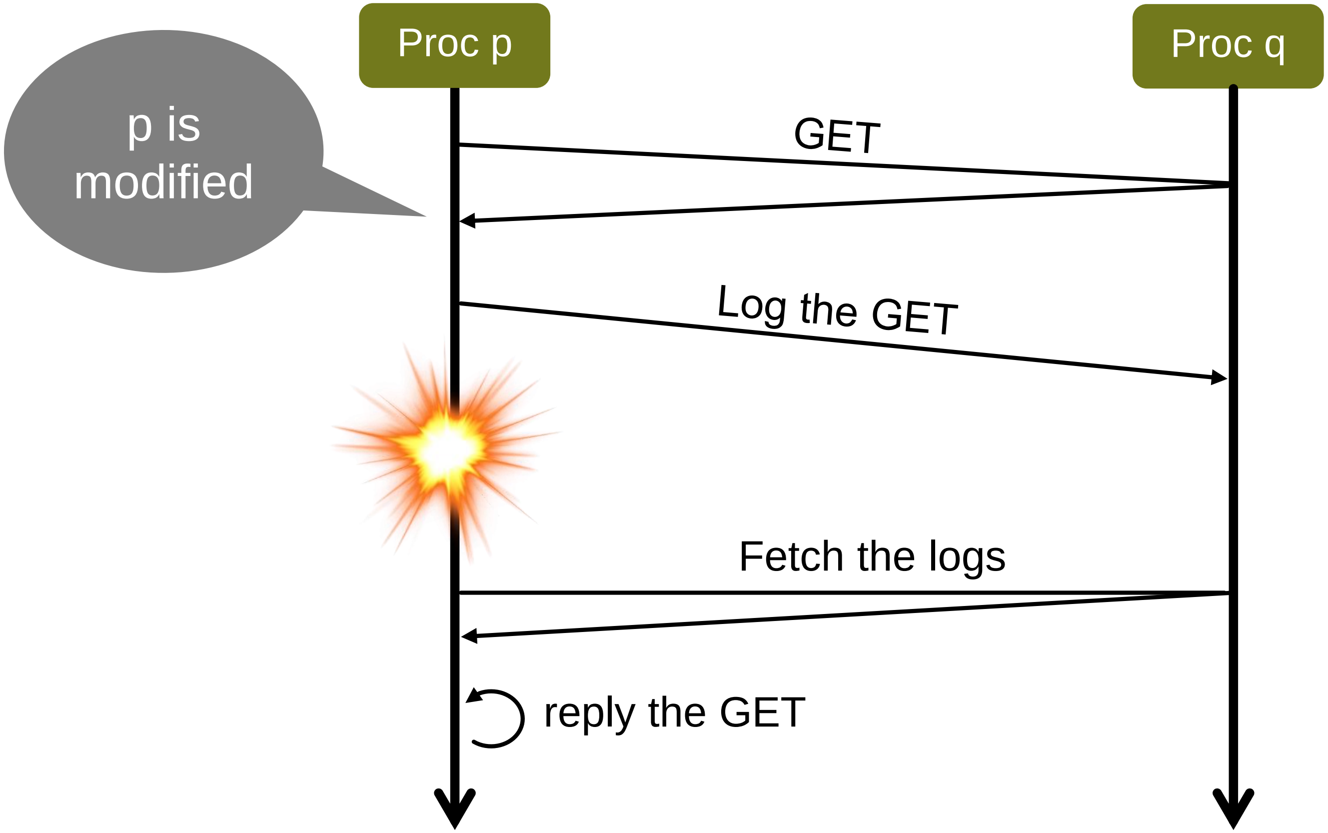


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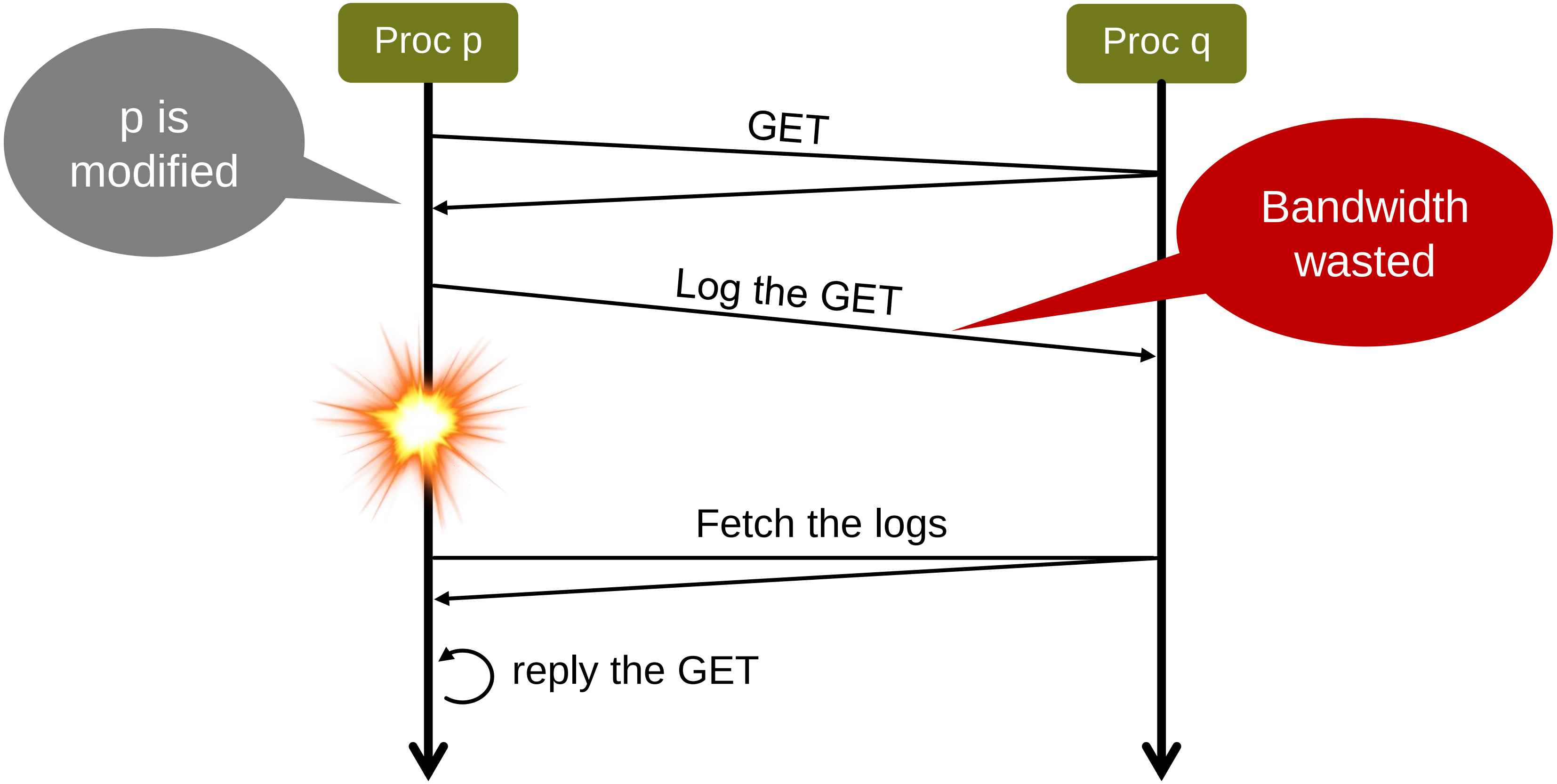


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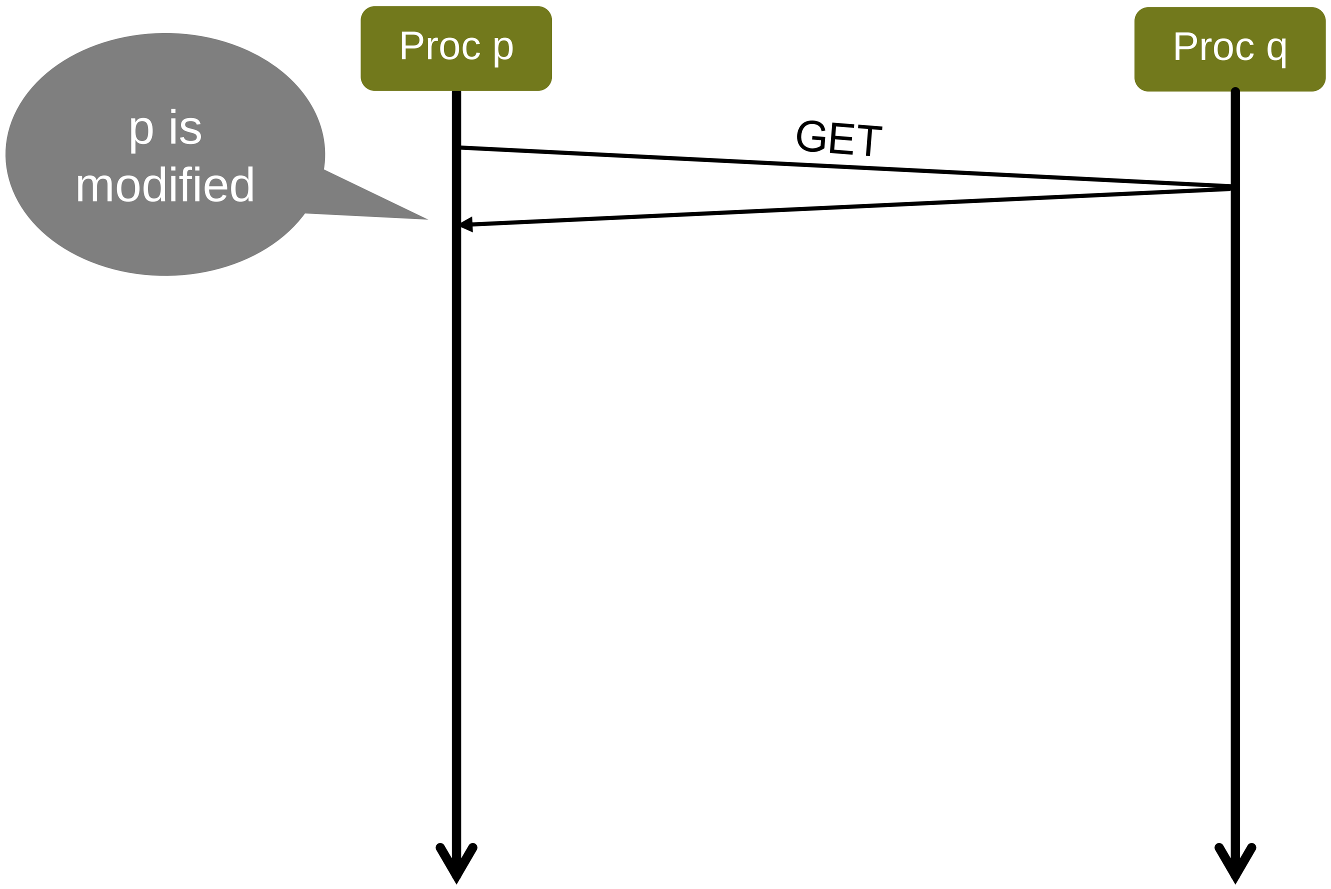

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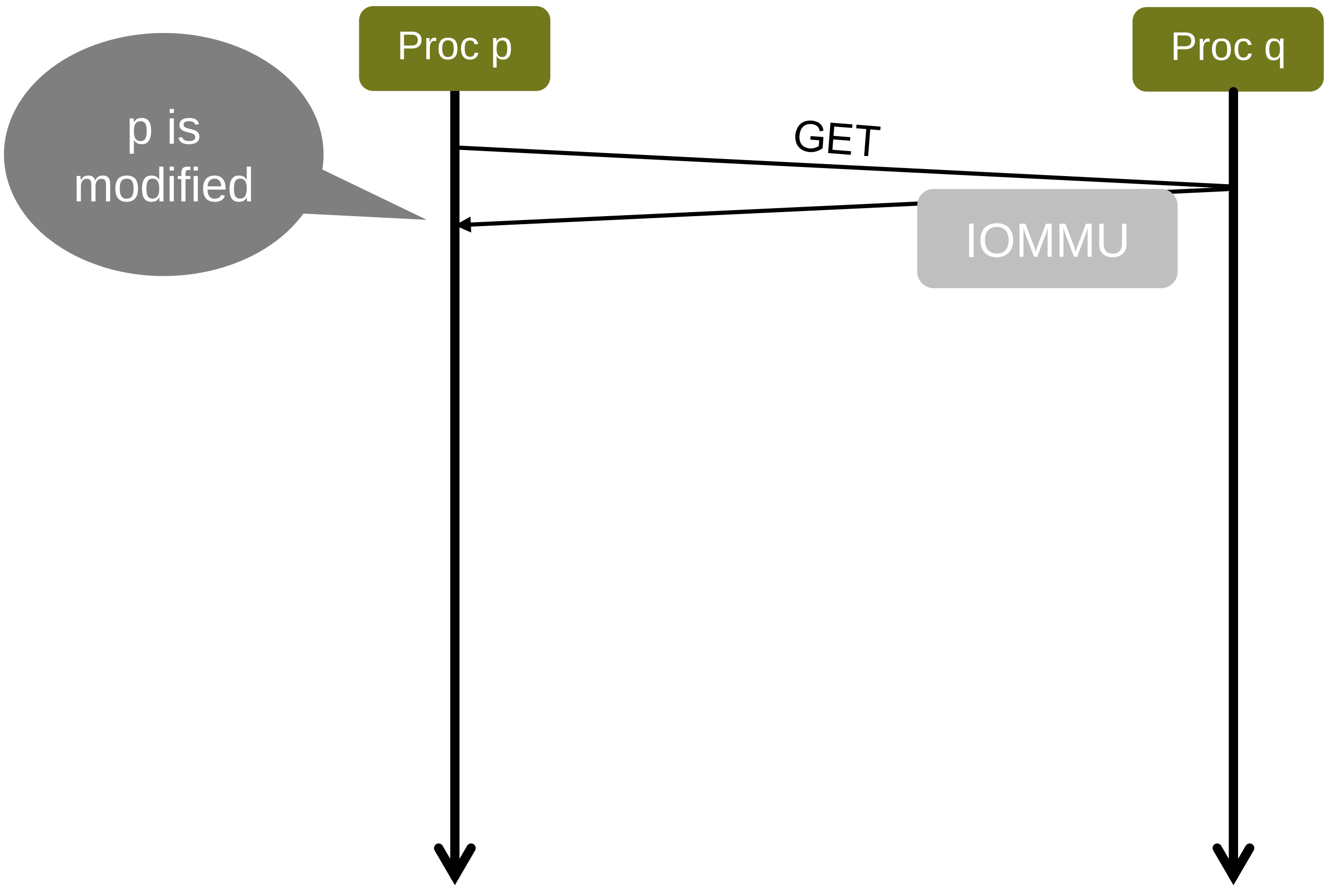

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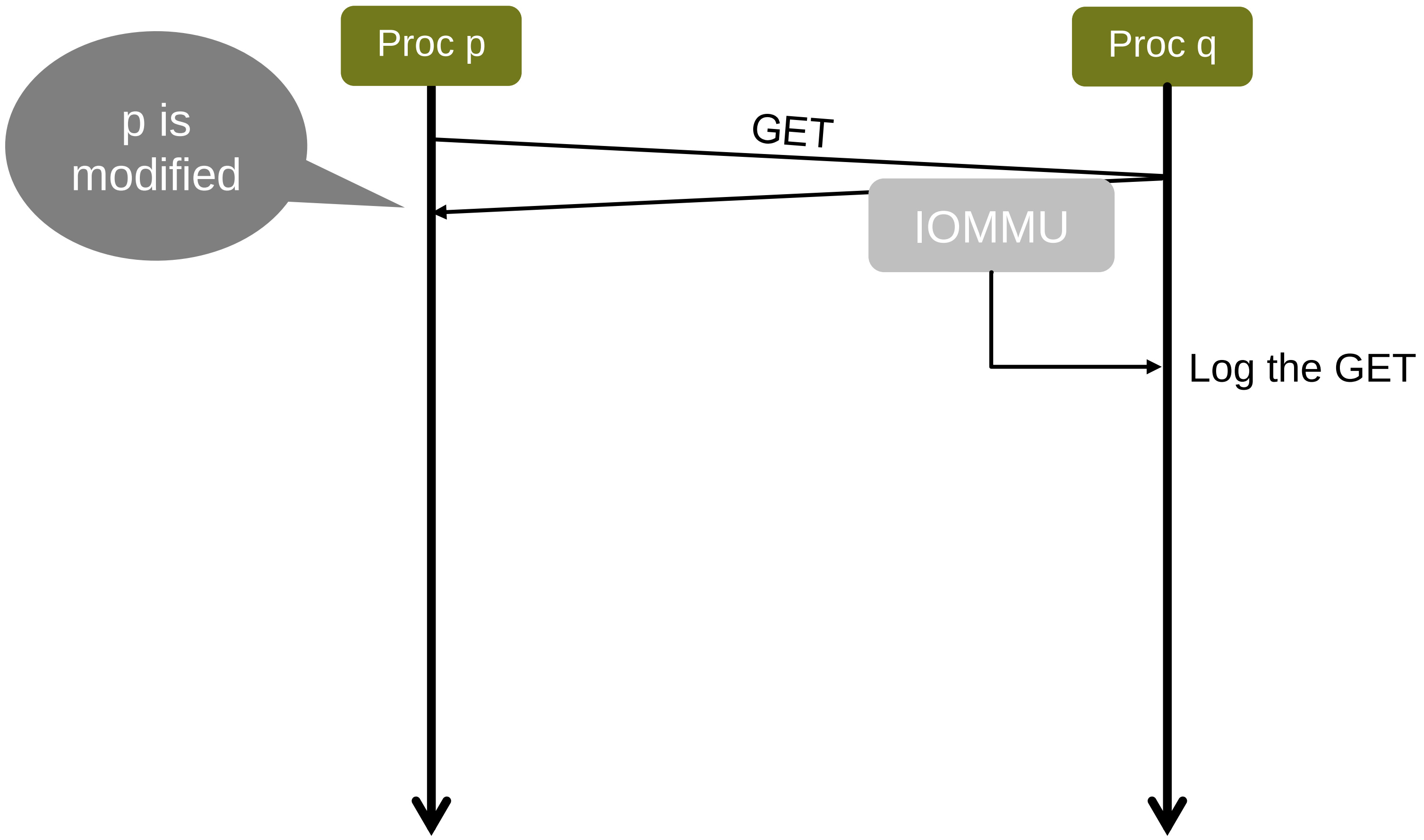
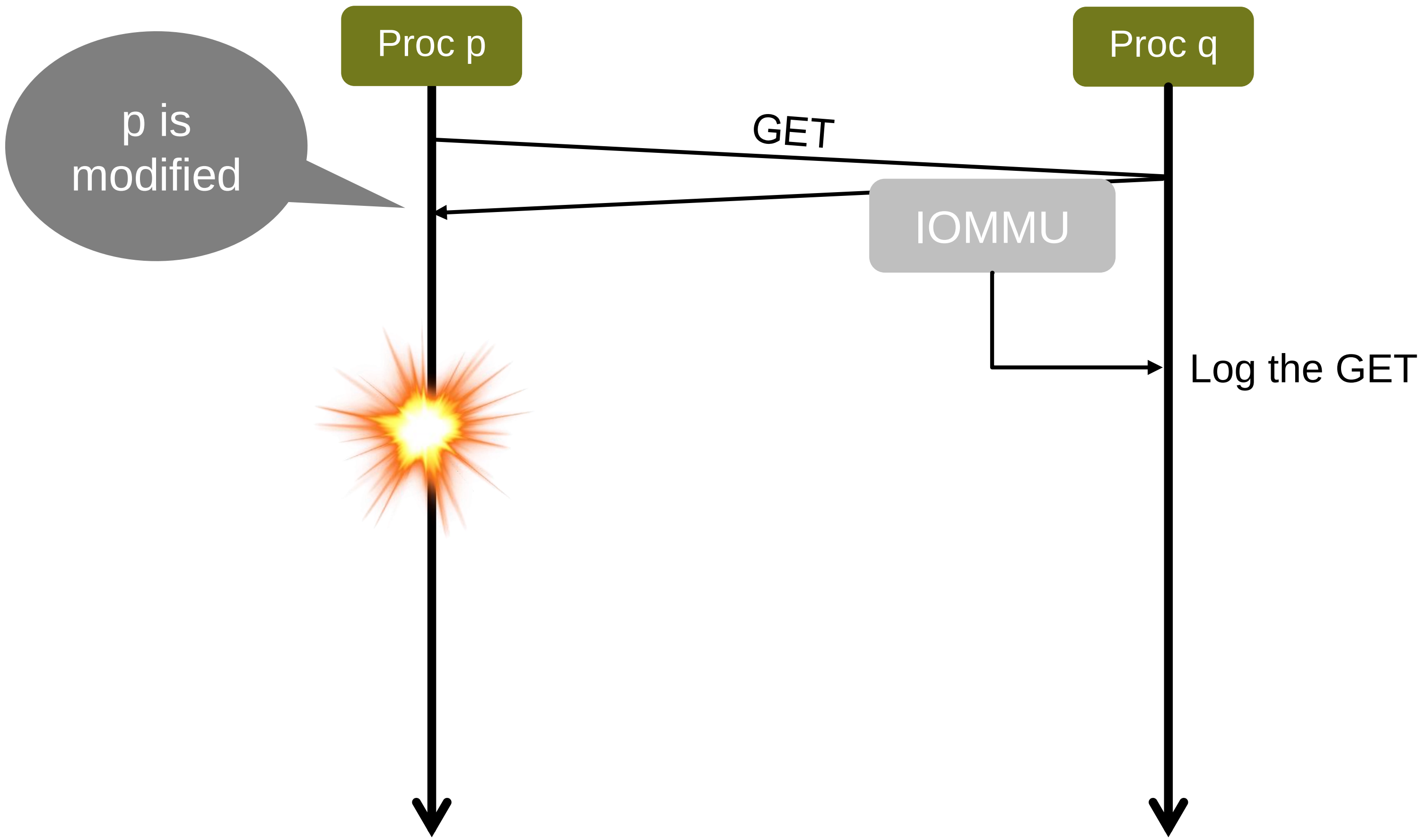


# Active Access Use-Cases

## Accelerating logging for RMA

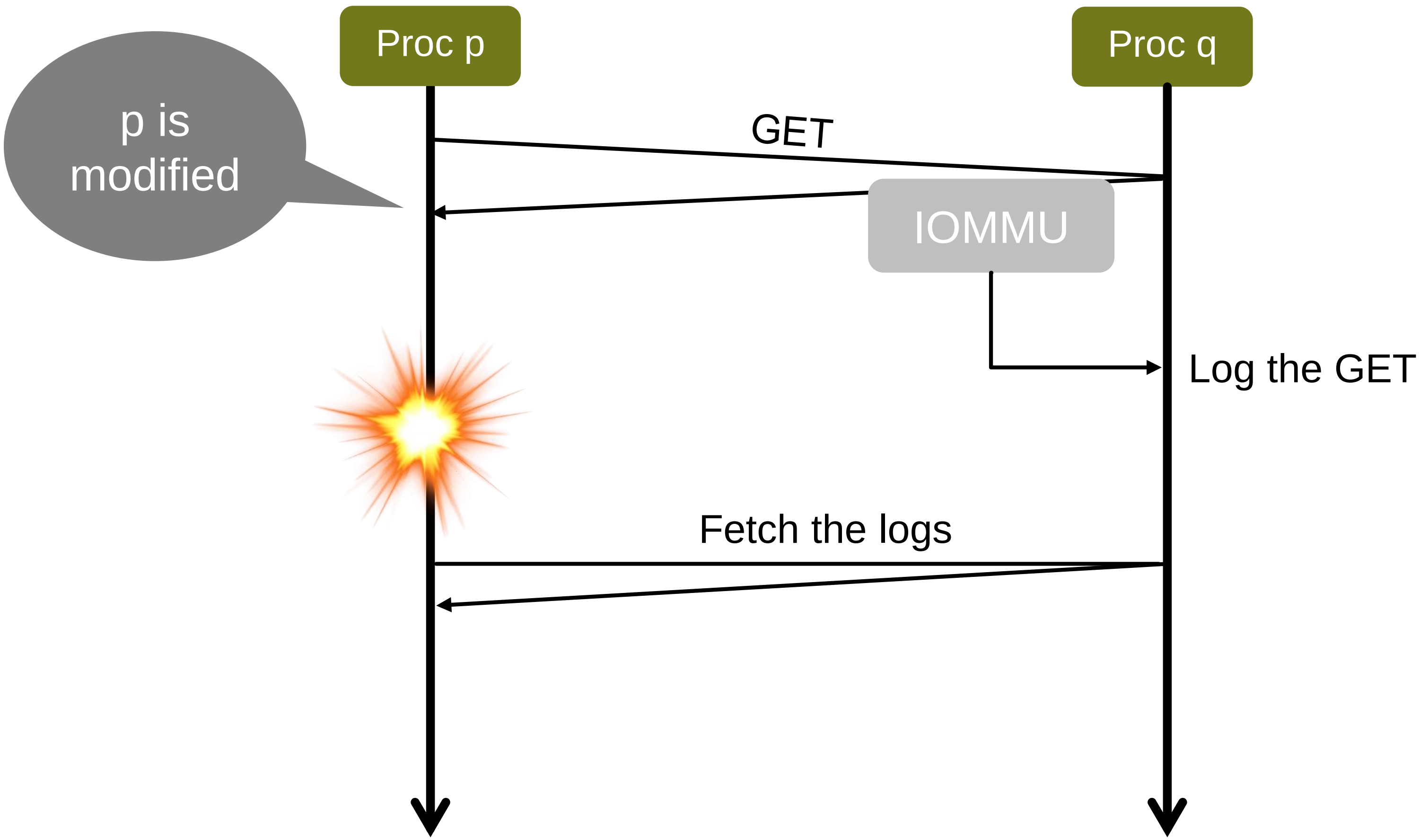
- Logging gets (AA):



# ACTIVE ACCESS USE-CASES

## ACCELERATING LOGGING FOR RMA

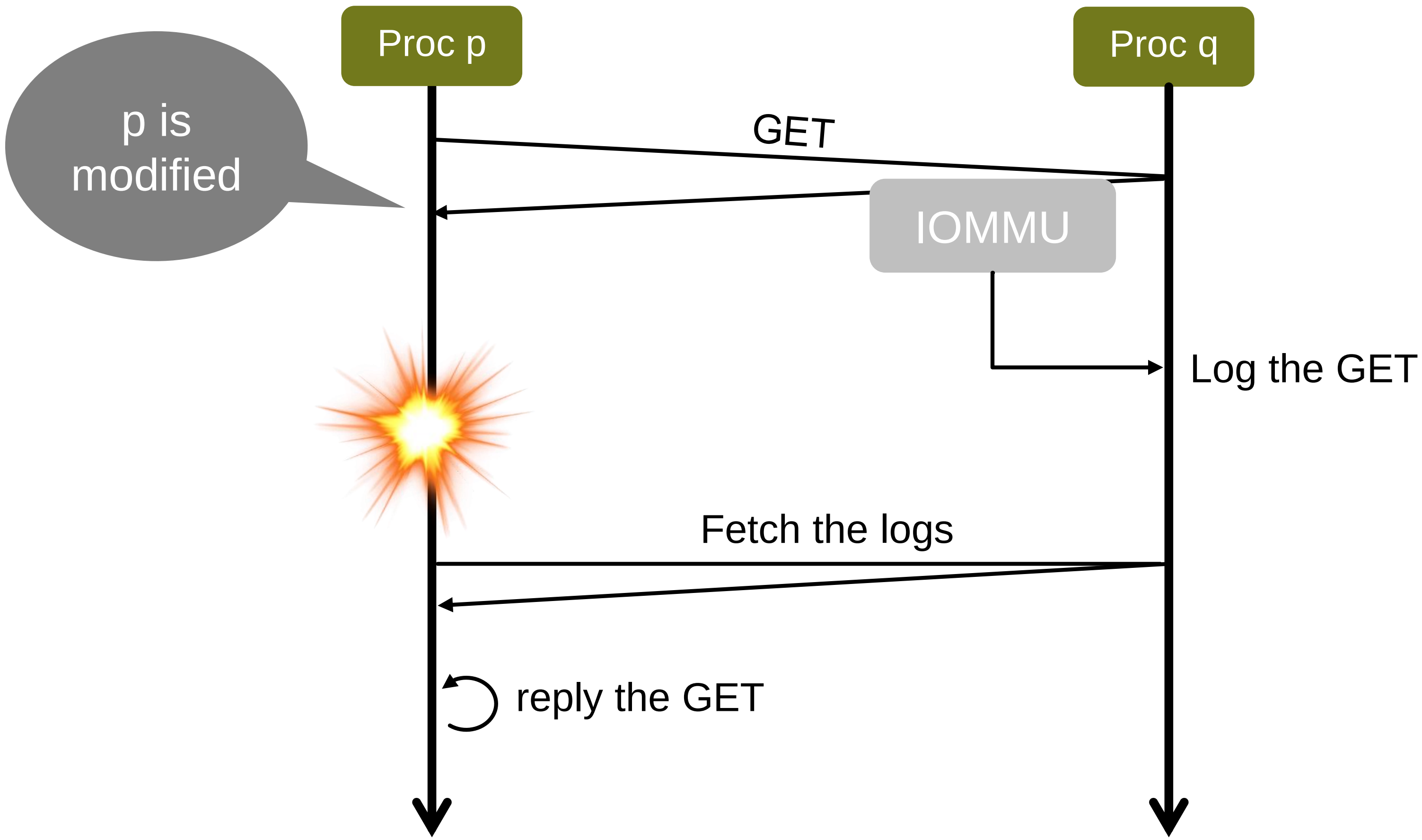
- Logging gets (AA):



# ACTIVE ACCESS USE-CASES

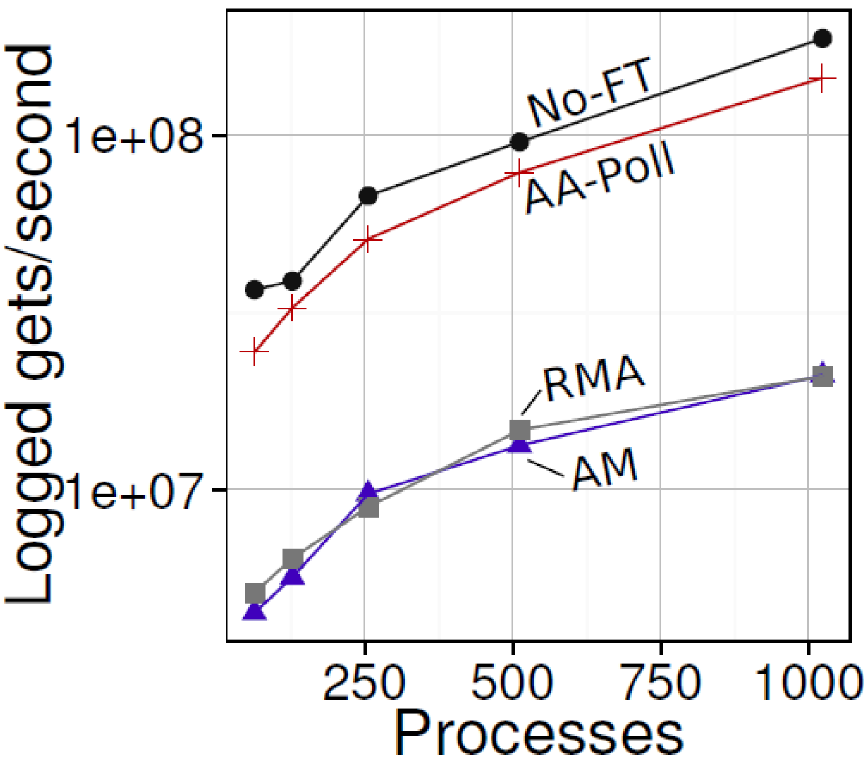
## ACCELERATING LOGGING FOR RMA

- Logging gets (AA):



# Performance: Large-Scale Codes
## Fault Tolerance Scheme

Logging gets:




Sorting time: