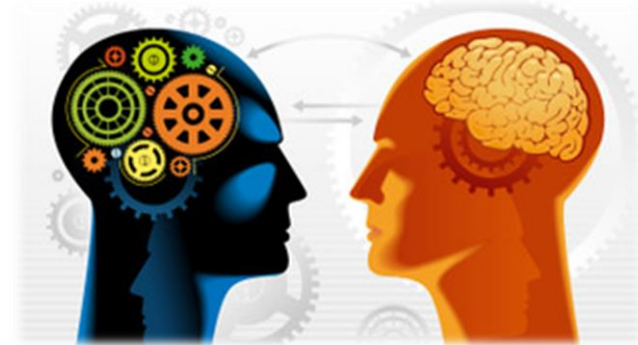
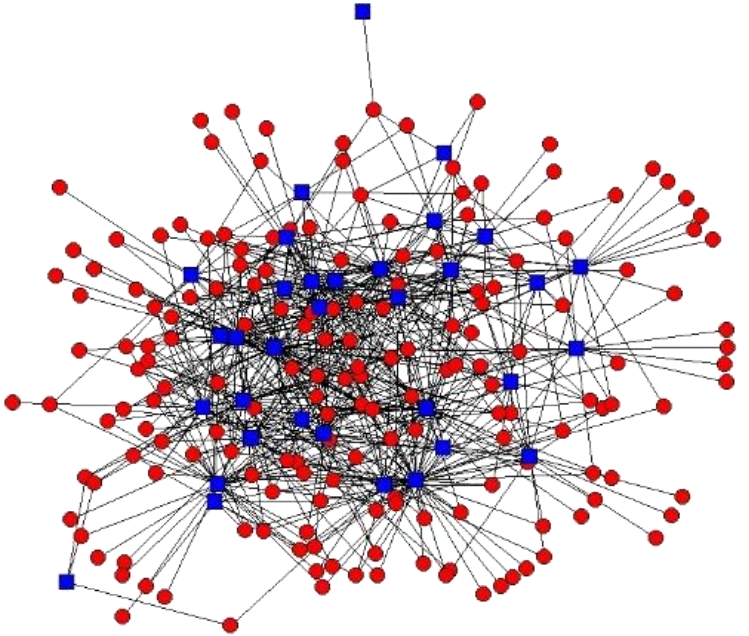


High-Performance Distributed RMA Locks

PATRICK SCHMID, MACIEJ BESTA, TORSTEN HOEFLER



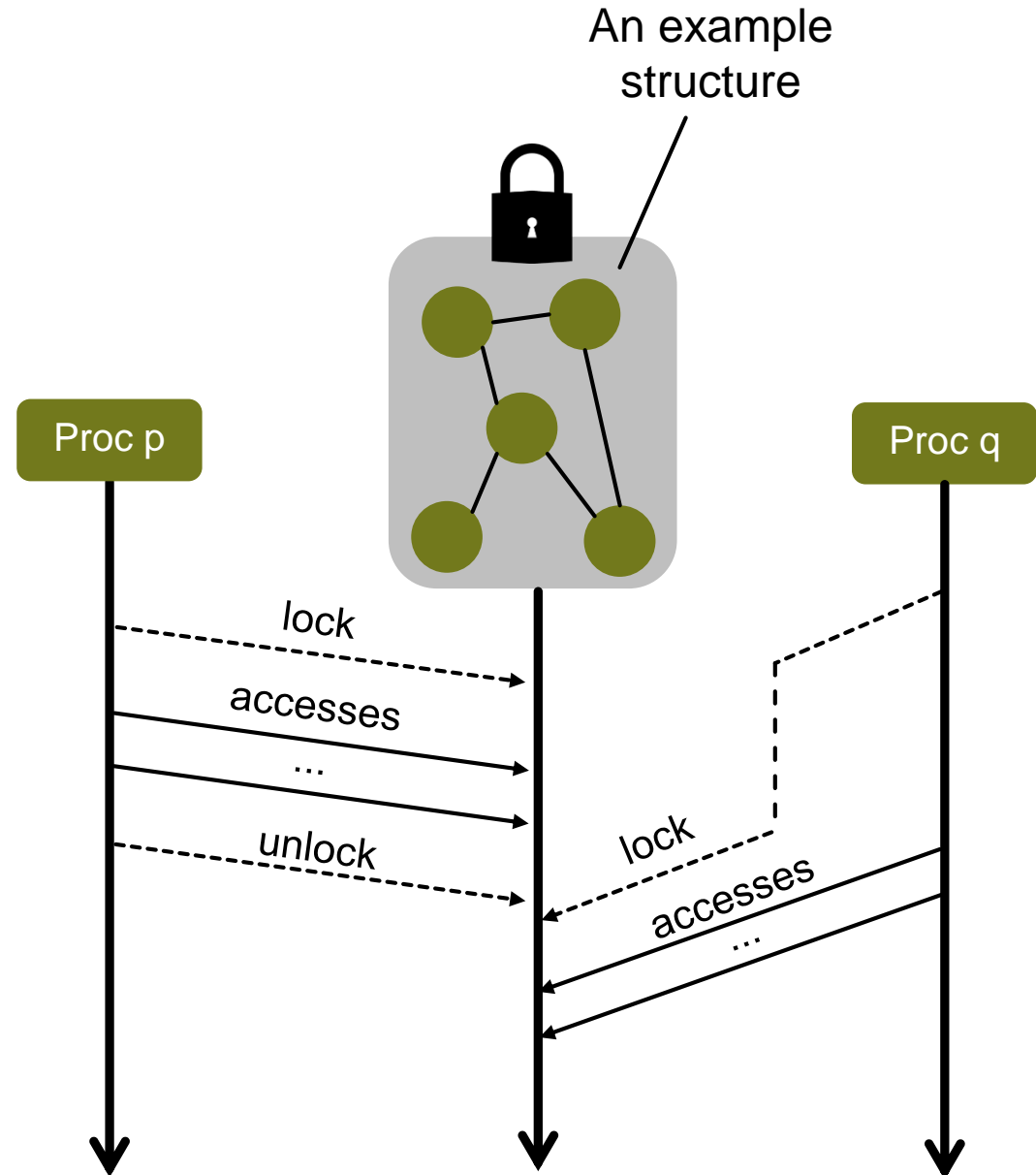
NEED FOR EFFICIENT LARGE-SCALE SYNCHRONIZATION



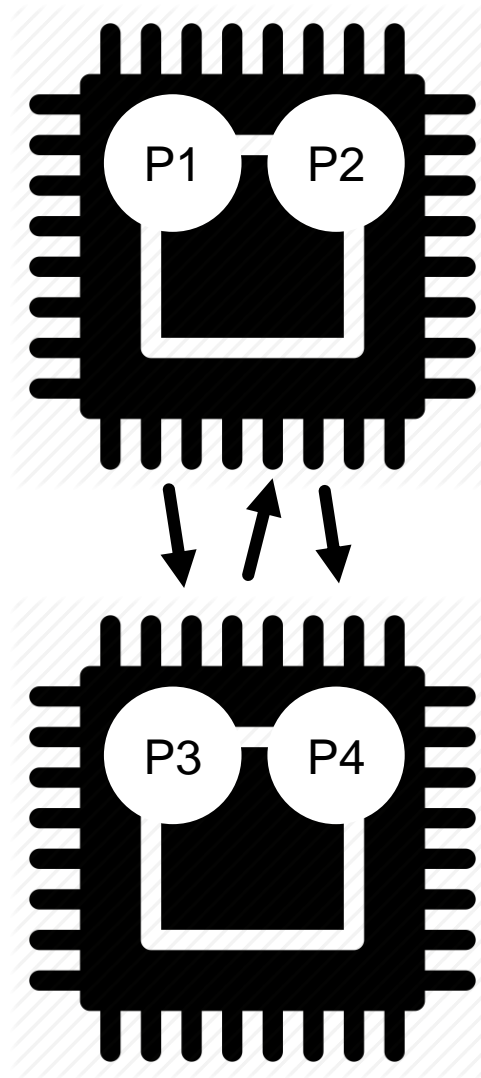
LOCKS

 Inuitive semantics

 Various performance penalties



LOCKS: CHALLENGES



LOCKS: CHALLENGES



We need intra- and inter-node topology-awareness



We need to cover arbitrary topologies



LOCKS: CHALLENGES



We need to distinguish
between readers and writers

Reader

Reader

Reader

Writer



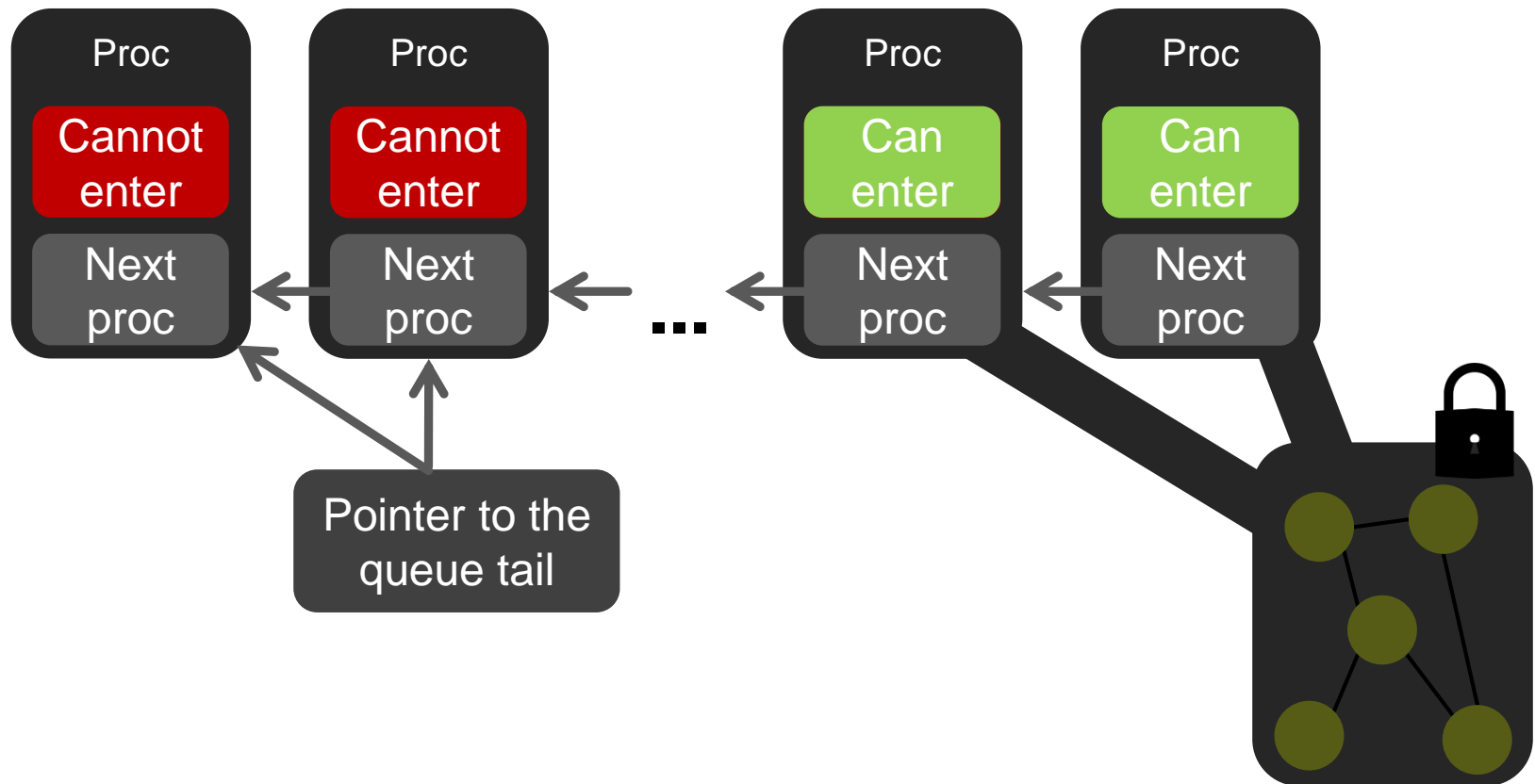
We need flexible
performance for both types
of processes



What will we use in the
design?

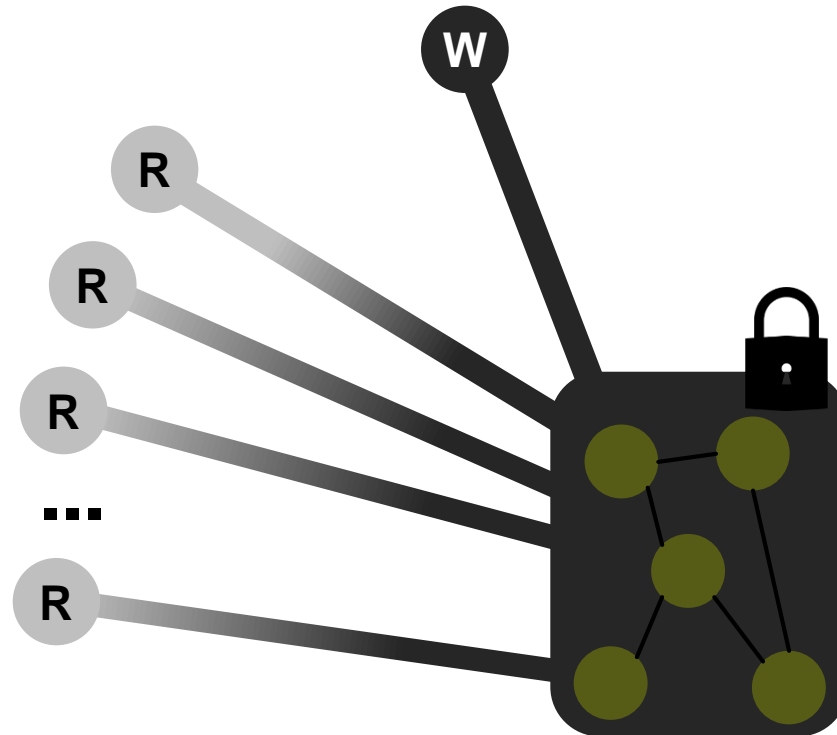
WHAT WE WILL USE

MCS Locks



WHAT WE WILL USE

Reader-Writer Locks





How to manage the design complexity?

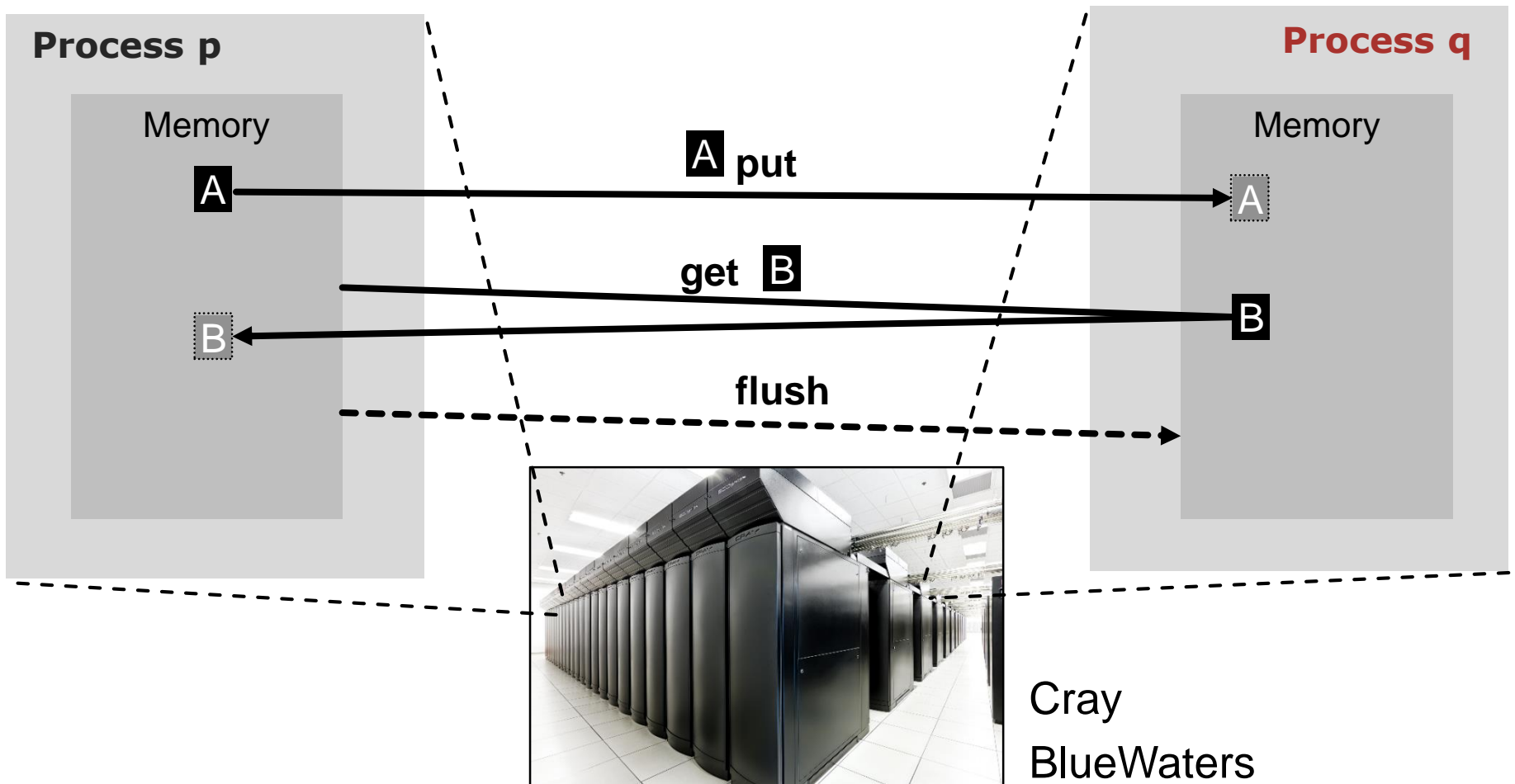


How to ensure tunable performance?



What mechanism to use for efficient implementation?

REMOTE MEMORY ACCESS (RMA) PROGRAMMING



REMOTE MEMORY ACCESS PROGRAMMING

- Implemented in hardware in NICs in the majority of HPC networks support RDMA





How to manage the design complexity?



How to ensure tunable performance?



What mechanism to use for efficient implementation?

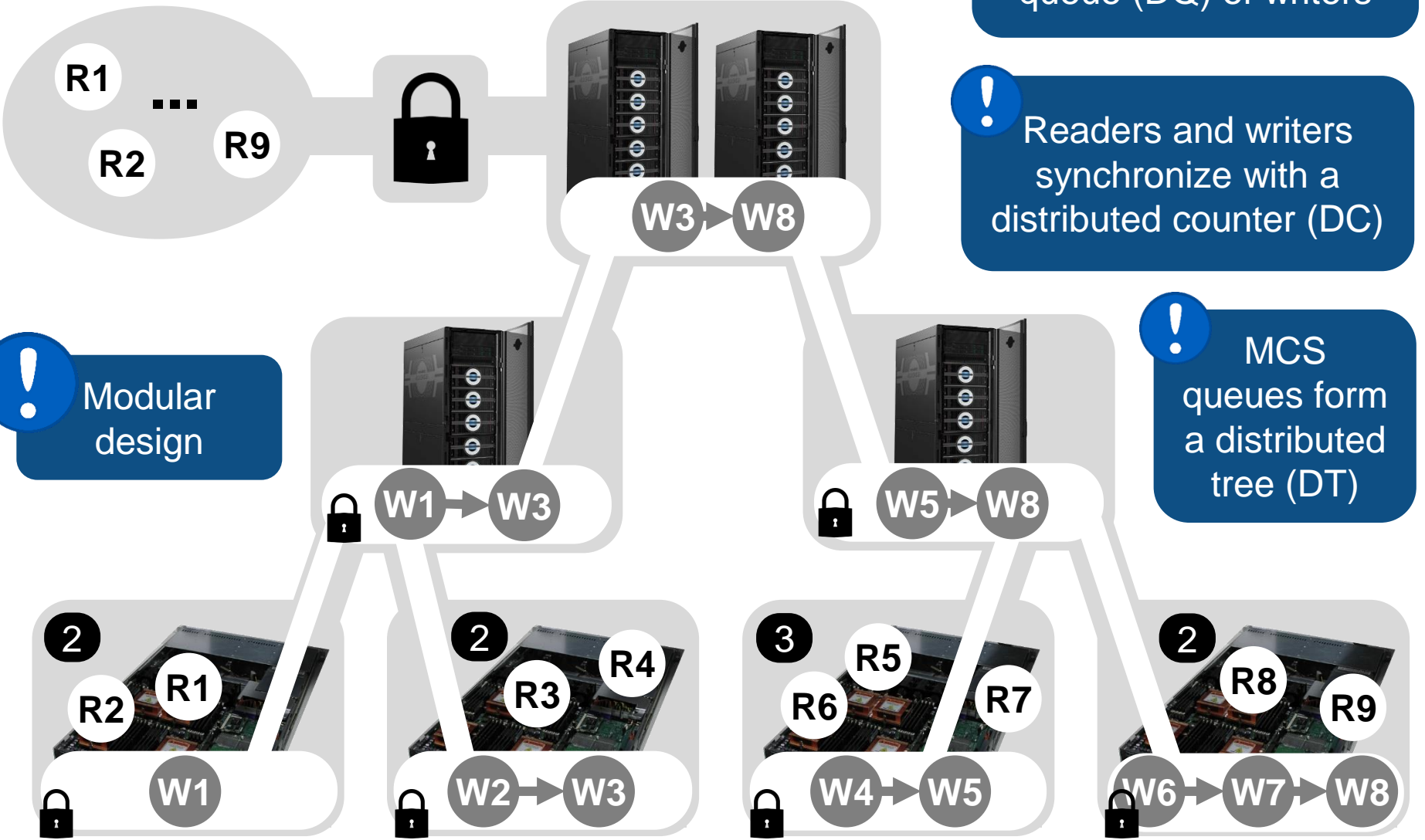
? How to manage the design complexity?

! Each element has its own distributed MCS queue (DQ) of writers

! Readers and writers synchronize with a distributed counter (DC)

! MCS queues form a distributed tree (DT)

! Modular design

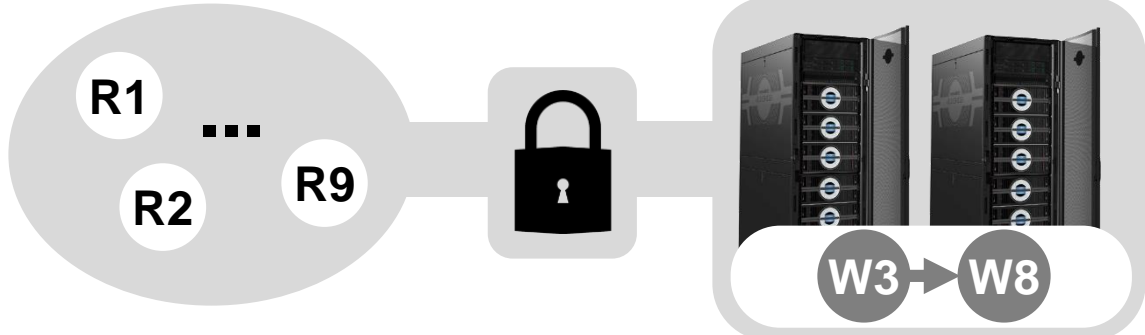


How to ensure tunable performance?

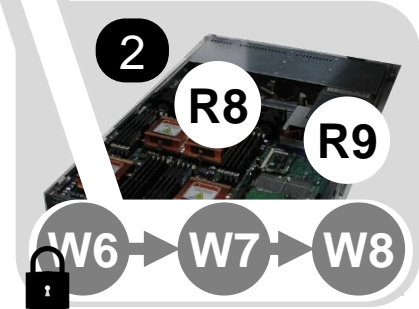
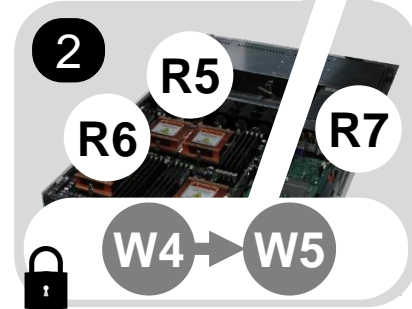
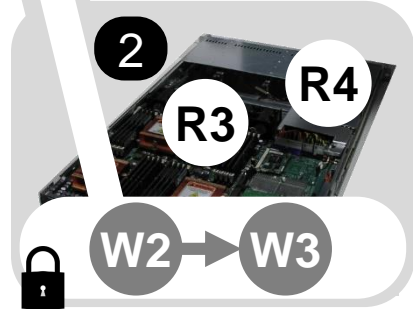
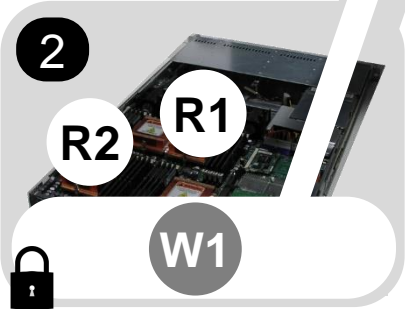
! Each DQ: fairness vs throughput of writers

! DC: a parameter for the latency of readers vs writers

! DT: a parameter for the throughput of readers vs writers



! A tradeoff parameter for every structure



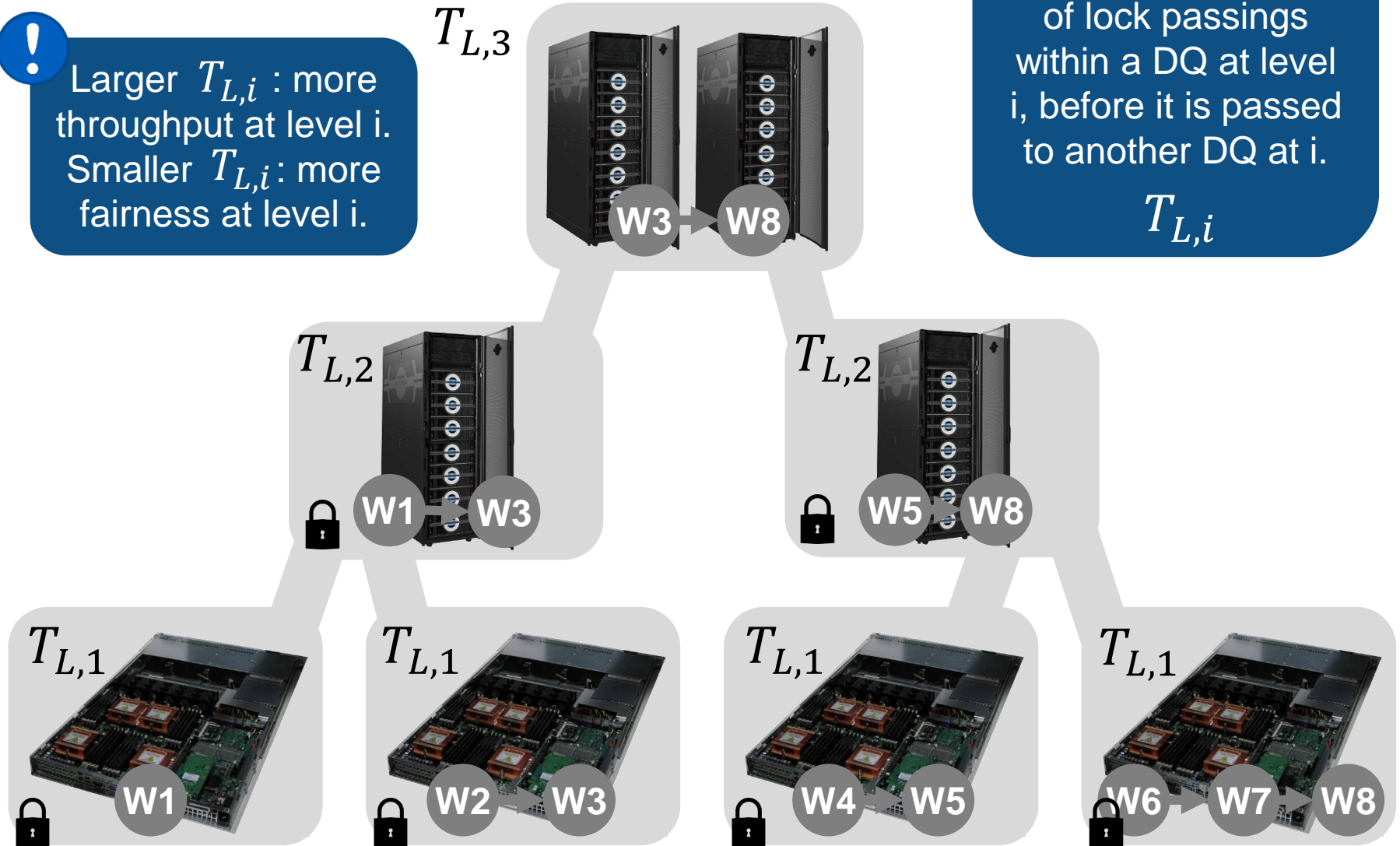
DISTRIBUTED MCS QUEUES (DQs)

Throughput vs Fairness

! Larger $T_{L,i}$: more throughput at level i .
 Smaller $T_{L,i}$: more fairness at level i .

! Each DQ: The maximum number of lock passings within a DQ at level i , before it is passed to another DQ at i .

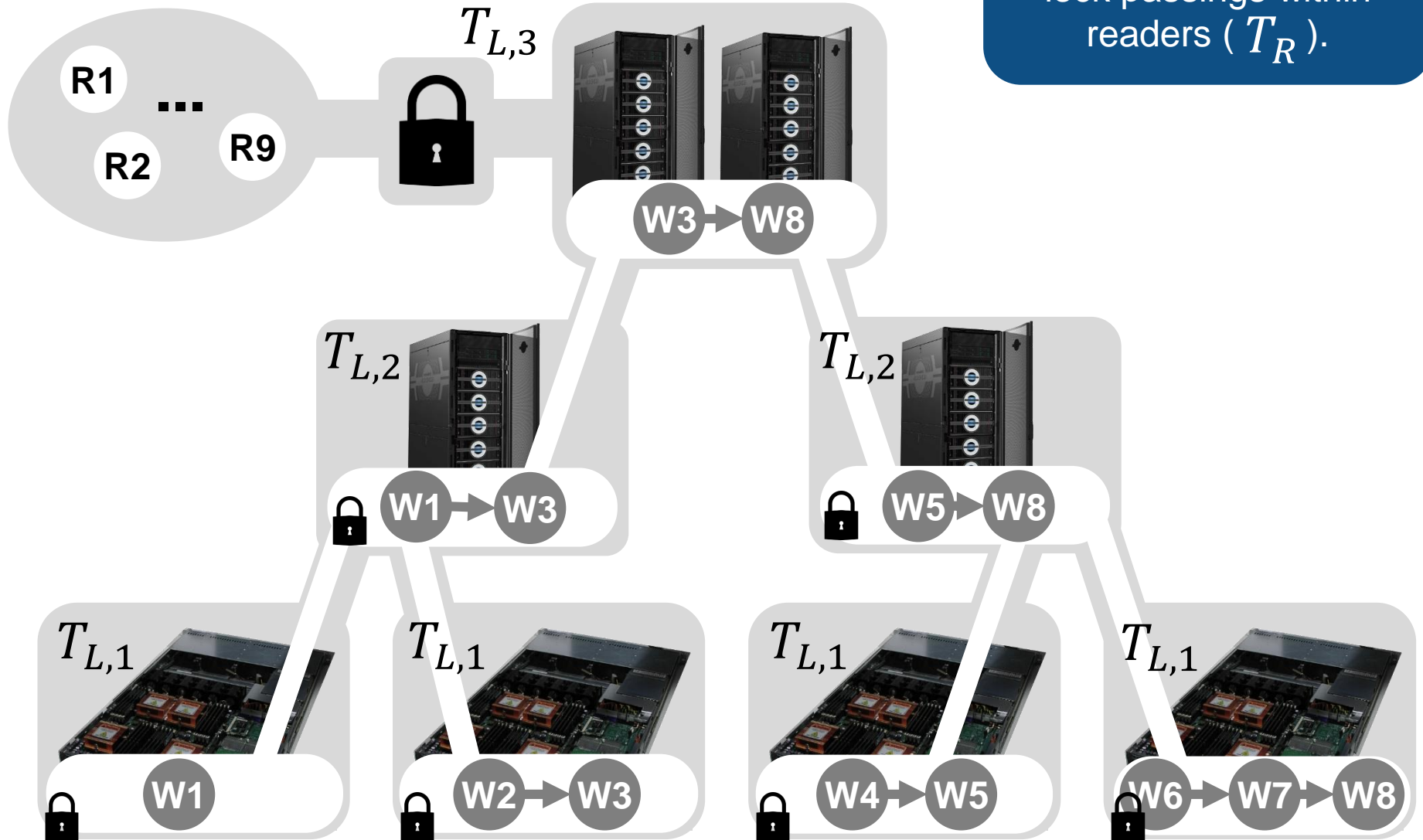
$T_{L,i}$



DISTRIBUTED TREE OF QUEUES (DT)

Throughput of readers vs writers

! DT: The maximum number of consecutive lock passings within readers (T_R).



DISTRIBUTED COUNTER (DC)

Latency of readers vs writers

DC: every k th compute node hosts a partial counter, all of which constitute the DC.

! $k = T_{DC}$



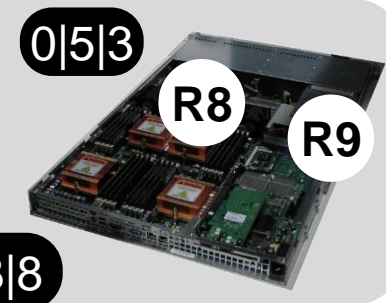
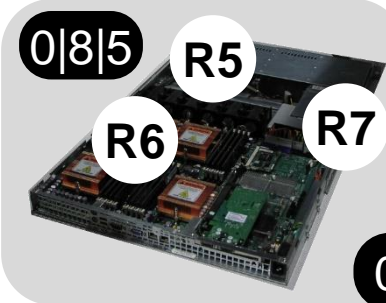
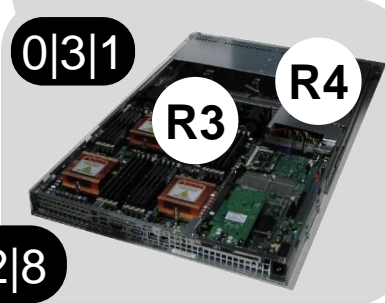
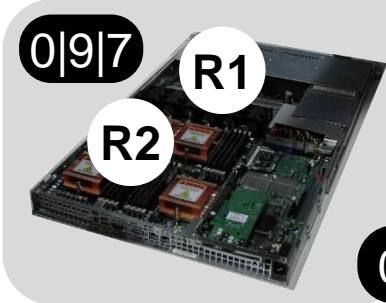
A writer holds the lock $b|x|y$

Readers that arrived at the CS

Readers that left the CS

$T_{DC} = 1$

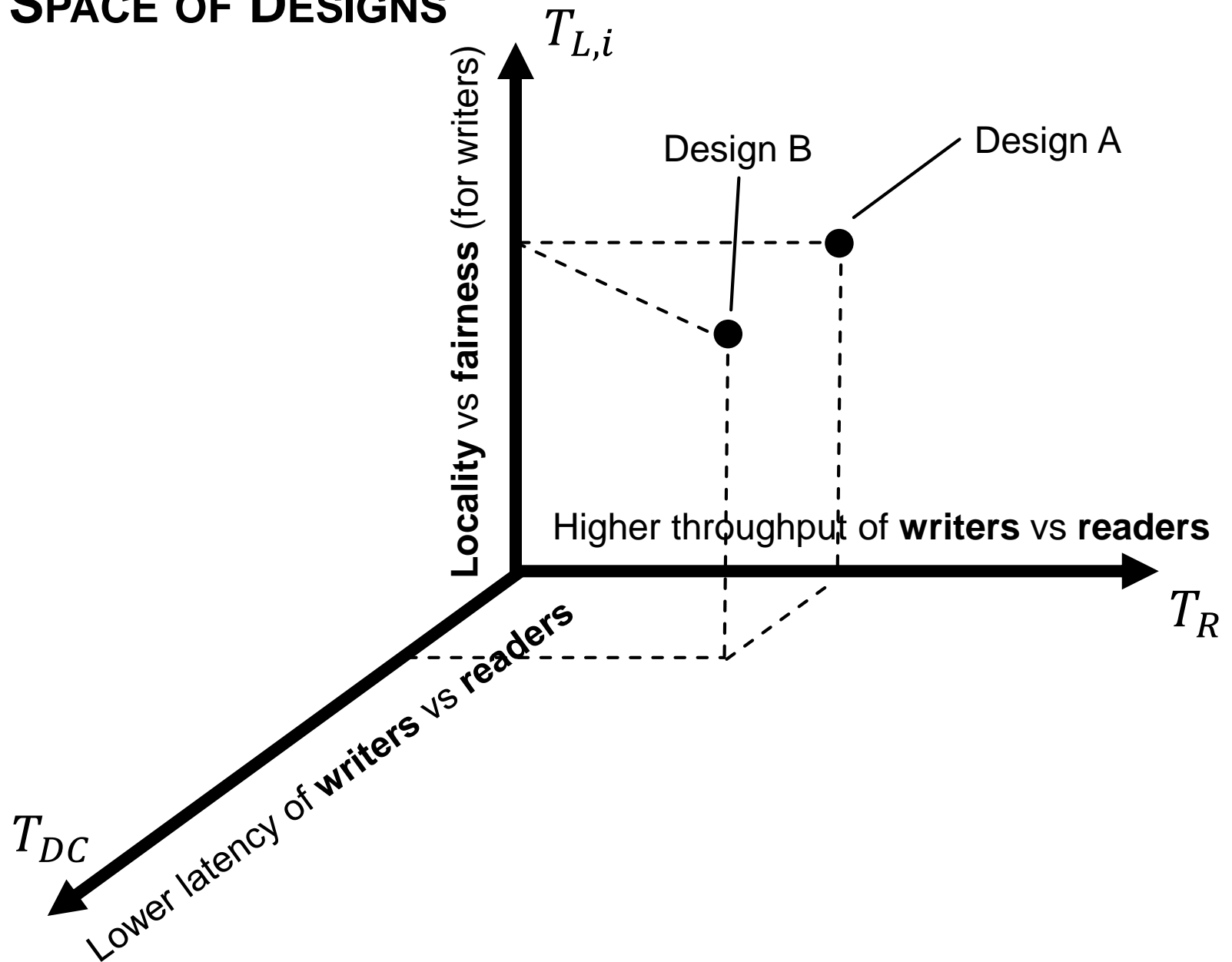
$T_{DC} = 2$



0|12|8

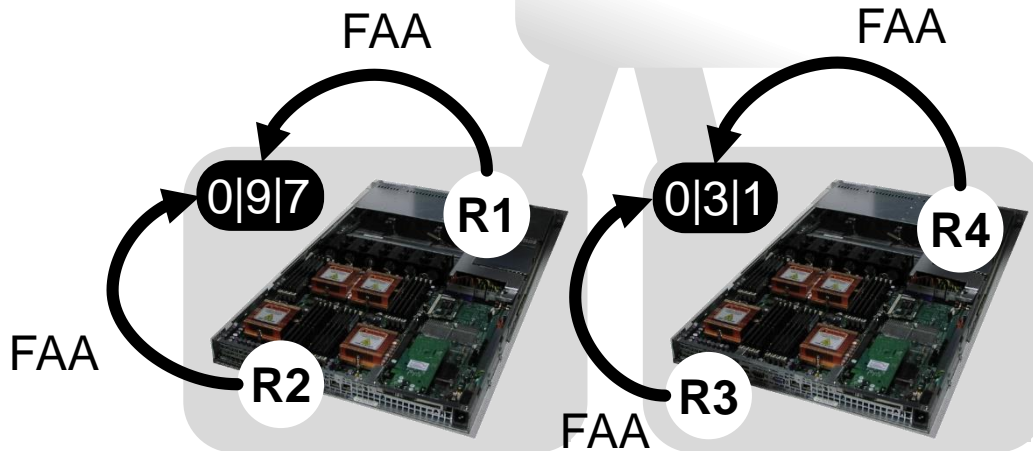
0|13|8

THE SPACE OF DESIGNS



LOCK ACQUIRE BY READERS

! A lightweight acquire protocol for readers: only one atomic fetch-and-add (FAA) operation

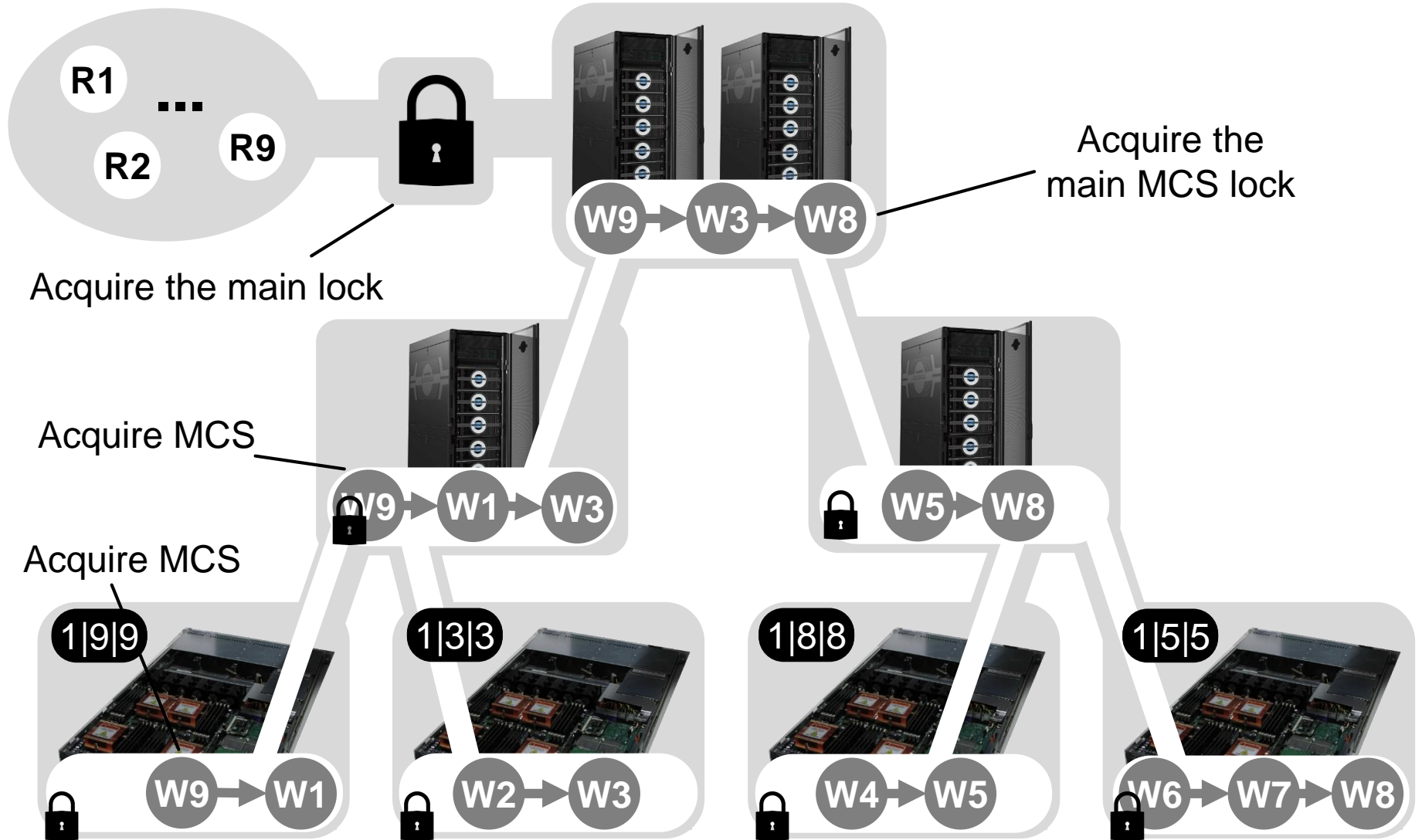


A writer holds the lock — **b|x|y**

Readers that arrived at the CS —

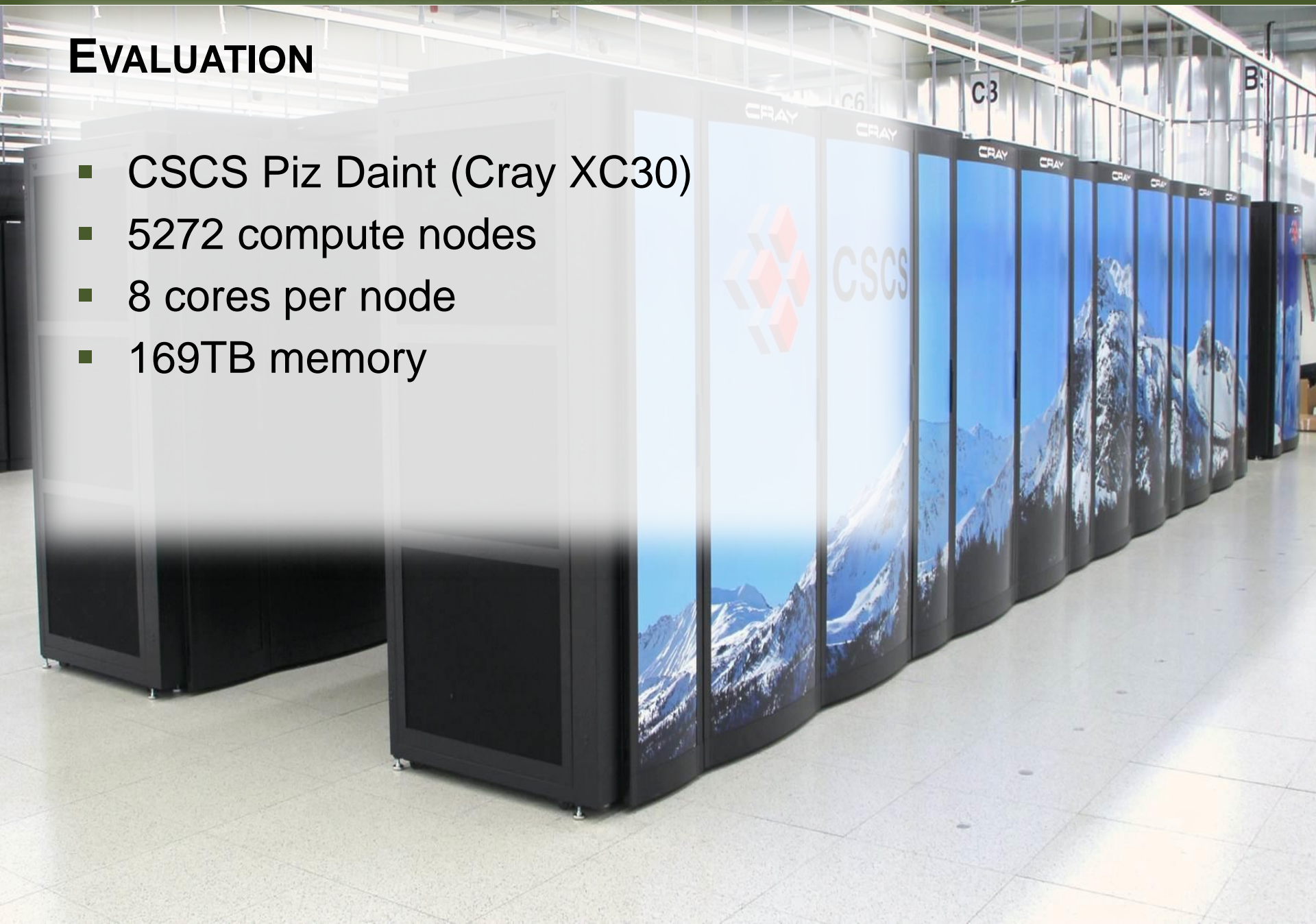
Readers that left the CS —

LOCK ACQUIRE BY WRITERS



EVALUATION

- CSCS Piz Daint (Cray XC30)
- 5272 compute nodes
- 8 cores per node
- 169TB memory



EVALUATION

CONSIDERED BENCHMARKS

The **latency**
benchmark

DHT

Distributed
hashtable
evaluation

Throughput
benchmarks:

Empty-critical-section

Single-operation

Wait-after-release

Workload-critical-section

EVALUATION

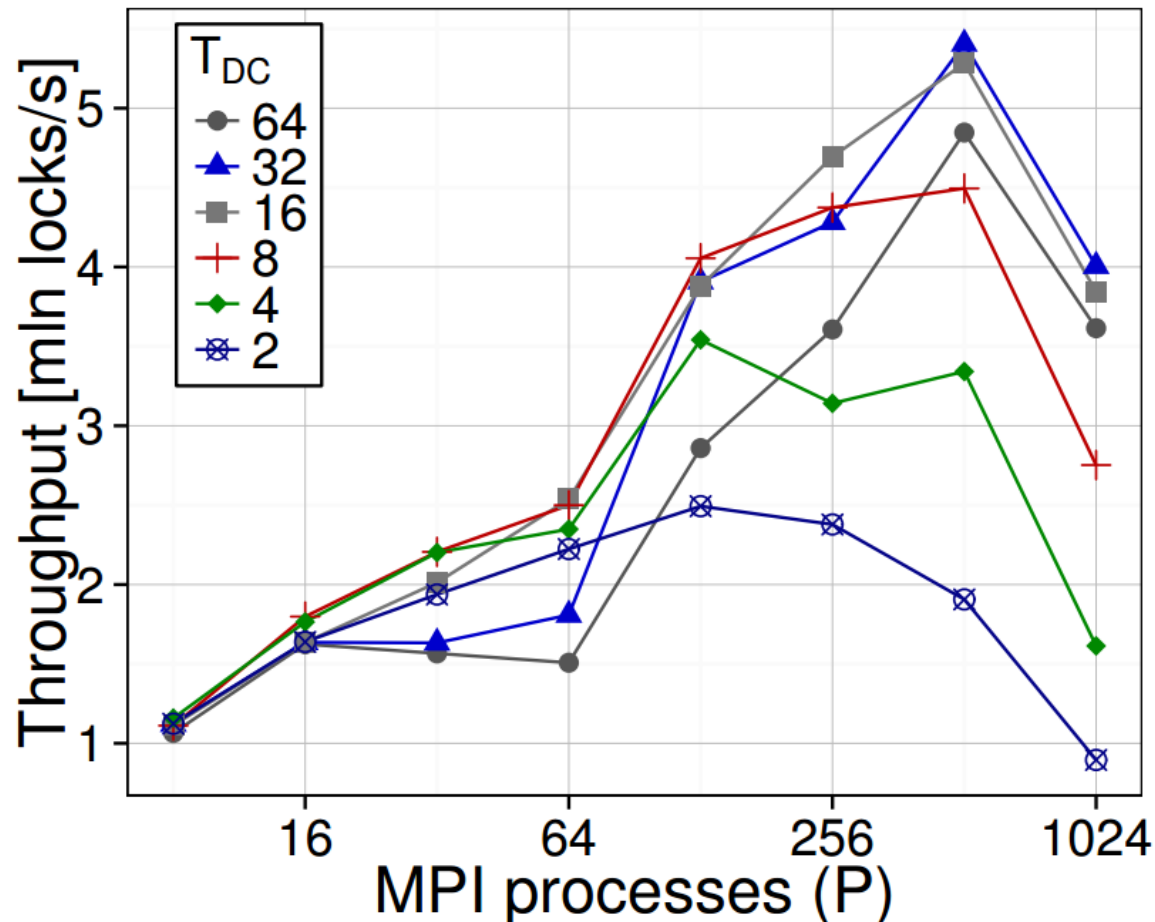
DISTRIBUTED COUNTER ANALYSIS

0|9|7

0|3|1

0|12|8

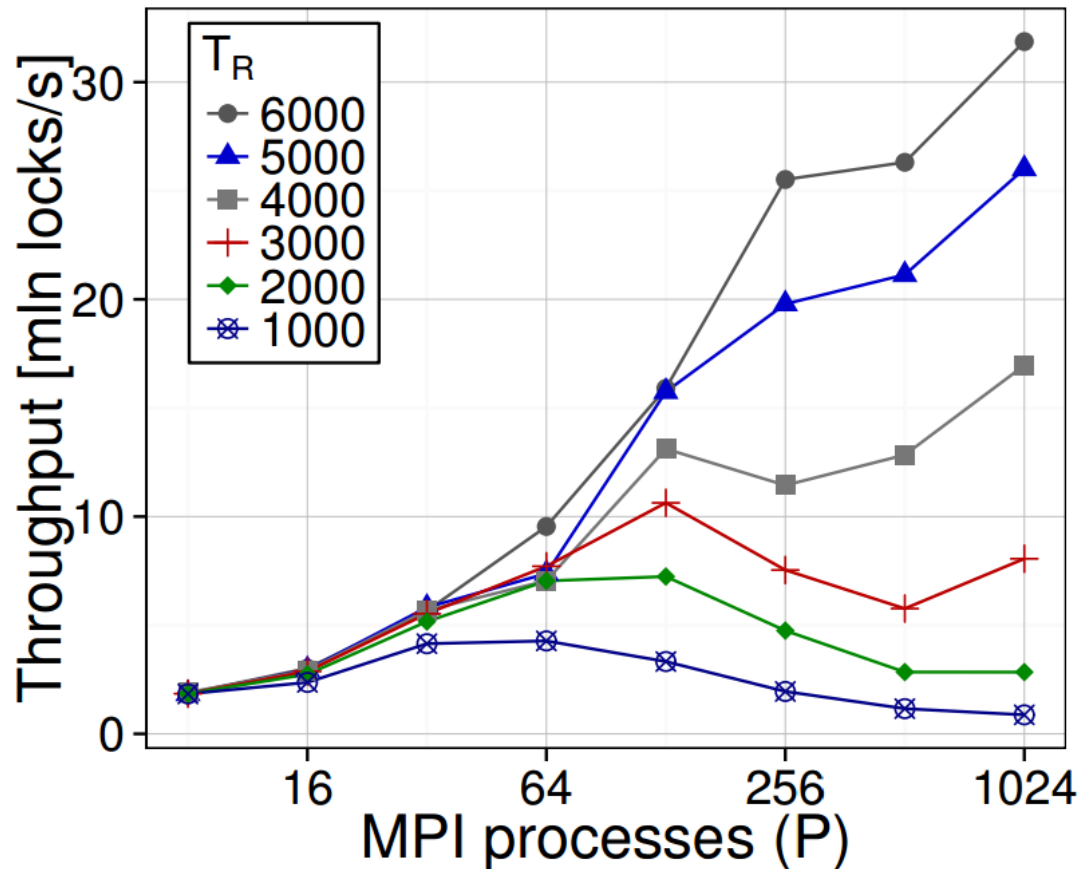
Throughput, 2% writers
Single-operation benchmark



EVALUATION

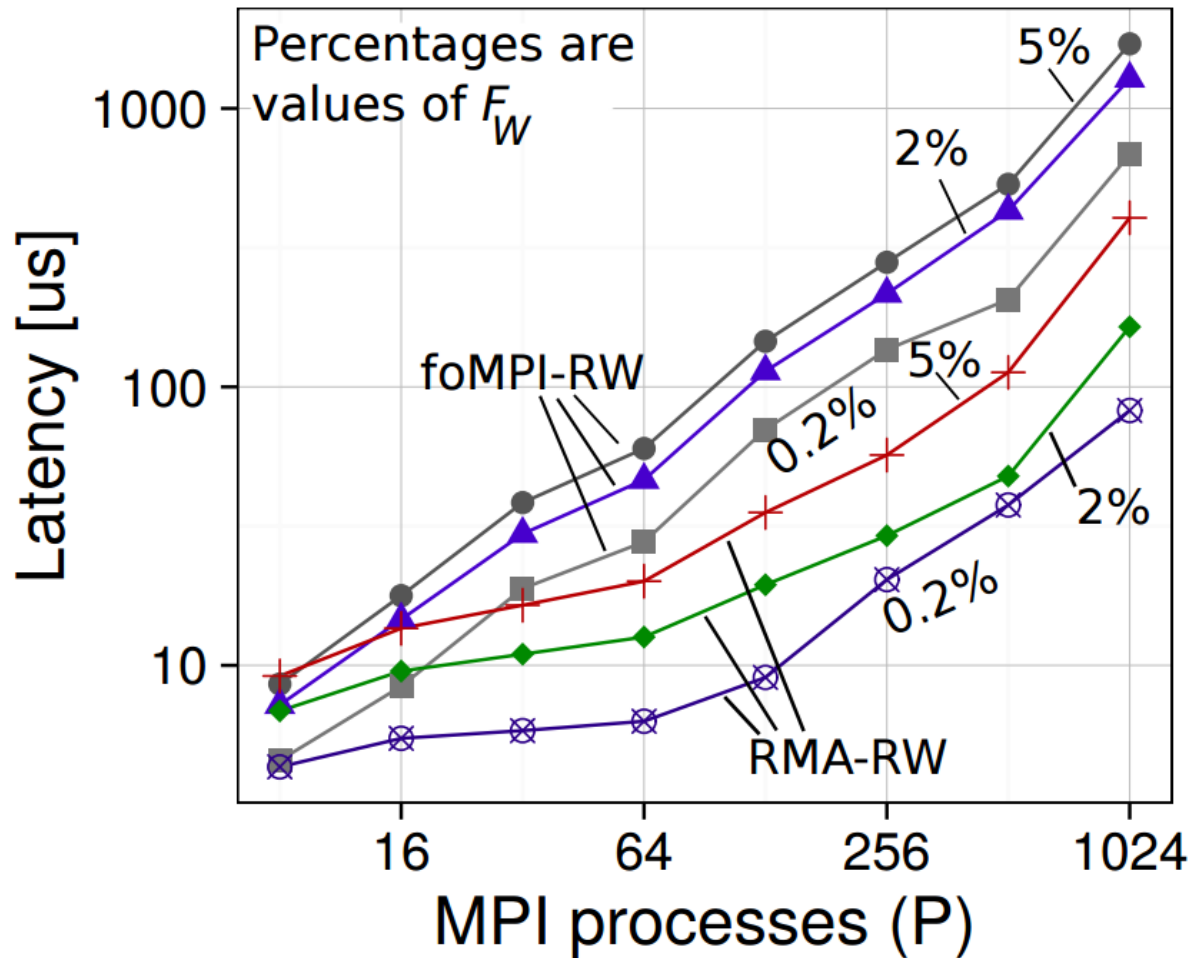
READER THRESHOLD ANALYSIS

Throughput, 0.2% writers,
Empty-critical-section benchmark



EVALUATION

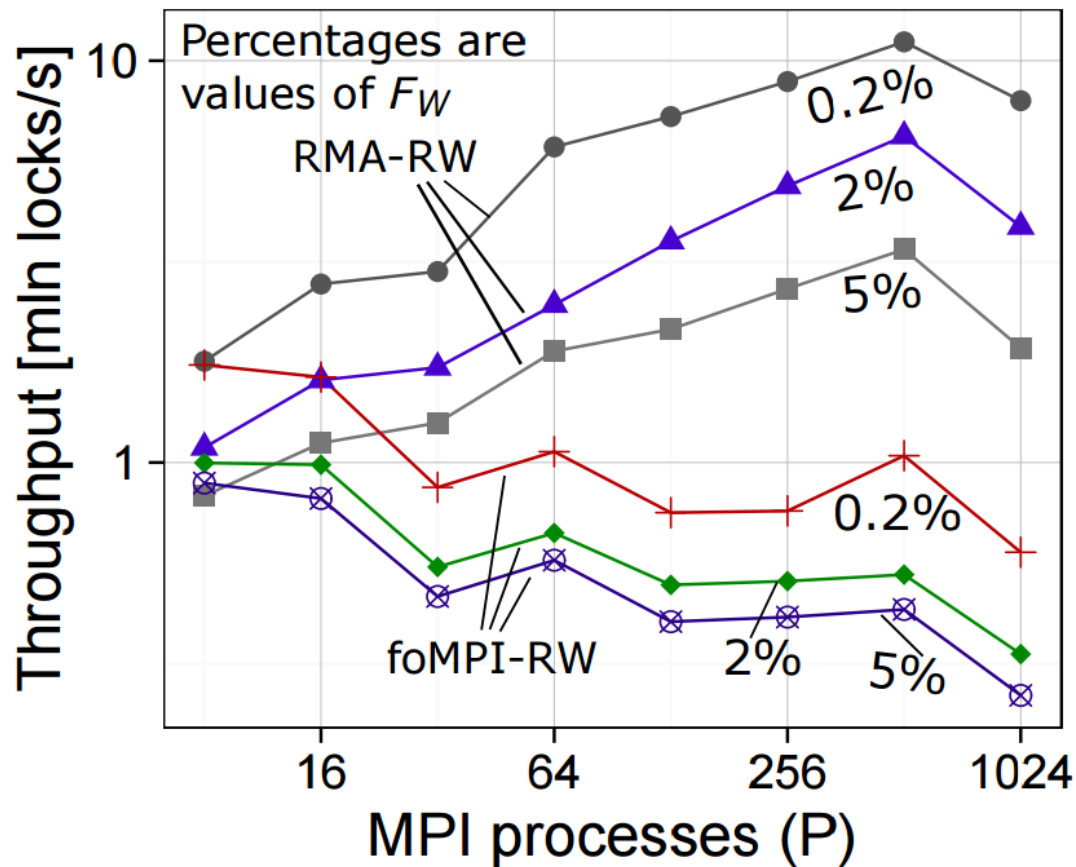
COMPARISON TO THE STATE-OF-THE-ART



EVALUATION

COMPARISON TO THE STATE-OF-THE-ART

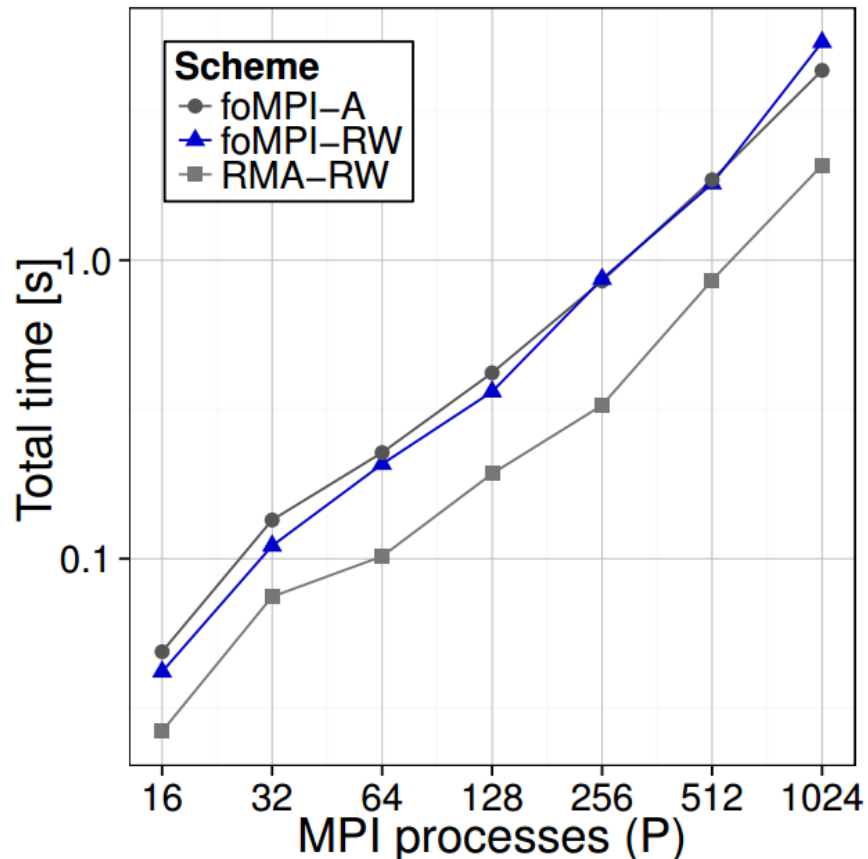
Throughput, single-operation benchmark



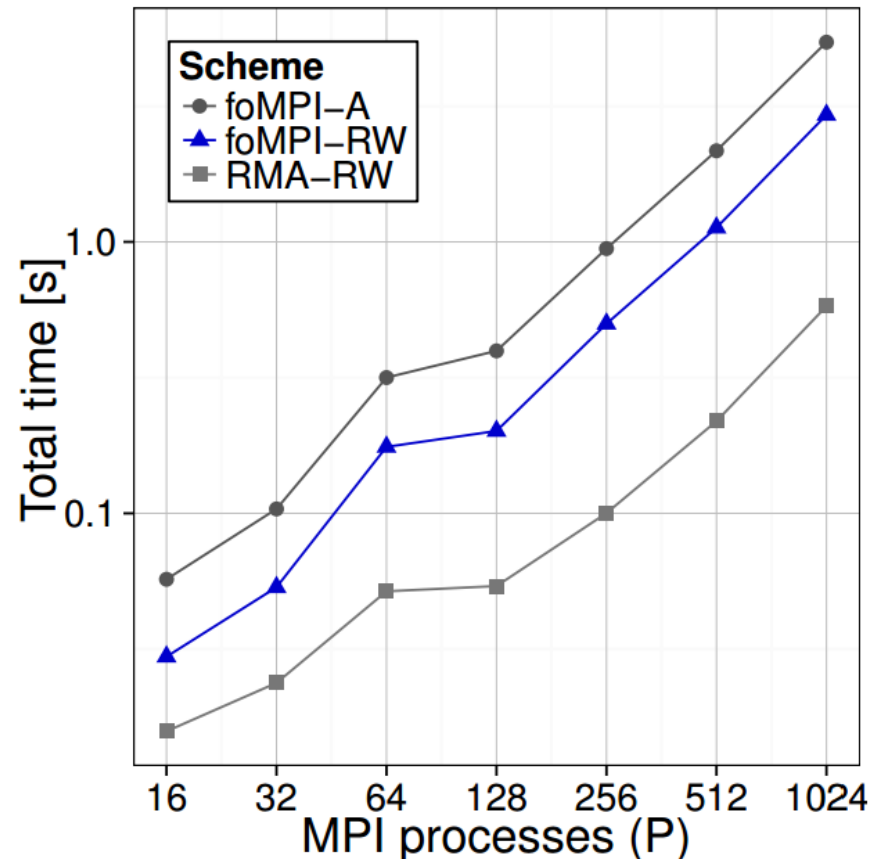
EVALUATION

DISTRIBUTED HASHTABLE

20% writers



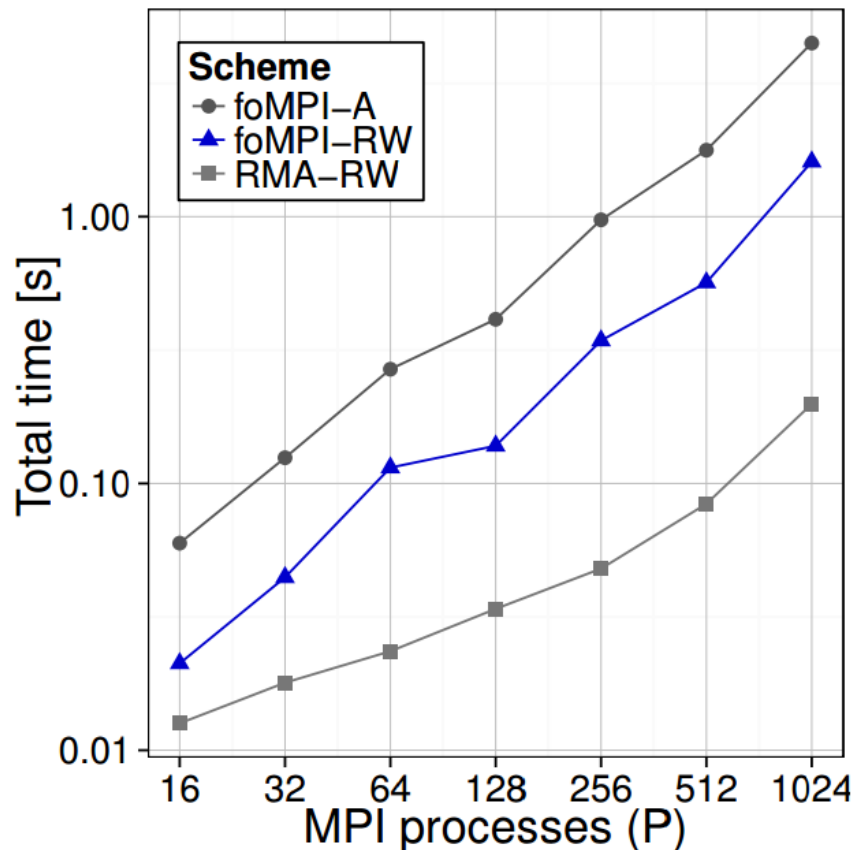
10% writers



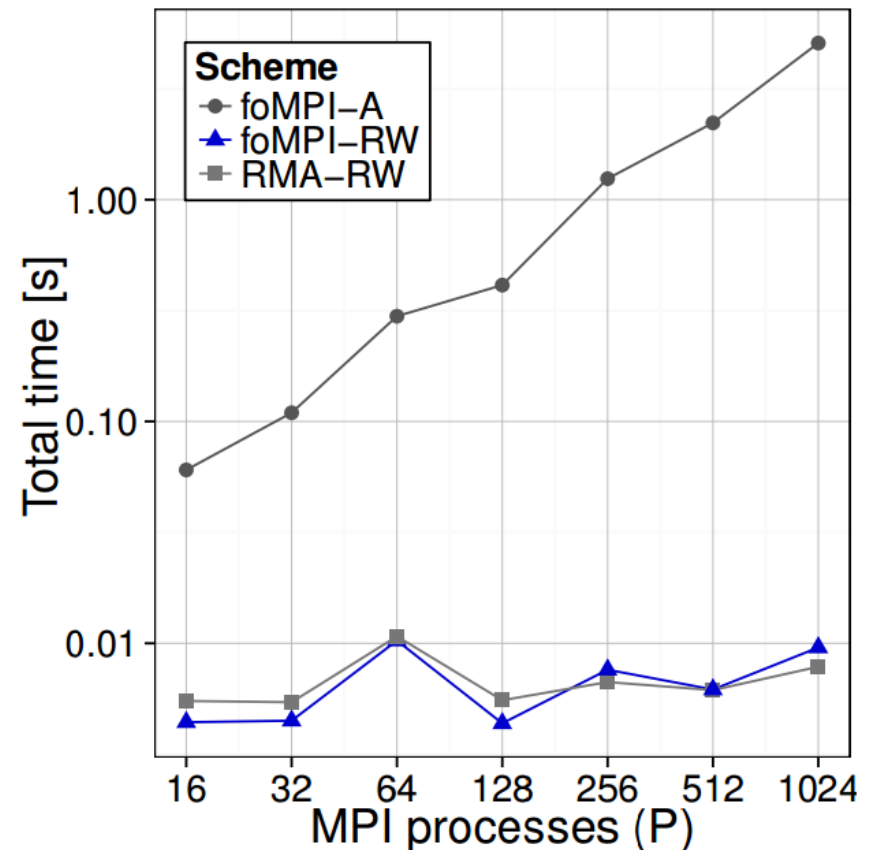
EVALUATION

DISTRIBUTED HASHTABLE

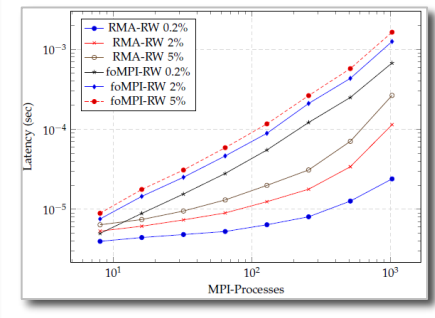
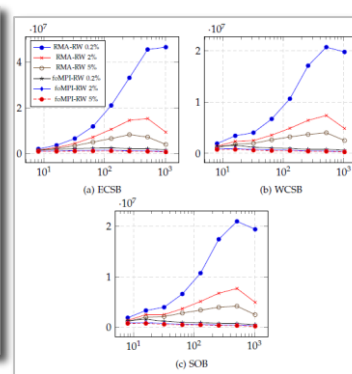
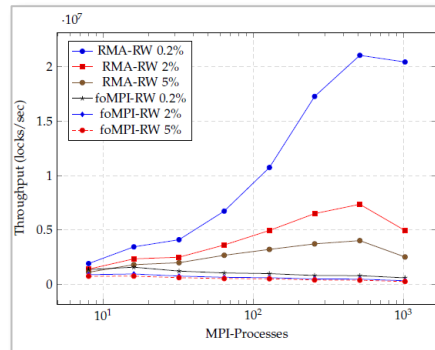
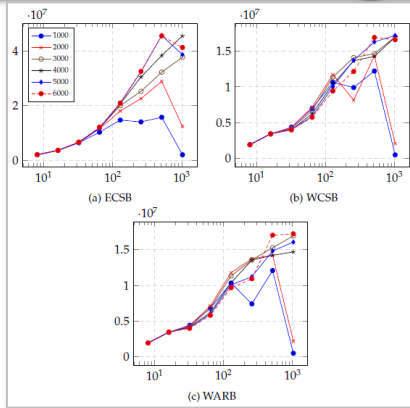
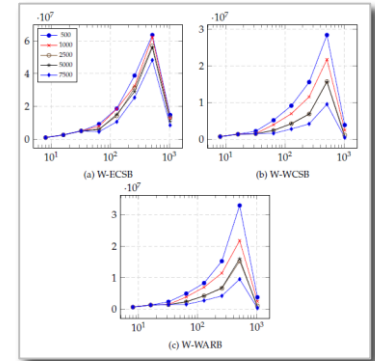
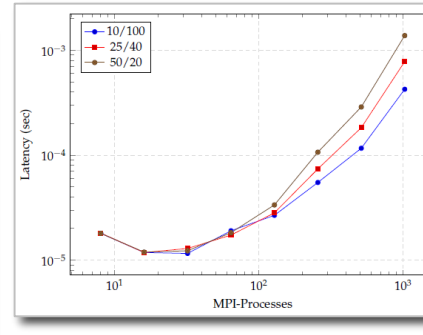
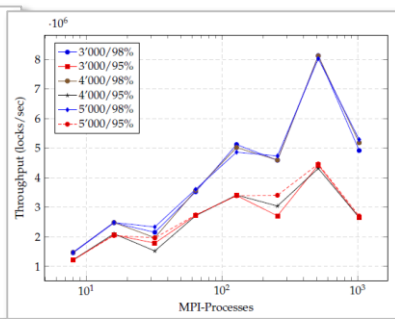
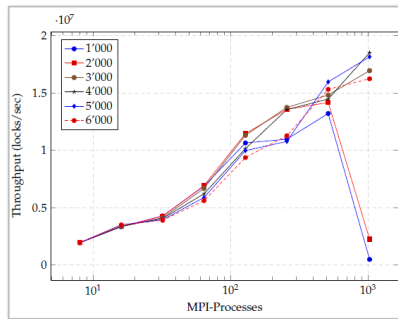
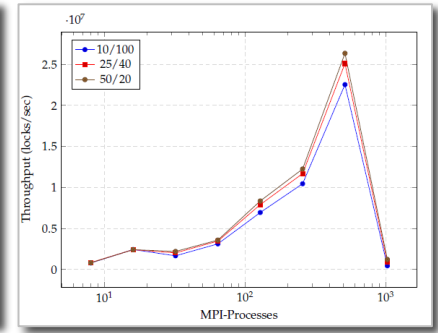
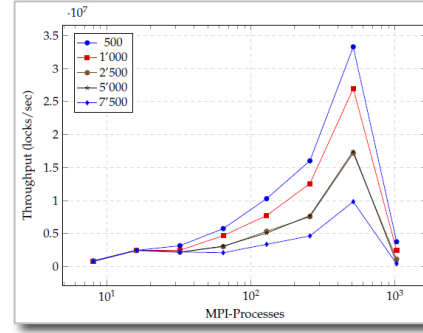
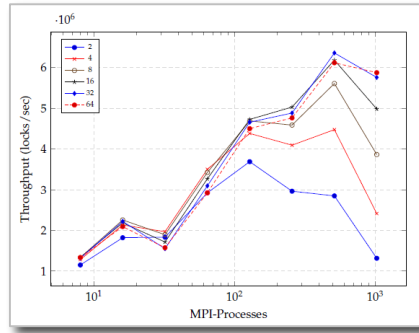
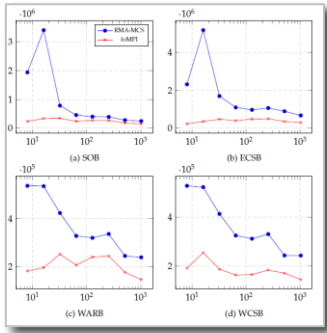
2% of writers



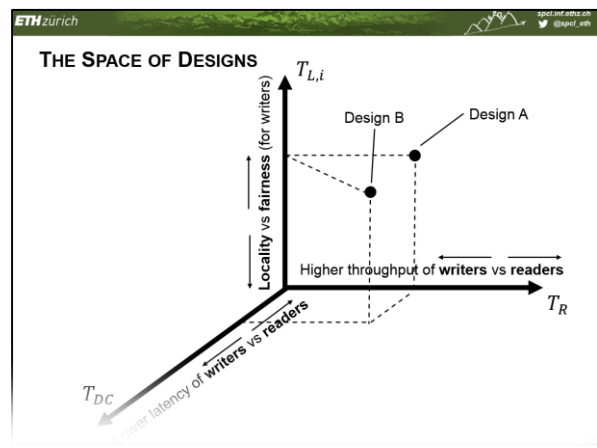
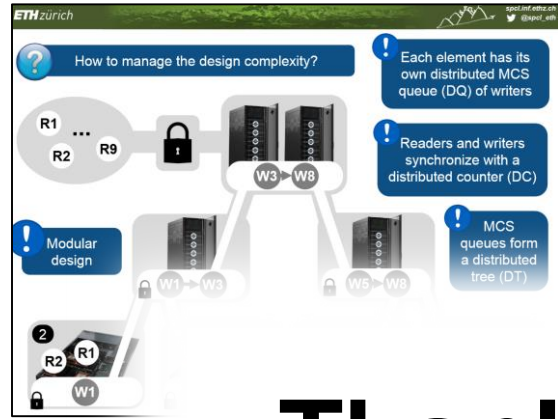
0% of writers



OTHER ANALYSES



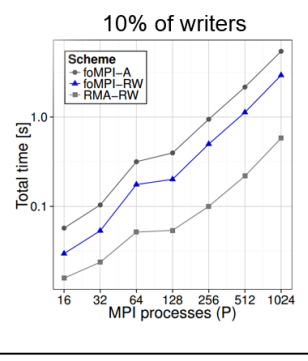
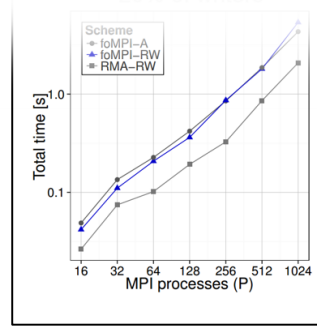
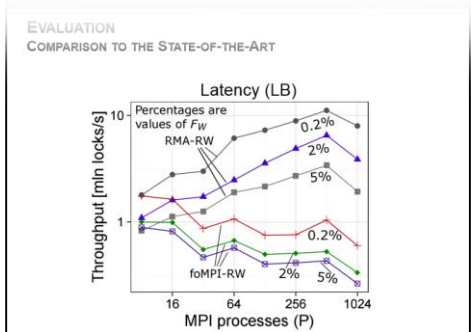
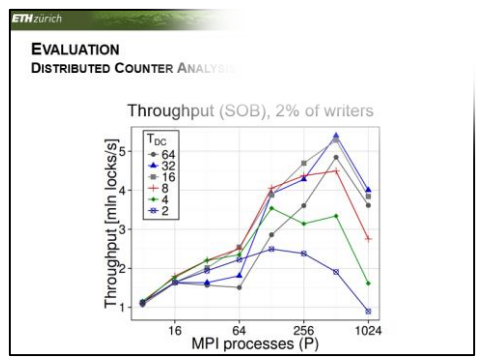
CONCLUSIONS



Thank you for your attention

Modular design
correct

able
ges

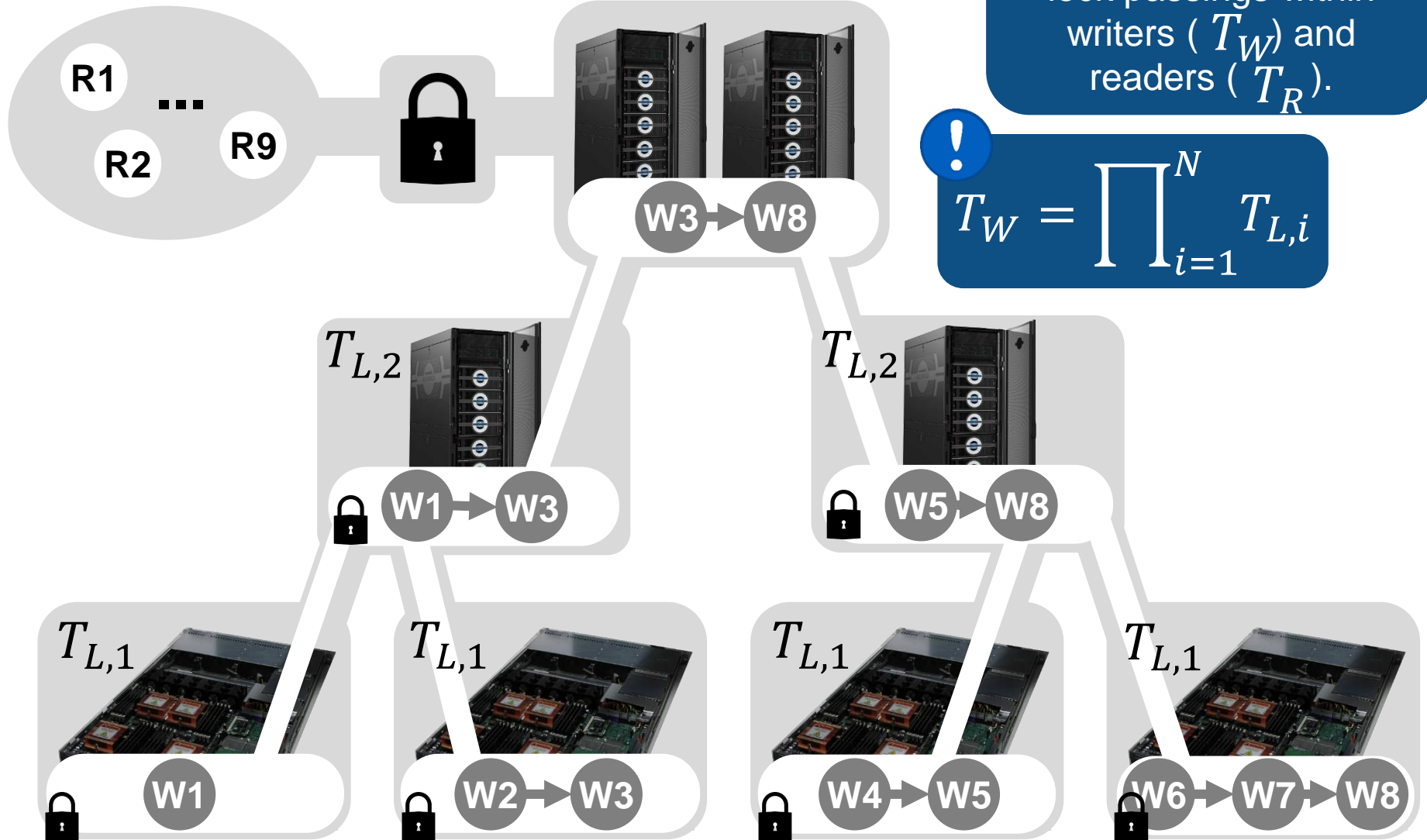


Improves latency and throughput over state-of-the-art

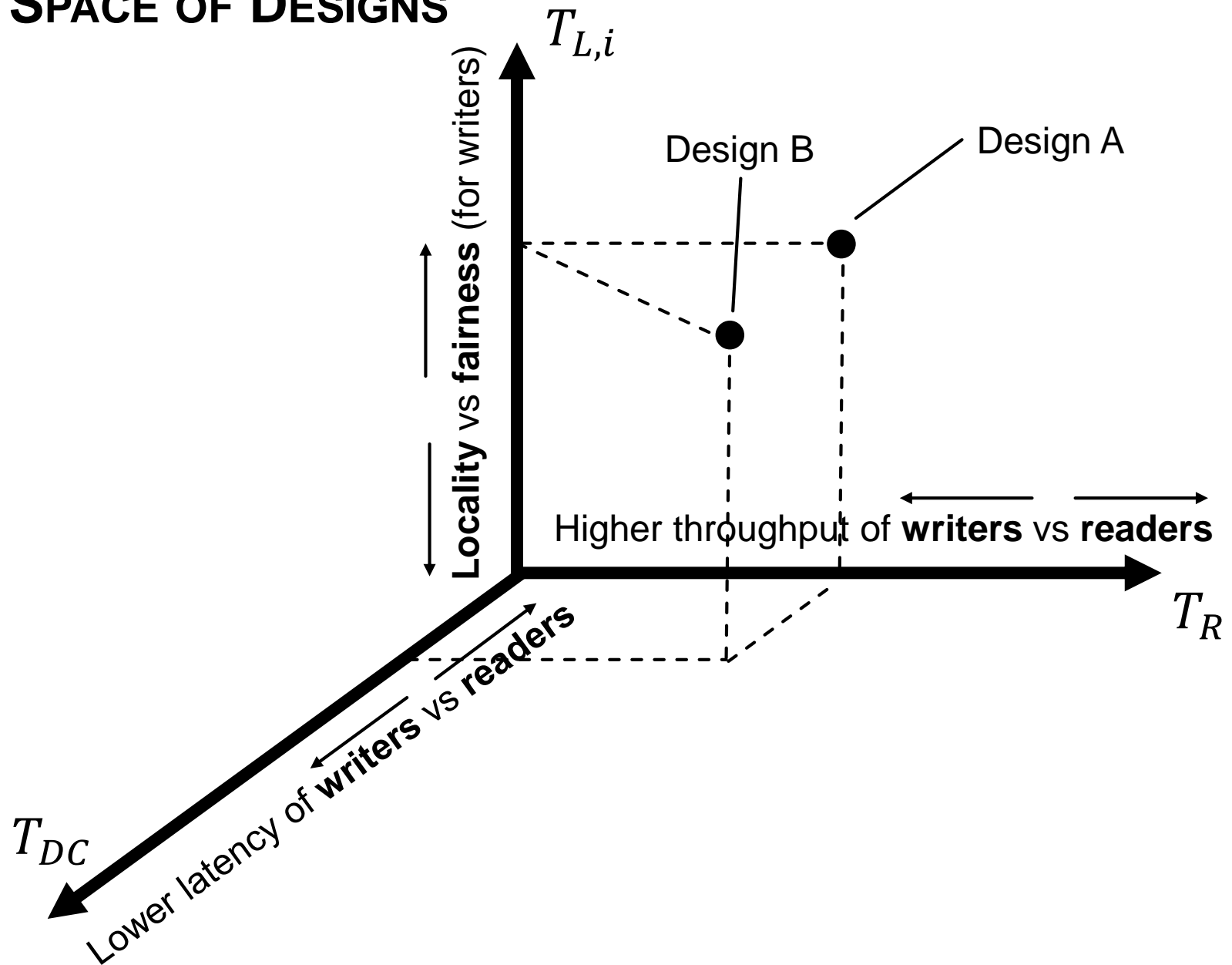
Enables high-performance distributed hashtable

DISTRIBUTED TREE OF QUEUES (DT)

Throughput of readers vs writers



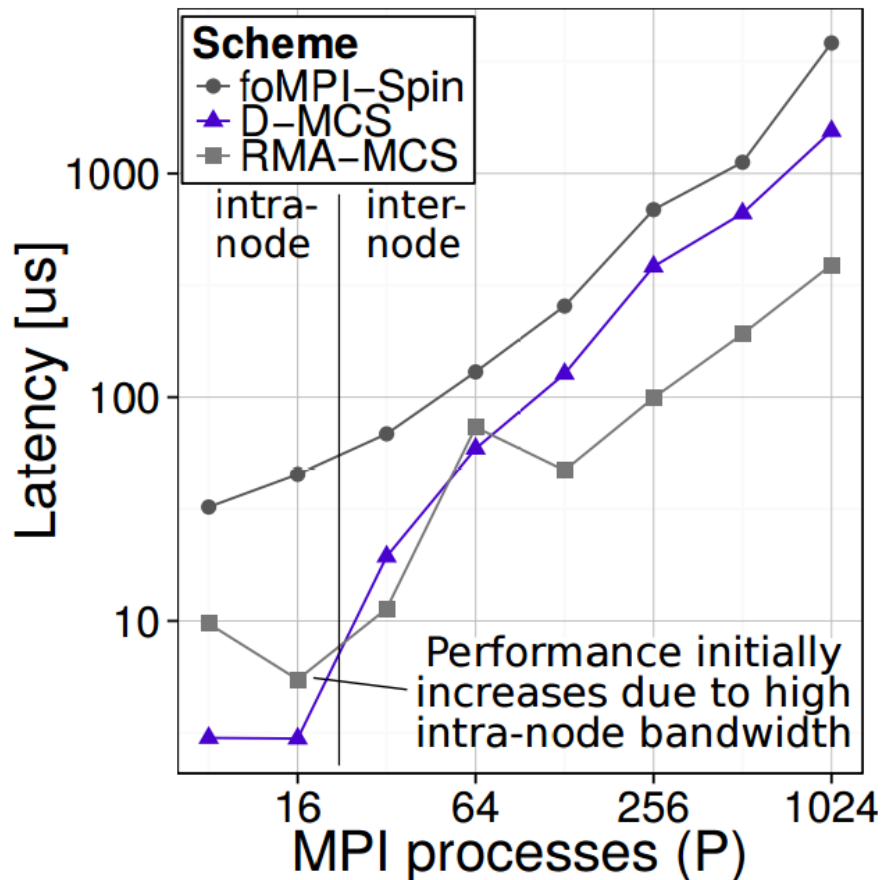
THE SPACE OF DESIGNS



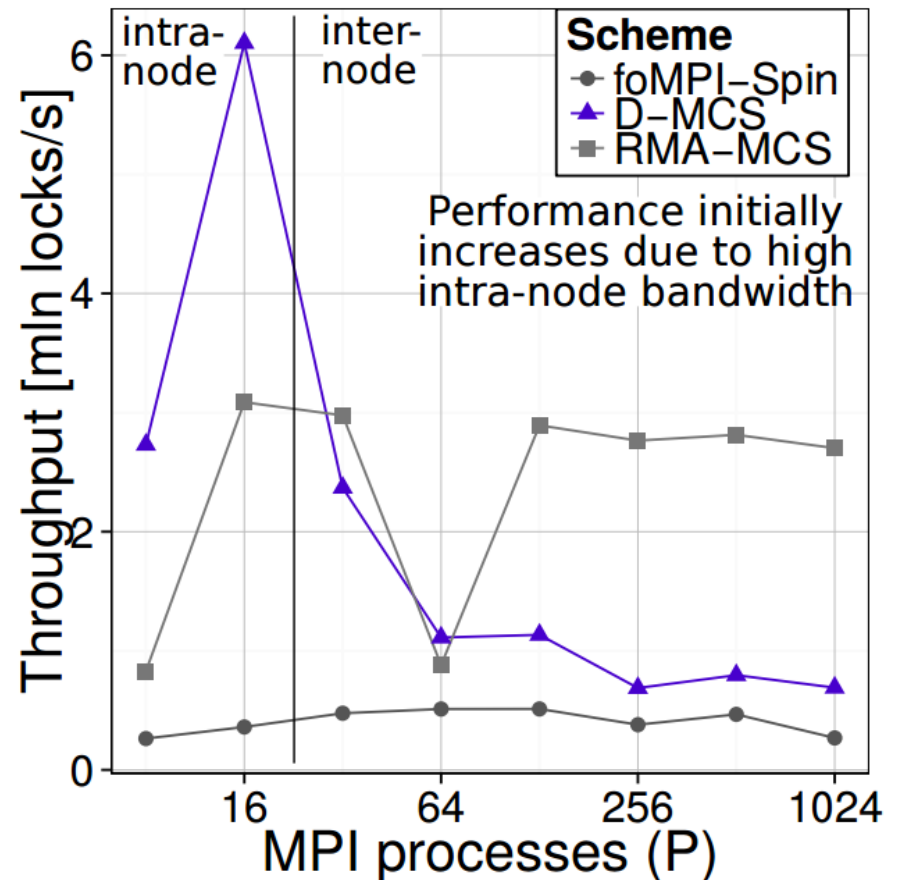
EVALUATION

D-MCS VS OTHERS

Latency (LB)



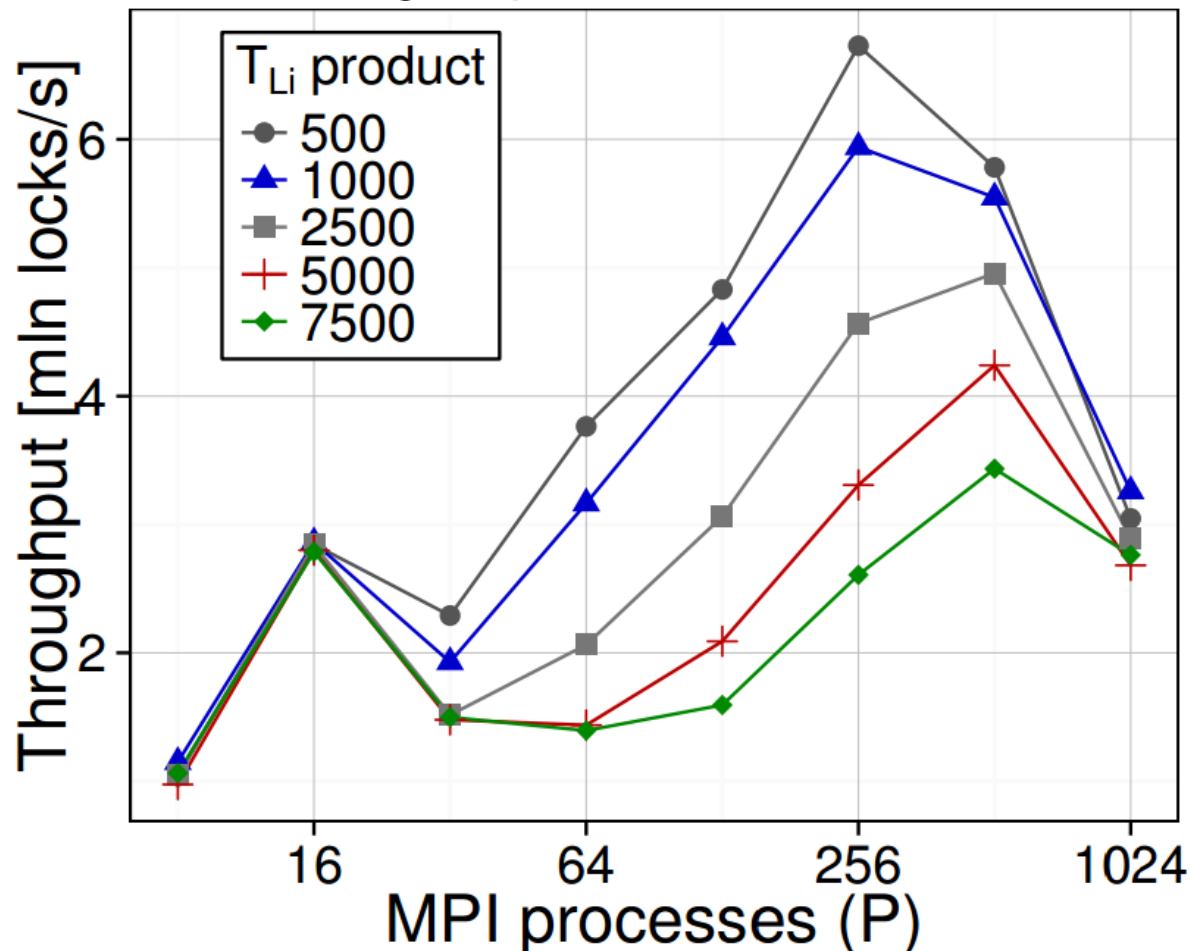
Throughput (ECSB)



EVALUATION

WRITER THRESHOLD ANALYSIS

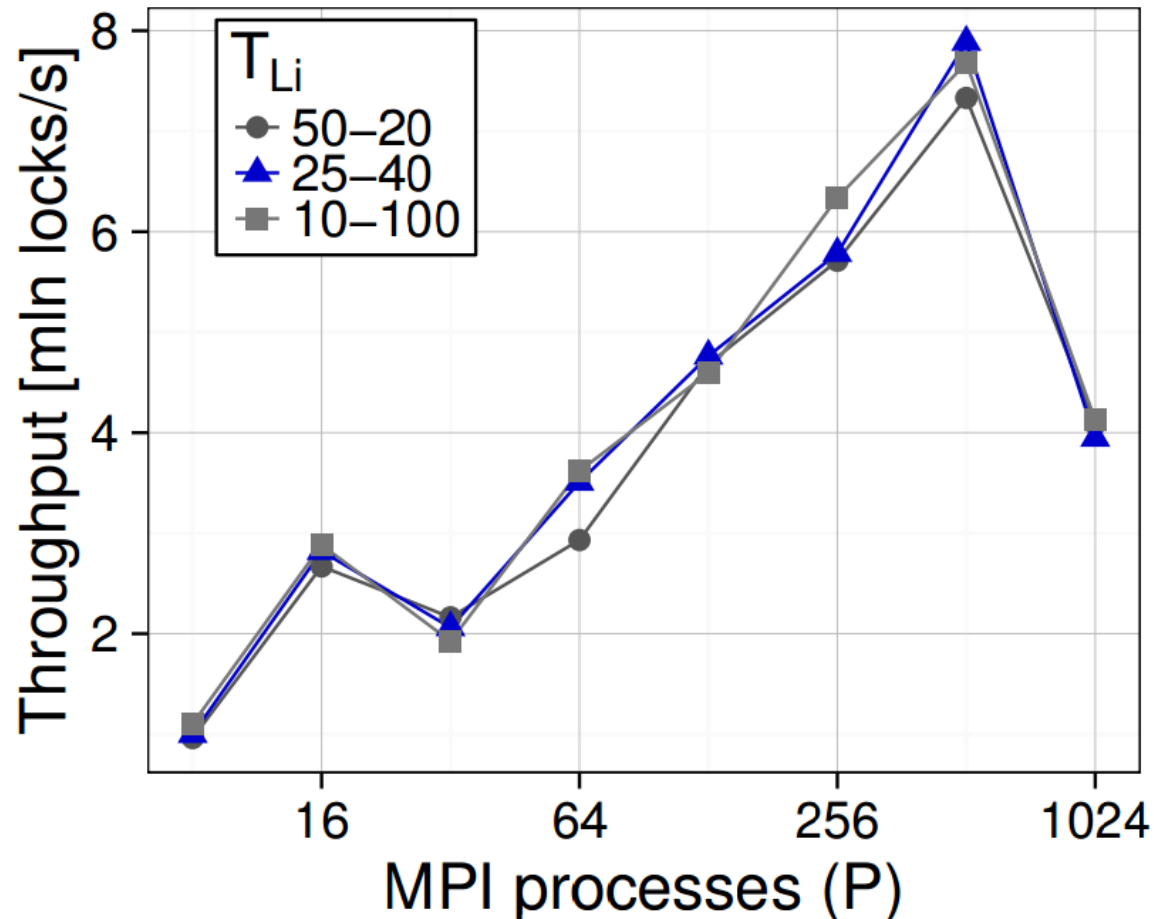
Throughput, 25% of writers
Single-operation benchmark



EVALUATION

FAIRNESS VS THROUGHPUT ANALYSIS

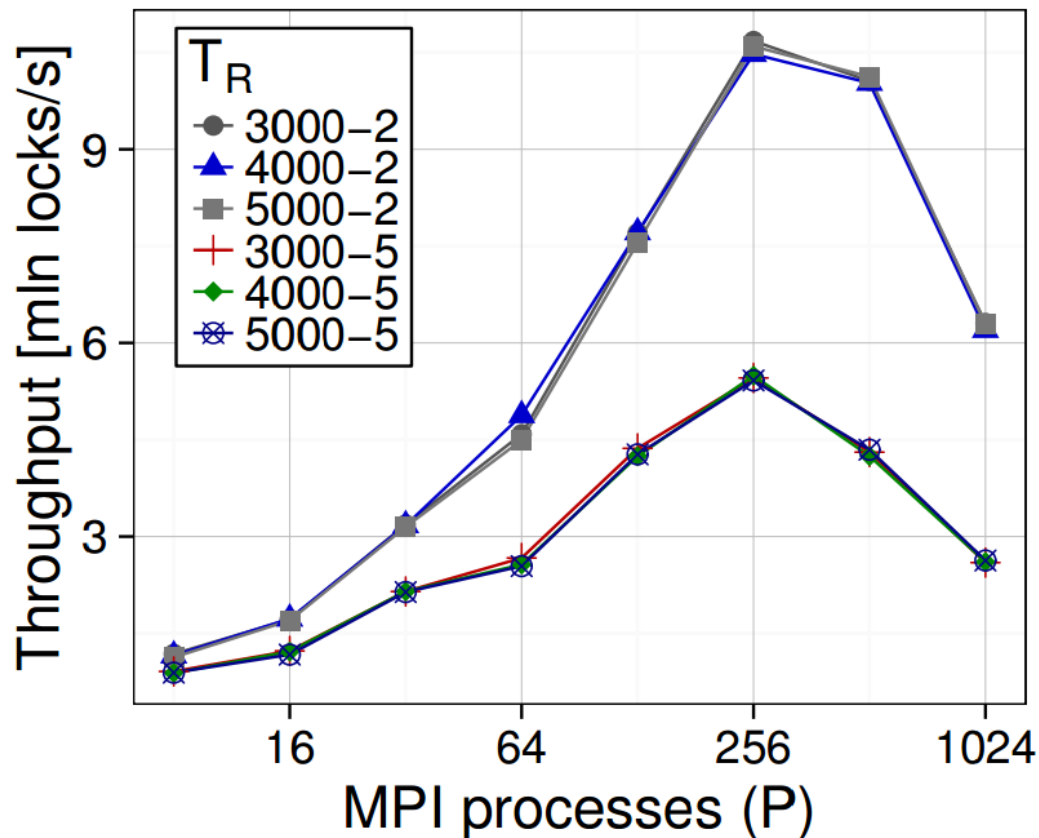
Throughput, 25% of writers,
Single-operation benchmark



EVALUATION

READER THRESHOLD ANALYSIS

Throughput, 2% and 5% writers,
Empty-critical-section benchmark



FEASIBILITY ANALYSIS

	UPC (standard) [44]	Berkeley UPC [1]	SHMEM [4]
Put	UPC_SET	bupc_atomicX_set_RS	shmem_swap
Get	UPC_GET	bupc_atomicX_read_RS	shmem_mswap
Accumulate	UPC_INC	bupc_atomicX_fetchadd_RS	shmem_fadd
FAO (SUM)	UPC_INC, UPC_DEC	bupc_atomicX_fetchadd_RS	shmem_fadd
FAO (REPLACE)	UPC_SET	bupc_atomicX_swap_RS	shmem_swap
CAS	UPC_CSWAP	bupc_atomicX_cswap_RS	shmem_cswap

	Fortran 2008 [27]	Linux RDMA/IB [33, 43]	iWARP [18, 41]
Put	atomic_define	MskCmpSwap	masked CmpSwap
Get	atomic_ref	MskCmpSwap	masked CmpSwap
Accumulate	atomic_add	FetchAdd	FetchAdd
FAO (SUM)	atomic_add	FetchAdd	FetchAdd
FAO (REPLACE)	atomic_define*	MskCmpSwap	masked CmpSwap
CAS	atomic_cas	CmpSwap	CmpSwap