TORSTEN HOEFLER
Remote Memory Access Programming: Faster Parallel Computing Without Messages
with S. Ramos, R. Gerstenberger, M. Besta, R. Belli @ SPCL
presented at Tsinghua University, Beijing, China, November 2015

Founded 1855
- to support the industrialization of Switzerland

Top-20 general, Top-10 Computer Science

HPC at CSCS
- part of ETH

Piz Daint
5272 compute nodes
Xeon E5 + K20X
7.78 PF peak

18k students, 466 professors, 1.5 B budget

Swiss HPC Community
- PASC

PASC16
Platform for Advanced Scientific Computing Conference
Lausanne, Switzerland 08-10 June 2016
Scientific Benchmarking of Parallel Computing Systems, SC15
Motivation & Goals

- My dream: provably optimal performance (time and energy)
  - From problem to machine code
  - How to get there?

- Model-based Performance Engineering!
  1. Design a system model
  2. Define your problem
  3. Find (close-to) optimal solution in model → prove
  4. Implement, test, refine if necessary

- Will demonstrate techniques & insights
  - And obstacles 😊
  - RMA as a solution?
Example: Message Passing, Log(G)P

A PRACTICAL MODEL OF PARALLEL COMPUTATION

Our goal is to develop a model of parallel computation that will serve as a basis for the design and analysis of fast, portable parallel algorithms, such as algorithms that can be implemented effectively on a wide variety of current and future parallel machines. If we look at the body of parallel algorithms developed under current parallel models, many are impractical because they exploit artificial factors not present in any real-world parallel model. PRAM consists of a collection of processors which compute synchronously in parallel and communicate with a global random access memory.

Hardware Reality

Interlagos, 8/16 cores, source: AMD

POWER 7, 8 cores, source: IBM

Xeon Phi, 64 cores, source: Intel
Hardware Reality

Interlagos, 8/16 cores, source: AMD

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Kepler GPU, source: NVIDIA

InfiniBand, sources: Intel, Mellanox

BG/Q, Cray Aries, sources: IBM, Cray
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Example: Cache-Coherent Communication

Xeon Phi (Rough) Architecture
Invalid read $R_I = 278$ ns
Local read: $R_L = 8.6$ ns
Remote read $R_R = 235$ ns

*Inspired by Molka et al.: “Memory performance and cache coherency effects on an Intel Nehalem multiprocessor system”*
DTD Contention

- **E state:**
  - $a=0\text{ns}$
  - $b=320\text{ns}$
  - $c=56.2\text{ns}$

\[
\mathcal{T}_C(n_{th}) = c \cdot n_{th} + b - \frac{a}{n_{th}}
\]
Designing Broadcast Algorithms

- Assume single cache line → forms a Tree
  - We choose d levels and k_j children in level j
  - Reachable threads: \( n_{th} \leq 1 + \sum_{i=1}^{d} \prod_{j=1}^{i} k_j \)
  - Example: d=2, k_1=3, k_2=2:

![Diagram of a tree with nodes labeled 0 to 9, illustrating the broadcast algorithm.]

- \( t_0 = 0 \)
- \( t_1 = k_1^*c + b \)
- \( t_2 = t_1 + k_2^*c + b \)

\[ T_{tree} = \sum_{i=1}^{d} T_C(k_i) = \sum_{i=1}^{d} (c \cdot k_i + b) \]
\[ = \sum_{i=1}^{d} (R_R + R_L + c \cdot (k_i - 1)) \]

\( c = \) DTD contention
\( b = \) transmit latency
Finding the Optimal Broadcast Algorithm

- Broadcast example:

\[ T_{\text{tree}} = \sum_{i=1}^{d} T_C(k_i) = \sum_{i=1}^{d} (c \cdot k_i + b) \]
\[ = \sum_{i=1}^{d} (R_R + R_L + c \cdot (k_i - 1)) \]

\[ T_{\text{sbcast}} = \min_{d,k_i} \left( T_{fw} + \sum_{i=1}^{d} (c \cdot k_i + b) + \sum_{i=1}^{d} T_{nb}(k_i + 1) \right) \]

\[ N \leq 1 + \sum_{i=1}^{d} \prod_{j=1}^{i} k_j, \quad \forall i < j, k_i \leq k_j \]

Min-Max Modeling

- Example:
  - $T_0 + T_1$ write CL
  - $T_2$ polls for completion
Min-Max Modeling

- Example:
  - \( T_0 + T_1 \) write CL
  - \( T_2 \) polls for completion

---

Min-Max Modeling

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Min-Max Modeling

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  - $T_2$ polls for completion
Min-Max Modeling

- Example:
  - $T_0 + T_1$ write $CL$
  - $T_2$ polls for completion
Min-Max Modeling

- **Example:**
  - $T_0 + T_1$ write CL
  - $T_2$ polls for completion

---

*Ramos, Hoefler: “Modeling Communication in Cache-Coherent SMP Systems - A Case-Study with Xeon Phi “, HPDC’13*
Min-Max Modeling

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![Diagram of Min-Max Modeling](image)

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- Example:
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  - $T_2$ polls for completion

Small Broadcast (8 Bytes)

- Broadcast
- Min–Max Model
- Intel MPI

Latency (us) vs. Number of Threads

Barrier

Small Reduction

- Reduce
- Min–Max Model
- Intel MPI
- Intel OpenMP

Latency (us) vs. Number of threads

Lessons learned

- Rigorous modeling has large potential
  - Coming with great cost (working on tool support [1])

- Understanding cache-coherent communication performance is incredibly complex (but fun!)
  - Many states, min-max modeling, NUMA, …
  - Have models for Sandy Bridge now (QPI, worse!)

- Cache coherence really gets in our way here 😞

- Obvious question: why do we need cache coherence?
  - Answer: well, we don’t, if we program right!

[1]: Calotoiu et al.: Using Automated Performance Modeling to Find Scalability Bugs in Complex Codes, SC13
[2]: Gerstenberger et al.: Enabling Highly-Scalable Remote Memory Access Programming with MPI-3 One Sided, SC13, Best Paper
COMMUNICATION IN TODAY’S HPC SYSTEMS

- The de-facto programming model: MPI-1
  - Using send/recv messages and collectives

- The de-facto network standard: RDMA, SHM
  - Zero-copy, user-level, os-bypass, fuzz-bang

Random datacenter picture copyrighted by Reuters (yes, they go after academics with claims for 10 year old images)
MPI-1 MESSAGE PASSING – SIMPLE EAGER

Producer

Consumer

MPI-1 MESSAGE PASSING – SIMPLE EAGER

1. Data transfer to intermediate buffer

**MPI-1 Message Passing – Simple Eager**

![Diagram showing message passing process]

1. Data transfer to intermediate buffer
2. Acknowledgement

**Explanation:**
- The producer sends a message to the consumer.
- The message is transferred to an intermediate buffer.
- The consumer acknowledges the receipt of the data.

**Origin Aware of Completion:**
- The producer is aware of the completion of the transmission.

---

MPI-1 MESSAGE PASSING – SIMPLE EAGER

Critical path: 1 latency + 1 copy

MPI-1 MESSAGE PASSING – SIMPLE RENDEZVOUS

MPI-1 MESSAGE PASSING – SIMPLE RENDEZVOUS

Producer

Send

1. Transfer of communication parameters

Consumer

Mailbox

MPI-1 MESSAGE PASSING – SIMPLE RENDEZVOUS

Producer

Send

1. Transfer of communication parameters

2. Message matching

Mailbox

Consumer

Recv

MPI-1 Message Passing – Simple Rendezvous

MPI-1 MESSAGE PASSING – SIMPLE RENDEZVOUS

Critical path: 3 latencies

August 18, 2006

**A Critique of RDMA**

by Patrick Geoffray, Ph.D.

Do you remember VIA, the Virtual Interface Architecture? I do. In 1998, according to its promoters — Intel, Compaq, and Microsoft — VIA was supposed to change the face of high-performance networking. VIA was a buzzword at the time; Venture Capital was flowing, and startups multiplying. Many HPC pundits were rallying behind this low-level programming interface, which promised scalable, low-overhead, high-throughput communication, initially for HPC and eventually for the data center. The hype was on and doom was spelled for the non-believers.

It turned out that VIA, based on RDMA (Remote Direct Memory Access, or Remote DMA), was not an improvement on existing APIs to support widely used application-software interfaces such as MPI and Sockets. After a while, VIA faded away, overtaken by other developments.

VIA was eventually reborn into the RDMA programming model that is the basis of various InfiniBand Verbs implementations, as well as DAPL (Direct Access Provider Library) and iWARP (Internet Wide Area RDMA Protocol). The pundits have returned, VCs are spending their money, and RDMA is touted as an ideal solution for the efficiency of high-performance networks.

However, the evidence I'll present here shows that the revamped RDMA model is more a problem than a solution. What's more, the objective that RDMA pretends to address of efficient user-level communication between computing nodes is already solved by the two-sided Send/Recv model in products such as Quadrics QsNet, Cray SeaStar (implementing Sandia Portals), Qlogic InfiniPath, and Myricom's Myrinet Express (MX).

**Send/Recv versus RDMA**

The difference between these two paradigms, Send/Receive (Send/Recv) and RDMA, resides essentially in the
REMOTE MEMORY ACCESS PROGRAMMING

- Why not use these RDMA features more directly?
  - A global address space may simplify programming
  - … and accelerate communication
  - … and there could be a widely accepted standard

- MPI-3 RMA (“MPI One Sided”) was born
  - Just one among many others (UPC, CAF, …)
  - Designed to react to hardware trends, learn from others
  - Direct (hardware-supported) remote access
  - New way of thinking for programmers

MPI-3 RMA Summary

- MPI-3 updates RMA ("MPI One Sided")
  - Significant change from MPI-2
- Communication is "one sided" (no involvement of destination)
  - Utilize direct memory access
- RMA decouples communication & synchronization
  - Fundamentally different from message passing

**MPI-3 RMA Communication Overview**

- **Process A (passive)**
  - Memory
  - **Put**
  - **MPI window**
  - **Atomic communication calls** (Acc, Get & Acc, CAS, FAO)

- **Process B (active)**
  - Memory
  - **MPI window**
  - **Non-atomic communication calls** (put, get)

- **Process C (active)**
  - **Get**

- **Process D (active)**
  - **Atomic**
  - **...**
MPI-3 RMA Communication Overview

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Gropp, Hoefler, Thakur, Lusk: Using Advanced MPI
MPI-3 RMA Communication Overview

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- Process B (active)
- Process C (active)
- Process D (active)

Non-atomic communication calls (put, get)
Atomic communication calls (Acc, Get & Acc, CAS, FAO)

Gropp, Hoefler, Thakur, Lusk: Using Advanced MPI
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MPI-3 RMA COMMUNICATION OVERVIEW

Process A (passive)

Process B (active)

Process C (active)

Process D (active)

Memory

MPI window

Non-atomic communication calls (put, get)

Put

Get

Atomic

Atomic communication calls (Acc, Get & Acc, CAS, FAO)
MPI-3 RMA SYNCHRONIZATION OVERVIEW

Active Target Mode

- Fence
- Post/Start/Complete/Wait

Passive Target Mode

- Lock
- Lock All

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Active process
Passive process
Synchronization
Communication

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**Active Target Mode**
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### Active Target Mode
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### Passive Target Mode
- **Lock**
- **Lock All**

- **Active process**
- **Passive process**

**Communication**

---

Gropp, Hoefler, Thakur, Lusk: Using Advanced MPI
SCALABLE PROTOCOLS & REFERENCE IMPLEMENTATION

- Scalable & generic protocols
  - Can be used on any RDMA network (e.g., OFED/IB)
  - Window creation, communication and synchronization

Window creation

Communication

Synchronization
SCALABLE PROTOCOLS & REFERENCE IMPLEMENTATION

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- foMPI, a fully functional MPI-3 RMA implementation
  - DMAPP: lowest-level networking API for Cray Gemini/Aries systems
  - XPMEM, a portable Linux kernel module

http://spcl.inf.ethz.ch/Research/Parallel_Programming/foMPI
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**PERFORMANCE INTER-NODE: LATENCY**

**Put Inter-Node**
- 80% faster

**Get Inter-Node**
- 20% faster

**Graphs**
- Size [Bytes] vs. Latency [us]
- Transport Layer: FOMPI MPI-3.0, Cray UPC, Cray MPI-2.2, Cray MPI-1, Cray CAF
- DMAPP protocol change

**Half ping-pong**
- Proc 0
- put
- sync memory
- Proc 1

Gerstenberger, Besta, Hoefler: Enabling Highly-Scalable Remote Memory Access Programming with MPI-3 One Sided, SC13
PERFORMANCE INTRA-NODE: LATENCY

Put/Get Intra-Node

![Graph showing latency vs size for different transport layers]

- 3x faster

Half ping-pong

Proc 0

put

sync memory

Proc 1

Gerstenberger, Besta, Hoefler: Enabling Highly- Scalable Remote Memory Access Programming with MPI-3 One Sided, SC13
**Performance: Message Rate**

*Intra-Node*

*Inter-Node*

---

Gerstenberger, Besta, Hoefler: Enabling Highly-Scalable Remote Memory Access Programming with MPI-3 One Sided, SC13
PART 3: SYNCHRONIZATION

Active Target Mode

- Fence
- Post/Start/Complete/Wait

Passive Target Mode

- Active process
- Passive process
- Synchronization
- Communication

Lock

Lock All
SCALABLE FENCE PERFORMANCE

![Graph showing latency vs. number of processes for global synchronization methods.](image)

- **Global Synchronization**
  - FOMPI Win_fence
  - Cray UPC barrier
  - Cray CAF sync_all
  - Cray MPI Win_fence

- **90% faster**

<table>
<thead>
<tr>
<th>Bound</th>
<th>Complexity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time bound</td>
<td>$O(\log p)$</td>
</tr>
<tr>
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Gerstenberger, Besta, Hoefler: Enabling Highly-Scalable Remote Memory Access Programming with MPI-3 One Sided, SC13
**Flush Synchronization**

- Guarantees remote completion
- Performs a remote bulk synchronization and an x86 mfence
- One of the most performance critical functions, we add only 78 x86 CPU instructions to the critical path

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![Diagram](process0.png)

![Diagram](process2.png)
## Performance Modeling

Performance functions for synchronization protocols

<table>
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<tr>
<th>Fence</th>
<th>$P_{fence} = 2.9 \mu s \cdot \log_2(p)$</th>
</tr>
</thead>
</table>
| PSCW   | $P_{start} = 0.7 \mu s, P_{wait} = 1.8 \mu s$  
       | $P_{post} = P_{complete} = 350 ns \cdot k$ |
| Locks  | $P_{lock, excl} = 5.4 \mu s$  
       | $P_{lock, shrd} = P_{lock, all} = 2.7 \mu s$  
       | $P_{unlock} = P_{unlock, all} = 0.4 \mu s$  
       | $P_{flush} = 76 ns$  
       | $P_{sync} = 17 ns$ |

Performance functions for communication protocols

| Put/get | $P_{put} = 0.16 ns \cdot s + 1 \mu s$  
       | $P_{get} = 0.17 ns \cdot s + 1.9 \mu s$ |
| Atomics | $P_{acc, sum} = 28 ns \cdot s + 2.4 \mu s$  
       | $P_{acc, min} = 0.8 ns \cdot s + 7.3 \mu s$ |
APPLICATION PERFORMANCE

- Evaluation on Blue Waters System
  - 22,640 computing Cray XE6 nodes
  - 724,480 schedulable cores
- All microbenchmarks
- 4 applications
- One nearly full-scale run 😊
PERFORMANCE: MOTIF APPLICATIONS

Key/Value Store: Random Inserts per Second

![Graph showing Key/Value Store performance with different transport layers and process counts.]

Dynamic Sparse Data Exchange (DSDE) with 6 neighbors

![Graph showing Dynamic Sparse Data Exchange performance with varying numbers of processes.]
PERFORMANCE: APPLICATIONS


NAS 3D FFT [1] Performance

MILC [2] Application Execution Time

scale to 65k procs

scale to 512k procs

[1] Nishtala et al.: Scaling communication-intensive applications on BlueGene/P using one-sided communication and overlap. IPDPS'09
[2] Shan et al.: Accelerating applications at scale using one-sided communication. PGAS'12
In case you want to learn more

- Available in most MPI libraries today
- Some are even fast!

Using Advanced MPI
Modern Features of the Message-Passing Interface

How to implement producer/consumer in passive mode?

William Gropp
Torsten Hoefler
Rajeev Thakur
Ewing Lusk
**PRODUCER-CONSUMER RELATIONS**

- Most important communication idiom
  - Some examples:

- Perfectly supported by MPI-1 Message Passing
  - But how does this actually work over RDMA?
ONE SIDED – PUT + SYNCHRONIZATION

Producer

Consumer
ONE SIDED – PUT + SYNCHRONIZATION

Producer

Put

Consumer

1. Data transfer
ONE SIDED – PUT + SYNCHRONIZATION

Producer

Put

Flush

Consumer

1. Data transfer

2. Producer waits for remote completion

: origin aware of completion

ONE SIDED – PUT + SYNCHRONIZATION

COMPARING APPROACHES

Message Passing
1 latency + copy / 3 latencies

One Sided
3 latencies

**IDEA: RMA NOTIFICATIONS**

- First seen in Split-C (1992)

- Combine communication and synchronization using RDMA

- RDMA networks can provide various notifications
  - Flags
  - Counters
  - Event Queues

![Diagram of RMA Notifications](image-url)
COMPARING APPROACHES

Message Passing
1 latency + copy / 3 latencies

One Sided
3 latencies

Notified Access
1 latency

COMPARING APPROACHES

Message Passing
1 latency + copy / 3 latencies

One Sided
3 latencies

Notified Access
1 latency

But how to notify?
**PREVIOUS WORK: OVERWRITING INTERFACE**

- **Flags (polling at the remote side)**
  - Used in GASPI, DMAPP, NEON

- **Disadvantages**
  - Location of the flag chosen at the sender side
  - Consumer needs at least one flag for every process
  - Polling a high number of flags is inefficient
PREVIOUS WORK: COUNTING INTERFACE

- **Atomic counters (accumulate notifications → scalable)**
  - Used in Split-C, LAPI, SHMEM - Counting Puts, …

- **Disadvantages**
  - Dataflow applications may require many counters
  - High polling overhead to identify accesses
  - Does not preserve order (may not be linearizable)
WHAT IS A GOOD NOTIFICATION INTERFACE?

- **Scalable to yotta-scale**
  - Does memory or polling overhead grow with # of processes?

- **Computation/communication overlap**
  - Do we support maximum asynchrony? (better than MPI-1)

- **Complex data flow graphs**
  - Can we distinguish between different accesses locally?
  - Can we avoid starvation?
  - What about load balancing?

- **Ease-of-use**
  - Does it use standard mechanisms?
OUR APPROACH: NOTIFIED ACCESS

- Notifications with MPI-1 (queue-based) matching
  - Retains benefits of previous notification schemes
  - Poll only head of queue
  - Provides linearizable semantics
## Notified Access – An MPI Interface

- Minor interface evolution
  - Leverages MPI two sided `<source, tag>` matching
  - Wildcards matching with FIFO semantics

### Example Communication Primitives

<table>
<thead>
<tr>
<th>Function</th>
<th>Prototype</th>
</tr>
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<tbody>
<tr>
<td><code>MPI_Put</code></td>
<td><code>(void *origin_addr, int origin_count, MPI_Datatype origin_type, int target_rank, MPI_Aint target_disp, int target_count, MPI_Datatype target_type, MPI_Win win);</code></td>
</tr>
<tr>
<td><code>MPI_Get</code></td>
<td><code>(void *origin_addr, int origin_count, MPI_Datatype origin_type, int target_rank, MPI_Aint target_disp, int target_count, MPI_Datatype target_type, MPI_Win win);</code></td>
</tr>
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### Example Synchronization Primitives

```c
/*Functions already available in MPI*/
int MPI_Start(MPI_Request *request);
int MPI_Test(MPI_Request *request, int *flag, MPI_Status *status);
int MPI_Wait(MPI_Request *request, MPI_Status *status);
```
NOTIFIED ACCESS — AN MPI INTERFACE

- Minor interface evolution
  - Leverages MPI two sided <source, tag> matching
  - Wildcards matching with FIFO semantics

Example Communication Primitives

```
int MPI_Put_notify(void *origin_addr, int origin_count, MPI_Datatype origin_type, int target_rank, 
                   MPI_Aint target_disp, int target_count, MPI_Datatype target_type, MPI_Win win, 
                   int tag);

int MPI_Get_notify(void *origin_addr, int origin_count, MPI_Datatype origin_type, int target_rank, 
                    MPI_Aint target_disp, int target_count, MPI_Datatype target_type, MPI_Win win, 
                    int tag);
```

Example Synchronization Primitives

```
int MPI_Notify_init(MPI_Win win, int src_rank, int tag, int expected_count, MPI_Request *request);
/*Functions already available in MPI*/
int MPI_Start(MPI_Request *request);
int MPI_Test(MPI_Request *request, int *flag, MPI_Status *status);
int MPI_Wait(MPI_Request *request, MPI_Status *status);
```
NOTIFIED ACCESS - IMPLEMENTATION

- **foMPI** – a fully functional MPI-3 RMA implementation
  - Runs on newer Cray machines (Aries, Gemini)
  - DMAPP: low-level networking API for Cray systems
  - XPMEM: a portable Linux kernel module

- **Implementation of Notified Access via uGNI [1]**
  - Leverages uGNI queue semantics
  - Adds unexpected queue
  - Uses 32-bit immediate value to encode source and tag

---

EXPERIMENTAL SETTING

- **Piz Daint**
  - Cray XC30, Aries interconnect
  - 5'272 computing nodes (Intel Xeon E5-2670 + NVIDIA Tesla K20X)
  - Theoretical Peak Performance 7.787 Petaflops
  - Peak Network Bisection Bandwidth 33 TB/s

**PING PONG PERFORMANCE (INTER-NODE)**

- 1000 repetitions, each timed separately, RDTSC timer
- 95% confidence interval always within 1% of median

![Graph showing Ping Pong Performance](image)

PING PONG PERFORMANCE (INTRA-NODE)

- 1000 repetitions, each timed separately, RDTSC timer
- 95% confidence interval always within 1% of median

COMPUTATION/COMMUNICATION OVERLAP

- 1000 repetitions, each timed separately, RDTSC timer
- 95% confidence interval always within 1% of median

**Pipeline – One-to-One Synchronization**

- 1000 repetitions, each timed separately, RDTSC timer
- 95% confidence interval always within 1% of median

![Graph showing normalized completion time vs. number of processes for MPI Message Passing, MPI One Sided, and Notified Access.](image)

*lower is better*

**REDUCE – ONE-TO-MANY SYNCHRONIZATION**

- Reduce as an example (same for FMM, BH, etc.)
  - Small data (8 Bytes), 16-ary tree
  - 1000 repetitions, each timed separately with RDTSC

![Graph showing comparison of different methods](image)

- Notified Access
- MPI Message Passing
- MPI One Sided PSCW
- MPI Reduce

(lower is better)
CHOLESKY – MANY-TO-MANY SYNCHRONIZATION

- 1000 repetitions, each timed separately, RDTSC timer
- 95% confidence interval always within 10% of median

(Higher is better)

- Notified Access
- MPI Message Passing
- MPI One Sided

[1]: J. Kurzak, H. Ltaief, J. Dongarra, R. Badia: "Scheduling dense linear algebra operations on multicore processors“, CCPE 2010
## DISCUSSION AND CONCLUSIONS

- **Performance of cache-coherency is hard to model**
  - Min/max models

- **RDMA+SHM are de-facto hardware mechanisms**
  - Gives rise to RMA programming

- **MPI-3 RMA standardizes clear semantics**
  - Builds on existing practice (UPC, CAF, ARMCI etc.)
  - Rich set of synchronization mechanisms

- **Notified Access can support producer/consumer**
  - Maintains benefits of RDMA

- **Fully parameterized LogGP-like performance model**
  - Aids algorithm development and reasoning

---

### Table: Performance Comparison

<table>
<thead>
<tr>
<th>Function</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{\text{init}}$</td>
<td>$0.07\mu s$</td>
</tr>
<tr>
<td>$t_{\text{free}}$</td>
<td>$0.04\mu s$</td>
</tr>
<tr>
<td>$t_{\text{start}}$</td>
<td>$0.008\mu s$</td>
</tr>
<tr>
<td>$t_{\text{na}}$</td>
<td>$0.29\mu s$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Shared Memory</th>
<th>uGNI FMA</th>
<th>uGNI BTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>0.25$\mu s$</td>
<td>1.02$\mu s$</td>
</tr>
<tr>
<td>G</td>
<td>0.08$ns$</td>
<td>0.105$ns$</td>
</tr>
</tbody>
</table>
ACKNOWLEDGMENTS
**Hardware Reality**
- Images of hardware components and devices.

**ACKNOWLEDGMENTS**

**PERFORMANCE MODELING**
- Performance functions for synchronization protocols:
  - Fence: $P_{fence} = 2.99x \cdot \log_2(x)$
  - PSCIW: $P_{send} = 0.71x, P_{recv} = 1.81x$
  - Locks: $P_{lock} = 5.5x, P_{unlock} = 2.72x$
  - Performance for communication protocols:
    - Put/get: $P_{put} = 0.16x, P_{get} = 1.57x$
    - Atomics: $P_{atomic} = 20.8x, P_{atomic} = 2.43x$

**PERFORMANCE INTER-NODE: LATENCY**
- Put Inter-Node: 80% faster
- Get Inter-Node: 20% faster

**PERFORMANCE: APPLICATIONS**
- Annotations represent performance gain of 56% over Cray MPI-1 [3].
- NAS 3D FFT [1] Performance
- MLIC [2] Application Execution Time

**IDEA: RMA NOTIFICATIONS**
- First seen in Split-C (1992)
- Combine communication and synchronization using RDMA
  - RDMA networks can provide various notifications
    - Flags
    - Counters
    - Event Queues

**CHOLESKY – MANY-TO-MANY SYNCHRONIZATION**
- 1000 repetitions, each timed separately, RTTSC timer
- 95% confidence interval always within 10% of median

**Using Advanced MPI**
- Modern Features of the Message-Passing Interface
  - Notified Access
  - MPI Message Passing
  - MPI One Sided