

# Hardware Acceleration for Knowledge Graph Processing: Challenges & Recent Developments

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**ABSTRACT** Knowledge graphs (KGs) have achieved significant attention in recent years, particularly in the area of the Semantic Web as well as gaining popularity in other application domains such as data mining and search engines. Simultaneously, there has been enormous progress in the development of different types of heterogeneous hardware, impacting the way KGs are processed. The aim of this paper is to provide a systematic literature review of knowledge graph hardware acceleration. For this, we present a classification of the primary areas in knowledge graph technology that harnesses different hardware units for accelerating certain knowledge graph functionalities. We then extensively describe respective works, focusing on how KG related schemes harness modern hardware accelerators. Based on our review, we identify various research gaps and future exploratory directions that are anticipated to be of significant value both for academics and industry practitioners.

**INDEX TERMS** Knowledge Graphs, Semantic Web, Hardware Architectures, Systematic Literature Review, Graph Algorithms, Heterogeneous Hardware, FPGA, GPU, ASIC, CPU

## I. INTRODUCTION

**K**NOWLEDGE graphs (KG) are structured representations of information that are used to represent and organize data in a way that is easily accessible and understandable. They are used in a variety of applications, including information retrieval, natural language processing, and artificial intelligence (AI) [1]–[6].

In the current era of data-centric ecosystems, it has become vitally important to organize and represent the enormous volume of knowledge appropriately. Recently, knowledge graphs have risen as a powerful tool for representing complex associations among entities and concepts across various domains, enhancing semantic search. As these knowledge graphs continue to grow in both scale and complexity, conventional computing methods encounter difficulties in effectively processing and analysing them in real-time, and addressing these challenges has prompted the investigation of hardware acceleration as a potential solution.

Hardware acceleration involves harnessing the capabilities of specialized hardware components designed to perform specific tasks more efficiently than what would be possible

using a general-purpose Central Processing Unit (CPU), such as Graphics Processing Units (GPUs) or Field Programmable Gate Arrays (FPGAs). Both GPUs and FPGAs [7], [8] use strategies such as optimized memory use and low-precision arithmetic to accelerate computation, adding a boost to CPU server engines. While hardware acceleration has demonstrated remarkable success in various computational domains, its impact on knowledge graph processing remains relatively unexplored. Hardware acceleration has the potential to substantially enhance the performance of knowledge graph applications, enabling quicker and more precise data processing and analysis.

In this systematic literature review, we will examine the applications and consequences of hardware acceleration on knowledge graphs. We will review the existing literature on this topic and identify the main findings and trends in the use of hardware acceleration in knowledge graph applications. We will also consider the potential benefits and drawbacks of hardware acceleration, and we identify challenges and opportunities for future research and development.

## II. OVERVIEW OF KNOWLEDGE GRAPHS

Knowledge Graphs (KGs) accumulate and convey knowledge of the real world. They can effectively organize data to represent complex information, so that it can be efficiently and extensively explored in traditional and advanced applications, offering significant benefits for data exploitation in creating new knowledge. Knowledge graphs have emerged as an approach for the systematic representation of knowledge of real-world entities in a machine-readable format [9].

### A. REPRESENTATIONS

A knowledge graph is usually modeled using one of two data representations [10]: the Labeled Property Graph (LPG), also called property graph, and the Resource Description Framework (RDF). The **LPG model** categorizes vertices and edges with the help of labels and allows attributes for vertices and edges in the form of key-value pairs as properties. **RDF** represents knowledge graphs in the form of triples, where each triple consists of a subject, a predicate, and an object. Formally, edges are represented as triples  $(h, r, t)$ , where  $h$  and  $t$  are the head and tail entities, and  $r$  is the relation between them.

Knowledge graphs, regardless of the used data model, capture the relationships between entities and are composed of entities (vertices, also referred to as nodes) and relationships (edges), forming a graph structure that allows complex interconnections and associations to be easily visualized and understood.

### B. EMBEDDINGS

The knowledge graph input is typically human-readable, however certain tasks benefit from a transformed (embedded) machine representation. **Knowledge Graph Embedding (KGE)** models provide a way to represent entities (vertices) and relations (edges) of a knowledge graph in vector spaces, referred to as embeddings. These models capture the semantics of the graph and are used in various downstream tasks like link prediction, classification, and recommendation.

The goal of training a knowledge graph embedding model is to learn embeddings for entities and relations such that the embeddings of the head and tail entities are close to each other in the embedding space when connected by a relation. This is achieved by optimizing a loss function that captures the likelihood of the observed triples in the graph. One common approach is to train on both positive and negative triples. A positive triple is an observed triple in the graph, and a negative triple is a corrupted version of a positive triple. The negative triples are sampled by replacing the head or tail entity of a positive triple with another entity in the graph.

### C. BENEFITS AND APPLICATIONS

The benefits of knowledge graphs are manifold. They provide a structured and semantically rich representation of knowledge, which can be leveraged for various applications. For instance, KGs can be used to improve search engine results by understanding the context and semantics behind a user's

query. They can also be used in recommendation systems to provide more personalized and context-aware recommendations [11].

In addition to these, knowledge graphs have been successfully applied in numerous other domains. For instance, in the pharmaceutical industry, KGs can be used to represent complex relationships between drugs, diseases, and patients, thereby aiding in drug discovery and personalized medicine [12], [13]. In the field of social sciences, knowledge graphs can be used to analyze social networks and understand the dynamics of social interactions [14]–[16].

In education, several knowledge graph-based applications focus on supporting remote teaching and learning. For example, considering the importance of course allocation tasks in universities, a knowledge graph-based approach was proposed to automate this task. One could construct a course knowledge graph in which the entities are courses, lecturers, course books, and authors in order to suggest relevant courses to students [17]–[20].

In healthcare, the growth of the medical sector has led to more options for treatments. To help with this, medical recommender systems, especially biomedical knowledge graph-based recommender systems (such as doctor and medicine recommender systems), have been developed. For instance, in recommending medications, one can construct a heterogeneous graph whose nodes are medicines, diseases, and patients to recommend accurate and safe medicine prescriptions for patients with complicated medical issues [21]–[29].

Various works also propose to enhance general generative models with knowledge graphs. The focus of these works is usually to use KGs in order to enhance the LLM answers, for example by grounding knowledge in general models to reduce effects such as hallucinations [30]–[34]. Example schemes include Knowledge Graph Prompting (KGP) [35], Graph Neural Prompting (GNP) [36], Think-on-Graph (ToG) [37], Knowledge Solver (KSL) [38], KnowledgeGPT [39], and others [40], [41]. Zhu *et al.* [42] discuss how LLMs can be used for enhancing KG construction and tasks. Wen *et al.* [43] present MindMap, a framework to perform reasoning on KG data. Pertinent triples from a KG are retrieved and the LLM is prompted to answer a question based on these triples and show the reasoning process by generating a “mind map” in the form of a textual reasoning tree.

Retrieval Augmented Generation (RAG) enhances the abilities of LLMs by enabling the retrieval of documents into the LLM context to provide more accurate and relevant responses. MRAG [44] focuses on the multi-aspect problems where as structure-enhanced RAG schemes employ different strategies for structuring text to improve retrieval quality. A common idea is to construct a knowledge graph from text, which enables retrieval amongst entities and relationships [45]–[49]. RAPTOR [50] generates multi-level summaries for clusters of related documents, building a tree of summaries with increasing levels of abstraction to better capture the meaning of the text. Graph RAG [51] creates a

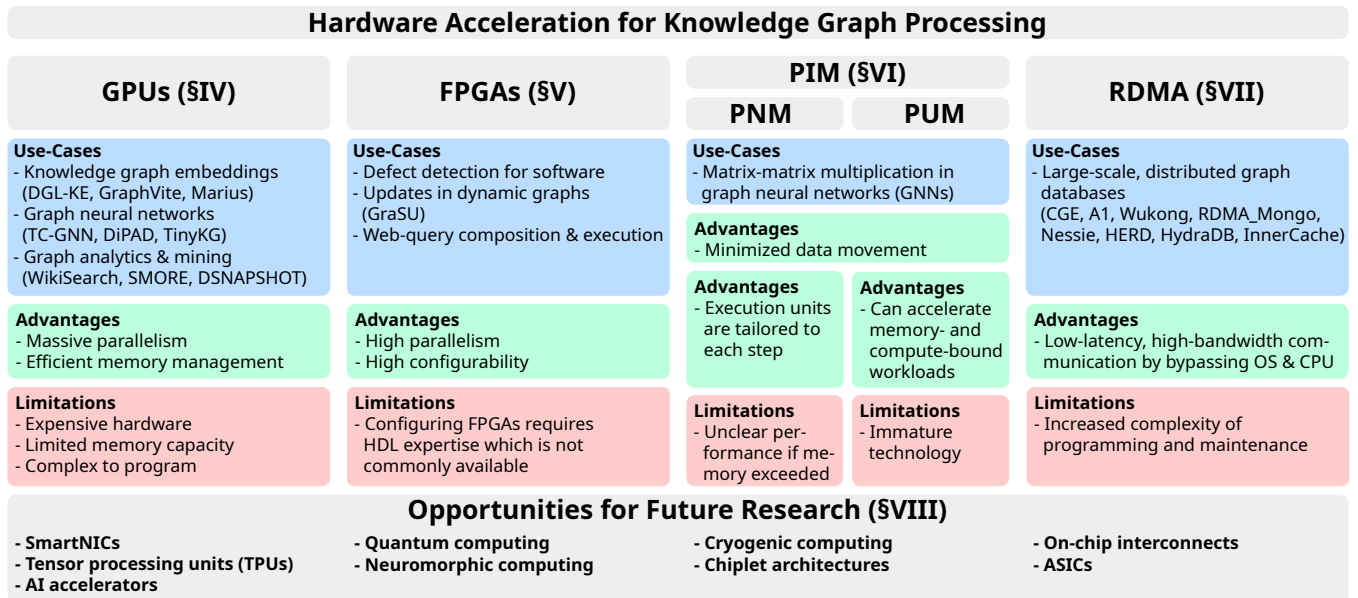


FIGURE 1: Overview of different hardware acceleration areas used for knowledge graph processing.

knowledge graph, and summarizes communities in the graph, which provide data at the different levels of abstraction.

#### D. CHALLENGES AND FUTURE DIRECTIONS

Despite their numerous benefits, knowledge graphs also pose several challenges. Their heterogeneity, as mentioned earlier, is one such challenge. It requires the development of sophisticated techniques for KG embedding that can effectively capture and preserve the diverse structures and semantics inherent in the knowledge graphs [52].

Another challenge lies in the dynamic nature of knowledge. As new information becomes available, KGs need to be updated to reflect this new knowledge. This requires efficient methods for knowledge graph updating and evolution [53].

Furthermore, the quality of the knowledge graph is heavily dependent on the quality of the input data. Hence, ensuring the accuracy and reliability of the data used to construct the KG is another significant challenge [54], [55].

The existing methods for generating knowledge graph embeddings still suffer several severe limitations. Many established methods only consider surface facts (triplets) of knowledge graphs. However, additional information, such as entity types and relation paths, are ignored, which can further improve the embedding accuracy. The performance of most traditional methods that do not consider the additional information is unsatisfactory. Recently, some researchers have started to combine additional information with a knowledge graph to improve the efficiency of embedding models [56].

Finally, more efficient processing of KGs is of great relevance, in the face of the ongoing growth of the dataset sizes. One strategy for achieving more performance is incorporating hardware acceleration techniques.

### III. OVERVIEW OF HARDWARE ACCELERATION

Hardware acceleration involves offloading specific computational tasks from the CPU to specialized hardware components within a system, leading to more efficient task processing. There are several kinds of hardware acceleration, including GPU (Graphics Processing Unit) for graphics and parallel tasks, DSP (Digital Signal Processor) for handling signals like audio, FPGA (Field-Programmable Gate Array) which can be customized for different uses after its production, ASIC (Application-Specific Integrated Circuit) designed for specific tasks, and NPU or AI Accelerators aimed at speeding up machine learning tasks. Figure 1 presents an overview of the covered hardware acceleration areas for knowledge graph processing.

To facilitate hardware acceleration, various technologies like CUDA by NVIDIA for general-purpose computing on GPUs, OpenCL for programming diverse systems, DXVA for hardware-accelerated video decoding, and WebGL for web-based graphics are used. These tools enable improved performance and energy efficiency, freeing up CPU resources for other tasks and enhancing the user experience. However, challenges such as compatibility issues, increased software complexity, higher initial costs, and the risk of hardware failure also arise. Despite these challenges, the benefits of hardware acceleration, including better performance and efficiency, make it a key element in advancing technology, especially as we move towards more specialized processing tasks.

### IV. GPUS & KNOWLEDGE GRAPHS

Graphics Processing Units (GPUs) have emerged as powerful units for a multitude of computationally intensive tasks. Initially made for gaming graphics, GPUs are now crucial in many devices including smartphones, computers, and gam-

ing consoles. Moreover, GPUs support massive parallelism, making them ideal for tasks that require heavy computation, such as machine learning, scientific computing, and cryptocurrency mining. They are now a key component in supercomputers and data centers. Nine out of the ten top supercomputers in the TOP500 list are powered by GPUs [57].

### A. FUNDAMENTAL GPU CONCEPTS

GPUs have several some key benefits that make them suitable for accelerating knowledge graph applications. GPUs support **massive parallelism** and excel at performing many operations simultaneously with thousands of cores, making them ideal for processing large-scale knowledge graphs, executing graph algorithms, and training machine learning models on knowledge graphs. Efficient **memory management** of GPUs can greatly speed up the processing of knowledge graphs. GPUs can use **thread-level parallelism** and employ **warp scheduling**. Specifically, GPU threads are grouped into warps, which are scheduled for execution together. By carefully organizing threads that access adjacent graph nodes or edges into the same warp (a technique known as “coalescing”), one can maximize memory access efficiency and minimize warp divergence, leading to significant performance improvements. GPU frameworks often allow the **asynchronous execution** of different operations, enabling the overlap of computation and memory transfer to hide latencies and improve throughput. Additionally, **stream prioritization** of operations can ensure responsive interactive querying in knowledge graph applications. **Hardware-accelerated libraries** such as cuGraph [58] (from NVIDIA’s RAPIDS suite) provide GPU-accelerated graph analytics algorithms, which can be used in knowledge graph applications. For deep learning on knowledge graphs, libraries such as PyTorch Geometric offer GPU-accelerated graph neural network layers.

### B. KNOWLEDGE GRAPHS WITH GPUS

GPUs have been increasingly leveraged in knowledge graph applications due to their capability for parallel processing in two main areas. First, knowledge graphs are typically stored and indexed using high-performance graph database engines. Data analytics and machine learning techniques are applied to data stored in graph databases by extracting relevant data from the knowledge graphs using query languages (SPARQL for RDF graphs and Cypher, Gremlin as well as others for property graphs). A large body of work [59], [60] has focused on accelerating graph databases and individual knowledge graph queries using GPUs. Second, knowledge graphs are employed to learn inductive information using either supervised or unsupervised machine learning approaches. Researchers have focused on the use of GPUs for accelerating this learning process which we outline below.

#### 1) Knowledge Graph Embeddings

Embedding matrices are large and they typically do not fit into the limited GPU memory. A common approach to address this challenge is to keep the embeddings in the main

memory and transfer them to the GPU memory as needed. However, this results in severe latency penalties if GPUs exchange data with the main memory frequently.

In a parallel setting where multiple workers together train a model, the graph and the embeddings need to be partitioned across workers. Depending on the partitioning strategy, workers might need access to embeddings of entities and relations that are not local to them. Workers also need to synchronize their updates to the embedding matrices. Depending on the sampling strategy employed, workers might require further remote access for entities of negative triples. This results in a high degree of communication between workers, which can be a bottleneck in the training process.

Several works have explored parallel training of knowledge graph embedding models on GPUs, tackling the above challenges. **DGL-KE** [12] is a distributed training framework for KGE models that uses a hybrid CPU-GPU system. It employs a distributed key-value store for both the knowledge graph structure and the embeddings, using shared CPU memory. A GPU worker unit retrieves embeddings from CPU memory, updates them, and then writes the embeddings back to the CPU memory. In DGL-KE, the knowledge graph is partitioned via METIS [61] such that most of the entity and relation embeddings are local, in order to minimize communication between the compute units. GPUs are not efficient in handling random memory access, and hence DGL-KE samples the negative triples in the CPU, and then transfers them to the GPU for training. This sampling is done from the local METIS partition to ensure that there is no increase in remote accesses for negative samples. Other optimizations in DGL-KE include relation partitioning and overlap of gradient updates for relation as well as entity embeddings.

**GraphVite** [62] focuses on multi-GPU training of KGE models. In line with past works, it tackles the challenges of limited GPU memory and bus bandwidth as well as synchronization overhead. GraphVite partitions the embeddings in a way that avoids CPU-GPU or inter-GPU communication during training. Positive triples are partitioned so, that they access pairwise disjoint embeddings, and negative triples are sampled from the local partition. Workers perform mini-batch updates on the local embeddings and synchronize only at the end of an epoch.

**Marius** [63] is a framework designed for efficient computation of graph embeddings on a single machine by leveraging partition caching and buffer-aware data orderings to minimize disk access and interleave data movement with computation. The pipeline updates node embedding parameters in CPU memory asynchronously, allowing for staleness, while the relation embeddings are updated in GPU memory synchronously. This design choice is based on the observation that updates to node embedding vectors are sparse, whereas updates to relation embedding parameters are dense due to the smaller number of edge-types in real-world graphs.

Another way to use GPUs for KGEs is to transform the knowledge graph completion problem into a similarity join problem, which can be efficiently processed by GPUs. This

method can leverage the metric properties of some KGE models, such as TransE [64] and RotatE [65], to reduce the number of vector operations and filter out irrelevant candidates. By using GPUs, this method can achieve fast and accurate knowledge graph completion on large-scale datasets [66].

## 2) Graph Neural Networks

A graph neural network (GNN) [67] is a neural network in which input samples are graphs. GNNs, as opposed to embeddings, support end-to-end learning. Thus, GNNs can be used to solve various KG-related tasks like link prediction, knowledge graph alignment, and node classification [68]. GPUs can accelerate the computation of GNNs by exploiting the parallelism and locality of graph operations and utilizing the specialized hardware features of GPUs. For example, **TC-GNN** [69] proposes the use of tensor cores to accelerate sparse matrix multiplication in GNNs by transforming the sparse graph data into dense tensors. **PIPAD** [70] proposes to use pipelining and parallelism techniques to improve the efficiency and scalability of dynamic GNN training on GPUs.

Traditional KGE methods mainly focus on predicting the legitimacy between two entities and a particular relation type. GNNs have been shown to be effective in capturing the topological features of entities such as shapes of neighborhood sub-graphs which are overlooked by the traditional KGE methods [71]. However, their model complexity is higher in terms of the number of trainable parameters.

**Sheikh et al.** [72] propose three key strategies to scale GNNs to large knowledge graphs. Their system leverages vertex-cut partitioning to create self-sufficient graph sections and employs local negative sampling within partitions, significantly reducing communication overhead. It also utilizes edge mini-batch training, allowing efficient handling of large graph sections on GPUs.

**TinyKG** [73] is a memory-efficient framework for training Knowledge Graph Neural Networks. Traditional training of these networks is memory-intensive due to the need to store all intermediate activation maps for gradient computation, making deployment challenging in memory-constrained environments. TinyKG addresses this by using exact activations during the forward pass and storing a quantized version in the GPU buffers. During the backward pass, these quantized activations are dequantized for gradient computation. TinyKG employs a simple quantization algorithm to compress activations, reducing the training memory footprint with minimal accuracy loss.

## 3) Symbolic Learning and Rule Mining

Machine learning techniques that learn numerical models are hard to interpret and quantify. Instead, symbolic learning can be used to learn hypotheses in a logical (symbolic) language that “explains” sets of positive and negative edges. Such hypotheses are interpretable and quantifiable (e.g., “all airports are domestic or international”), partially addressing the out-of-vocabulary issue. Symbolic learning techniques

such as rule and pattern mining are used to discover interesting patterns over knowledge graph data. GPUs can exploit features of rule mining algorithms for more performance, for example frequent itemset generation, candidate pruning, support counting, and confidence evaluation. There exists a large body of work that focuses on accelerating rule mining specifically, and frequent itemset mining more generally, using GPUs. Most of them focus on accelerating the underlying algorithm like Apriori [74] that is widely used for rule mining. We refer the reader to a recent survey [75] of several GPU accelerated frequent itemset mining solutions proposed in literature for further reference.

## 4) Graph Analytics and Mining

The application of analytical methods to large-scale graphs is known as graph analytics. Such algorithms frequently examine the graph topology, or how nodes and groups of nodes are related. GPUs can accelerate a wide range of graph algorithms such as breadth-first search (BFS), single-source shortest path (SSSP), and community detection [60].

**WikiSearch** [76] is an efficient parallel keyword search engine designed for large-scale knowledge graphs, with a focus on the Wikidata Knowledge Base, though it is applicable to other knowledge graphs as well. To exploit parallelism, a novel approach for keyword search based on the central graph method is proposed. Unlike traditional methods that approximate the group Steiner tree problem, this approach can naturally operate in parallel and returns compact, information-rich answer graphs. It is optimized for both multi-core CPU and GPU architectures. WikiSearch also introduces a novel pruning strategy based on keyword co-occurrence to refine search results further.

**Scalable Multi-hop REasoning (SMORE)** [77] is a framework for both single-hop knowledge graph completion and multi-hop reasoning on large knowledge graphs, that involves predicting answers to queries that span multiple relations or hops in the graph, which requires capturing complex dependencies and performing logical operations over entities and relations. The computational complexity for such tasks increases significantly with the number of hops, leading to higher memory requirements and processing times. For a massive knowledge graph containing hundreds of millions of entities, it is not feasible to materialize training instances, and training data needs to be efficiently sampled on the fly with high throughput to ensure efficient utilization of computation resources. SMORE addresses this with a novel bidirectional rejection sampling approach for efficient online training data generation and an asynchronous system design that overlaps data sampling, embedding computation, and CPU-GPU communication. Also, graph partitioning is not feasible for multi-hop reasoning, as it requires traversing multiple relations in the graph, which will often span across multiple partitions. SMORE is designed to operate in a shared memory environment, bypassing the limitations of graph partitioning in multi-hop reasoning, and demonstrates near-linear speed-up with the number of GPUs used for training.

In the field of biomedicine, the connections among various biomedical entities, including drugs, diseases, symptoms, proteins, and genes play a crucial role in understanding the underlying mechanisms of diseases and drugs. Biomedical knowledge graphs play an important role in representing these connections and are used in various applications such as drug discovery and repurposing. **Distributed Accelerated Semiring All-Pairs Shortest Path (DSNAPSHOT)** [78] is a scalable knowledge graph analytics system that can perform all-pairs shortest path (APSP) computation on large biomedical knowledge graphs. It exploits the relation between the semiring GEMM [79] and the APSP computation, and implements a GPU-optimized distributed semiring GEMM kernel, the key operation in the Floyd-Warshall algorithm for APSP computation. Further, DSNAPSHOT proposes optimizations for both inter-node and intra-node communication, and achieves 90% parallel efficiency on the Summit super-computer.

#### 5) Graph Visualization

Due to high dimensionality, heterogeneity, and sparsity of data, displaying knowledge graphs might be difficult. By offering parallel computing capability, high memory bandwidth, and specialized hardware characteristics for graphics tasks, GPUs can make it possible for large-scale graph data to be rendered and processed more quickly, thereby speeding up knowledge graph visualization. One such example is **KG4Vis** [80], a knowledge graph-based approach for visualization recommendation. It uses a TransE-based embedding technique to learn the embeddings of both entities and relations of the knowledge graph from existing dataset-visualization pairs. Such embeddings intrinsically model the desirable visualization rules and can be accelerated by GPUs.

### C. CHALLENGES & LIMITATIONS

As knowledge graphs continue to grow in size and complexity, GPUs will likely play an increasingly important role in managing and extracting value from these datasets. However, GPUs also have several disadvantages that might make them unsuitable for some knowledge graph applications.

The **cost** of high-performance GPUs can be steep, which can be a barrier to their use, especially for small organizations or individual developers. GPUs have their own onboard memory, which is typically much less than the main memory available to a CPU. While this memory is typically faster, the **limited memory capacity** can be a challenge when working with large datasets that do not fit into the GPU's memory. GPUs are more **complex to program** than CPUs. Writing code that effectively leverages the parallel processing capabilities of a GPU can require a different approach than what many developers are accustomed to [81]. GPUs often use more power and generate more heat than CPUs, which can lead to additional **hardware requirements** regarding power supply and cooling in a computer system. Not all tasks can be effectively parallelized and see benefits from a GPU [82]. Tasks with heavy data dependencies or those

that are inherently sequential may not see a performance improvement on a GPU, and might even be slower than on a CPU. Such **limited tasks** may benefit from applying a hybrid (CPU+GPU) processing strategy [83].

Hence, it is worth noting that not all knowledge graph tasks can benefit from GPU acceleration. Certain operations, such as graph updates or graph schema modifications, may not be well-suited for GPU parallelism. The effectiveness of GPU acceleration will ultimately depend on specific graph algorithms, data sizes, and hardware configurations. Thus, concrete benchmarking and microarchitectural analysis of various knowledge graph-related tasks is required to understand the degree to which each task can benefit from GPU acceleration.

## V. FPGAS & KNOWLEDGE GRAPHS

Field-Programmable Gate Arrays (FPGAs) have emerged as integral components in contemporary digital electronics, facilitating the development of custom digital circuits with a degree of versatility unmatched by other devices. Characterized by arrays of programmable logic blocks and configurable interconnects, FPGAs offer a distinctive combination of adaptability and performance.

### A. FUNDAMENTAL FPGA CONCEPTS

The cornerstone of any FPGA, **logic elements** and **logic blocks** comprise arrays of both combinational and sequential circuit elements. Programmable in nature, they can be tailored to execute a myriad of logical functions, laying the groundwork for the vast functionalities FPGAs are known for. The pathways of **configurable interconnects** serve a pivotal role in an FPGA's architecture, facilitating signal routing across the device. Their adaptability ensures seamless communication between discrete segments of a given design, optimizing the device's functionality. A quintessential aspect of an FPGA's reprogrammability is its **configuration memory**. This component retains the user-defined design logic, effectively determining the FPGA's operational behavior. Acting as the interface between the FPGA and its external environment, **I/O blocks** are instrumental in the device's ability to both send and receive signals, thereby ensuring effective communication with other devices or components. In light of the stringent timing constraints often associated with FPGA applications, effective clock distribution and management are paramount. Mastery over **clock management** is crucial for the successful deployment of FPGA-based designs. Analogous to programming languages in the realm of software development, **Hardware Description Language (HDL)** such as VHDL and Verilog as well as, more recently, other abstractions such as **High-Level Synthesis (HLS)** [84] are employed to define and describe circuit behavior within an FPGA.

### B. KNOWLEDGE GRAPHS WITH FPGAS

FPGAs have been increasingly utilized for knowledge graph processing due to their high parallelism and configurabil-

ity, which can significantly enhance the efficiency of graph computations. FPGAs can be used to accelerate various graph processing tasks, including defect detection in software code [85], high-throughput updates on dynamic graphs [86], efficient traversal of edge-labeled directed graphs [87] and automated composition and execution of Semantic Web queries [88]. FPGAs have also been used for implementing various graph algorithms, such as BFS or PageRank [89]–[91].

Different techniques have been employed to optimize the use of FPGAs for knowledge graph processing. For instance, **GraSU** [86], an FPGA library designed for the Xilinx Alveo™ U250 accelerator card, exploits the spatial similarity of graph updates to improve overall efficiency. GraSU outperformed two state-of-the-art CPU-based dynamic graph systems significantly in terms of update throughput. Another technique involves the use of a pipeline approach that combines parallel BFS and nondeterministic finite automaton for efficient graph traversal [87]. Additionally, the use of partial runtime-reconfiguration enables transparent query evaluation on an FPGA [88].

Several specific schemes and mechanisms have been developed to optimize the use of FPGAs for knowledge graph processing. For instance, a work-stealing-based scheduler, **HWS** [92], has been designed to optimize workload balance on heterogeneous CPU-FPGA systems. Another example is the implementation of a stochastic matrix function estimator on FPGAs to boost the performance and energy efficiency of subgraph centrality computations [93], [94]. Furthermore, an accelerator for quantized Graph Convolutional Networks (GCNs) with edge-level parallelism has been developed, using low-precision integer arithmetic during inference [95], which demonstrated significant speedups and energy savings compared to other models.

### C. ADVANTAGES & DISADVANTAGES

FPGAs offer several advantages for semantic knowledge graph processing. They provide high parallelism and configurability, which can significantly enhance the efficiency of graph computations [85]. FPGAs can also provide significant speedups and energy savings compared to other models [95]. Despite the advantages offered by FPGAs and their rapid growth, the use of FPGA technology is restricted to a narrow segment of hardware programmers due to their code written differently using a hardware description language to design the FPGA configuration. The challenge with the HDL approach is that configuring an FPGA requires both coding skills and a detailed knowledge of the underlying hardware, and the required expertise is not widely available. More recent abstractions such as HLS [84], [96]–[100] attempt to alleviate these issues. Additionally, while FPGAs can provide significant performance improvements for certain tasks, they may not benefit all queries [88].

## VI. PROCESSING-IN-MEMORY & KNOWLEDGE GRAPHS

Processing-In-Memory (PIM) is a promising way to alleviate the data movement bottleneck [101], [102], i.e., the waste of execution cycles and energy due to moving data between memory/storage and compute units, in current processor-centric computing systems (e.g., CPU, GPU).

### A. FUNDAMENTAL PIM CONCEPTS

There are two main PIM trends. The first one is called **Processing-Near-Memory (PNM)** and consists of placing compute logic near the memory arrays (e.g., DRAM subarrays, banks, ranks) [103]–[109]. **Processing-Using-Memory (PUM)** is the other one, which leverages the analog operational properties of memory components (e.g., cells, sense amplifiers) to perform computation [110]–[114]. PIM represents a successful research trend in recent years, and several commercial PIM systems and prototypes [115]–[125] have been presented.

### B. KNOWLEDGE GRAPHS WITH PIM

Graph Neural Networks use deep learning to process graph data, including knowledge graphs [126]. GNNs can solve different knowledge graph tasks, such as link prediction, knowledge graph alignment and reasoning, and node classification [68]. There are several classes of GNNs: GCNs [127], attentional GNNs [128] and message-passing GNNs [129]. **GCNs** are composed of several GCN layers, each computing two steps: the aggregation of vertex features (a *reduce* operation), and a combination of features (an *update* operation with typically fully-connected layers). After the loss computation, the backward pass is composed of feature/weight gradients computation (update), and feature gradients aggregation (reduce). While update operations (e.g., matrix multiplication) are compute-bound, reduce operations (e.g., gather-reduce-scatter) are very memory-bound. As such, reduce operations are good candidates for PIM-based acceleration. Several recent works [130]–[134] propose PIM acceleration for GCNs. Some of these works deploy PUM techniques such as ReRAM-based crossbars [131], [133]. Other works use PNM techniques with processing units in DDR DIMMs [130], [134] and in HBM stacks [132].

PUM approaches rely on crossbar arrays, which help minimizing data movement in reduce operations, and computing matrix multiplication efficiently. **ReFlip** [133] proposes a unified crossbar-based PUM architecture that supports both compute-bound and memory-bound kernels. With software/hardware co-optimizations, ReFlip maps both types of kernels efficiently onto the massive parallelism of its ReRAM-based crossbar arrays. **COIN** [131] targets the huge communication overheads of GCNs. For example, processing the Nell [135] knowledge graph causes 2.7TB of data moving between nodes of a baseline crossbar-based PUM architecture. COIN proposes an optimized on-chip interconnection network for efficient communication between compute elements and between the crossbars inside each compute element. The network design is applicable to different cross-

bars such as ReRAM- and SRAM-based, but COIN prefers ReRAM, which is significantly more energy efficient.

PNM approaches combine heterogeneous computing units that are specialized for different steps. **GNNear** [134] integrates an ASIC with matrix multiply and vector processing units and PNM-enabled DIMMs. Update operations are computed on the ASIC, while execution units in the buffer chip of the DIMMs compute reduce operations. Huang *et al.* [130] tackle the large memory footprint and data movement needs of GNNs with memory pooling. The authors propose a customized memory fabric interface for low-latency and high-throughput communication across PNM units in memory extension cards. The PNM units contain a RISC-V core, a matrix multiply unit, and a vector processing unit. **SGCN** [132] exploits the sparse nature of intermediate GCN features to reduce the memory footprint (via compression) and optimize communication. SGCN places aggregation units (with SIMD MACs) and combination units (with a systolic array for matrix multiplication) near HBM memory.

### C. ADVANTAGES AND DISADVANTAGES

PUM approaches for GNNs offer the advantage that the same crossbar-based PUM unit can accelerate both memory-bound and compute-bound kernels. Their main disadvantage is that they are based on memory technologies that are not yet mature (e.g., limited endurance and high area of ADCs in ReRAM and other non-volatile memories).

PNM approaches tailor their execution units to the specific needs of each step, which represents an advantage of their approach. However, they have yet to show how their performance would scale for knowledge graphs exceeding their memory capacity.

While the aforementioned works show great promise for GCN acceleration, their evaluations are all based on simulation. We hope to see soon efficient implementations of GNNs on existing real-world PIM architectures [115]–[125] and future ones.

## VII. CLUSTER-LEVEL RDMA & KNOWLEDGE GRAPHS

Remote Direct Memory Access (RDMA) is a mechanism for achieving high performance and scalability in both the supercomputing as well as the cloud data center landscapes [136]–[151]. RDMA has grown popular as RDMA-enabled network interface cards have become widely used, and is commonly supported in modern interconnects [152], [153]. Overall, RDMA has many use-cases, particularly in distributed environment. Examples include speeding up data replication [154]–[158], transactions [10], [159]–[162], index queries [163], file systems [164], general queries [165]–[167], or analytical workloads [10], [126], [168]–[176].

### A. FUNDAMENTAL RDMA CONCEPTS

In general, the advantages of RDMA stem from the fact that communication bypasses the OS and the CPU, reducing or eliminating overheads such as interrupts. While one can harness RDMA in different ways, highest performance is usually

achieved with fully-offloaded one-sided communication. In this approach, processes communicate by directly accessing dedicated portions of other processes' memory. In the established one-sided communication specification included in the Message-Passing Interface [177], this portion is called a window.

One-sided accesses are done with communication operations referred to as puts and gets. They – respectively – write to and read from windows, offering very low latencies and most often outperform other communication paradigms such as message passing [137]. Other useful RDMA operations include remote atomics such as Compare-and-Swap or Fetch-and-Add [176]–[179] that are often accelerated by the interconnect hardware. They enable very fast fine-grained synchronization. To enforce data consistency between windows, operations called flushes are employed to explicitly synchronize memories. The communication operations come in two variants, blocking (operation execution blocks till completion) and non-blocking (operation execution returns immediately upon initiating communication). The latter can additionally increase performance by overlapping communication and computation [137], with the user taking responsibility to synchronize memories at some point after starting the call. All of these routines are supported by most RDMA architectures.

### B. KNOWLEDGE GRAPHS WITH RDMA

**Cray Graph Engine (CGE)** [180], [181] is a system developed by Cray to support executing very large-scale RDF triple stores on top of Cray high-performance computing systems. CGE's design is based on the Partitioned Global Address Space (PGAS) abstraction, in which one creates a single logical memory pool encompassing all the physical distributed memories over all compute nodes. Thus, CGE effectively implements the Single Program Multiple Data (SPMD) model and uses a purely one-sided RMA programming model, where memory access is treated as effectively uniform (i.e., at the programming level, one does not distinguish between local or remote accesses). Hence, one does not need to consider problems such as efficient graph partitioning. Simultaneously, to achieve high performance, CGE heavily relies on different hardware features offered by the targeted systems. Such features include latency hiding, passive parallelism, and high network throughput for small remote requests that occur commonly in the targeted graph workloads. For example, one of the architectures used in the evaluation, the XMT2 system, used the Threadstorm processors with 128 hardware streams per node. For the whole system of a typical size (64–512 nodes), this amounts to a total of thousands to tens of thousands of software threads that can be used in a given single graph query. Finally, the CGE implementation relies on a low-level high-performance networking communication library [182] by Cray.

Improvements for graph analytics queries [183] with CGE were made by the use of non-blocking communication for large exchanges and by processing intermediate solutions



in stages to exploit locality. Additional recent improvements [184] make CGE more portable by replacing low-level DMAPP operations with one-sided MPI routines, as well as simplifying the software stack. Several optimizations are employed to enable container performance matching that of native execution. Message-aggregation within each compute node is employed for join/scan/merge operations to reduce the number of messages. That number is further reduced by improving the communication patterns to enable storing of messages for the same compute node consecutively. Distinct flushes for put and get operations improve the overlap of computation and communication.

**A1** [185] is a distributed in-memory graph database developed by Microsoft. It adds graph abstraction and query engine layers on top of an improved FaRM key-value store [160]. FaRM already comes with transaction support and uses one-sided read and write operations as well as RPCs to implement its functionality. A1 further improves FaRMs transactions by employing an optimistic multi-version concurrency control scheme by introducing a global clock and timestamps. RDMA is implemented with the RoCEv2 protocol [186] and DCQCN is used for congestion control. RDMA-based unreliable datagrams are used for clock synchronization and leases. A1 is latency-optimized by employing data structures, which reduce the number of read operations, co-locating data likely to be requested at the same time like nodes and their edges as well as RPC aggregation to reduce the number of messages. A1 uses a semi-structured data model based on Bond [187] with strictly-typed edges and weakly-typed nodes.

**Wukong** [188] is a research-oriented distributed in-memory RDF triple store. Its storage layer is implemented using a simplified version of a RDMA-friendly distributed hashtable based on DrTM-KV [159]. Wukong duplicates edges during graph partitioning to store self-contained sub-graphs on each compute node to preserve locality. It supports indices based on type and predicate. These indices are treated as a special kind of nodes and are usually replicated. Strings are stored separately and mapped to unique IDs to reduce network bandwidth. Wukong supports concurrent query execution with full history pruning, data (in-place) and/or execution (fork/join) migration as well as task stealing for load balancing and to reduce query latency. Originally providing limited update support, Wukong spawned several improved implementations. Wukong+S [189] adds support for stream queries as well as incremental key-value updates. Wukong+G [190] uses GPUs to further improve query throughput by using the GPU memory as cache as well as the massive compute power of GPUs for triple parsing. Adaptive query scheduling was further proposed [191] for Wukong+G to combine the processing of multiple queries similar to the fusion of kernels.

**RDMA\_Mongo** [192], a document-oriented NoSQL database, uses RDMA writes to replace part of its TCP/IP-communication layer. **Nessie** [193], a key-value store, uses cuckoo hashing with RDMA for its key-value operations.

**Nessie** decouples index and data storage to improve locality. **HERD** [140], another key-value store, uses one-sided RDMA writes and two-sided RDMA send/receives to complete each of its operations with a single network round trip. The key-value store **HydraDB** [139] uses RDMA to accelerate its read operations and key caches with timestamps to reduce network pressure for highly skewed workloads. Similarly, **InnerCache** [194] uses one-sided RDMA to accelerate reads from the key-value store acting as an application cache and two-sided semantics for writing data. RDMA-based Memcached has been used for the integration of the Hadoop storage layer (HDFS) with the underlying high performance parallel filesystem Lustre to improve the I/O performance of big data analytics [195]. Additionally a non-blocking API extension for Memcached to improve communication and computation overlap as well as an enhanced runtime design for hybrid use with SSDs was proposed [196].

Finally, the **Graph Database Interface (GDI)** [170] has recently been proposed to deliver a toolbox for designing a scalable and high-performance data access and transaction layer for general graph databases that can also be used to maintain knowledge graphs. Its RDMA-based implementation, **GDI-RMA** [171], has been shown to scale to more than a hundred thousand compute cores and to label- and property-rich graphs with more than 500 billion edges. The key mechanisms used for high performance are one-sided non-blocking RDMA communication, hardware-accelerated network atomic operations, and collective communication, a form of group communication that has been tuned over decades by the MPI community [177].

### C. ADVANTAGES AND DISADVANTAGES

RDMA usually enables significant performance advantages in terms of both latency and bandwidth. The former is enabled by eliminating expensive parts of the communication pipeline (such as interrupts) and by supporting features such as network-accelerated atomic operations. The latter is facilitated by features such as the overlap of computation and communication. On the other hand, RDMA is usually more complex to program and maintain. This, however, has been alleviated with efforts such as the one-sided communication within MPI [137], [177] or by GDI [170], [171].

## VIII. FUTURE RESEARCH OPPORTUNITIES

We identified four research gaps in current solutions, that provide opportunities for future studies: scalability, energy efficiency, real-time processing and the integration with other technologies.

While current hardware solutions have shown promise in handling large-scale knowledge graphs, there is a pressing need to address the **scalability** challenges posed by the ever-growing size and complexity of semantic data. The energy consumption of hardware accelerators, especially when processing extensive knowledge graphs, remains a concern. Research into more **energy-efficient** hardware designs is crucial. The ability to process and update knowledge graphs

in **real-time**, especially in dynamic environments, is still an area with limited research.

The synergy between different forms of hardware acceleration and **other technologies** is not fully explored. Existing works, such as DaCe [197], [198], focus on effective and efficient execution of different workloads on the underlying diverse hardware, targeting – among others – machine learning [199], linear algebra kernels [200], and – more recently – GNNs [201]. Extending this line of works towards knowledge graphs specifically is an interesting research opportunity. Another, related, opportunity is to combine this approach with other emerging technologies, such as quantum computing or neuromorphic computing.

In conclusion, while significant strides have been made in the domain of hardware-accelerated semantic knowledge graph processing, there remains a vast landscape of uncharted territory. By addressing the identified research gaps and capitalizing on the highlighted opportunities, the scientific community can pave the way for more efficient, scalable, and innovative solutions in the future.

#### A. NOVEL HARDWARE ACCELERATION SCHEMES

Beyond the hardware acceleration techniques previously mentioned, there are several innovative hardware solutions that can enhance knowledge graph processing.

**SmartNICs** are advanced network interface cards (NICs) that allow the processing of tasks on the NIC [202] instead of the CPU. For load balancing in distributed settings, SmartNICs can distribute incoming queries to different servers to ensure efficient utilization of resources. They can also be used in the context of data preprocessing, where SmartNICs preprocess and filter irrelevant data, therefore speeding up the data ingestion process of the knowledge graph.

Originally designed for machine learning, **Tensor Processing Units (TPUs)** can also be harnessed for knowledge graph tasks that incorporate machine learning. TPUs can accelerate the training and inference of GNNs to be used for node and graph classification as well as link prediction in knowledge graphs. TPUs can also compute efficiently node and edge embeddings for similarity searches and clustering in knowledge graphs.

Additionally various **AI accelerators**, such as Google’s Edge TPU and Intel’s Nervana Neural Network Processor, can process knowledge graphs in order to detect anomalies or inconsistencies to guarantee data integrity. Google’s Edge TPU can be used on edge devices to locally update a knowledge graph as new data streams in to ensure that graph processing remains current.

**Quantum Computing** is an emerging field with the potential to redefine computing. For knowledge graph processing it holds the promise of more efficient computation for various algorithms such as graph isomorphism, i.e. determining if two graphs are structurally identical, or pathfinding (finding the shortest path or optimal connections between nodes).

Inspired by the human brain, **Neuromorphic Computing** can be advantageous for traditionally challenging tasks.

Neuromorphic chips can help to identify patterns or trends in knowledge graphs and can aide in tasks like recommendation systems or predictive analytics. Similar as a human brain learns from experience, neuromorphic computing can adaptively learn from data in the knowledge graphs and refine queries and results over time.

Utilizing superconducting circuits that function at ultra-low temperatures, **Cryogenic Computing**, though in its infancy, has potential for large-scale knowledge graph processing tasks. At extremely low temperatures, superconducting circuits can process vast amounts of data simultaneously, which allows for massive parallel processing of large-scale knowledge graph analytics, where multiple queries and computations are performed concurrently. Cryogenic computing can also offer significant energy savings, making the processing more sustainable and cost-effective.

**Chiplet** architectures [203], where multiple silicon dies are integrated into a single package, have gained significant traction in the chip design industry [204]. Chiplets come with a wide range of benefits, including modularity, reusability, flexibility, specialization, cost-efficiency and reduced time-to-market. Even though we are not aware of any chiplet-based accelerators specifically designed to process knowledge graph, chiplets have played an important role in knowledge graph processing. A team of researchers was elected as Gordon Bell Prize [205] finalists for running their COAST (communication-optimized all-pairs shortest path) [206] algorithm for knowledge graphs on Frontier, the world’s first exascale supercomputer, which uses chiplet-based AMD EPYC CPUs [207], [208]. There is also a variety of propositions for chiplet-based accelerators for general graph processing [209]–[212], which hints for a large potential of leveraging their modularity and cost-efficiency for hardware accelerators tailored to knowledge graph processing.

As the number of compute cores in modern processors and accelerators is steadily increasing, networks-on-chips (NoCs) have emerged as a scalable **On-Chip Interconnect** solutions. In a NoC, data packets are sent through a series of links and routers, akin to computer networks [213]. The de facto standard topology for NoCs is a 2D mesh [214], [215], however, more elaborate topologies such as Slim NoC [216] or sparse Hamming graphs [217] have been proposed. Most accelerators for graph processing rely on these mesh topologies [218], [219], while some hardware architects argue that a mesh is not suitable for graph algorithms, as these algorithms often cause data movement between physically distant cores. One approach to tackle this challenge is the use of small-world networks [220] as NoC topologies for graph processing accelerators [221], [222]. We believe that there is significant value in a thorough investigation of traffic caused by knowledge graph processing and a subsequent evaluation of NoC topologies for knowledge graph accelerators.

Application-Specific Integrated Circuits (**ASICs**) mark a transformative shift in VLSI design, enabling systems to be embedded within single chips rather than assembled from

multiple components [223]. This evolution, akin to the earlier microprocessor revolution, not only reshapes the electronics industry's design and manufacturing strategies but also interconnects designers, CAE tool developers, and ASIC vendors in intricate ways. Broadly, ASIC covers a spectrum from programmable logic devices (PLD) to gate arrays (GA), standard cells (SC), and full custom (FC) designs, with GA and SC being the most commonly referenced. We find it surprising that there are no works on designing ASICs for knowledge graphs, beyond the PIM-related works; it constitutes a promising direction of future development.

## IX. CONCLUSION

In this paper, we explore hardware acceleration for knowledge graph applications. We review the existing literature, identify main designs and trends in that area, benefits and drawbacks of hardware acceleration, as well as the challenges and opportunities for future research and development. We consider GPUs, FPGAs, Processing-In-Memory, RDMA, and other forms of acceleration. Our work can help design more efficient KG processing schemes.

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