

# On the Parallel I/O Optimality of Linear Algebra Kernels: Near-Optimal LU Factorization

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## ABSTRACT

Dense linear algebra kernels, such as linear solvers or tensor contractions, are fundamental components of many scientific computing applications. In this work we present a novel method of deriving parallel I/O lower bounds for this broad family of programs. Based on the *X*-Partitioning abstraction, our method explicitly captures inter-statement dependencies. Applying our analysis to LU factorization, we derive *CONfLUX*, an LU algorithm with the parallel I/O cost of  $N^3/(P\sqrt{M})$  communicated elements per processor – only  $1/3\times$  over our established lower bound. We evaluate *CONfLUX* on various problem sizes, demonstrating empirical results that match our theoretical analysis, communicating asymptotically less than Cray ScaLAPACK or SLATE, and outperforming the asymptotically-optimal CANDMC library. Running on 1,024 nodes of Piz Daint, *CONfLUX* communicates  $1.6\times$  less than the second-best implementation and is expected to communicate  $2.1\times$  less on a full-scale run on Summit.

## 1 INTRODUCTION

Data movement is widely considered a bottleneck in high-performance computing [62], often dominating time and energy consumption of computations [38, 61]. Thus, deriving algorithmic I/O lower bounds has always been of theoretical interest [12, 35]; and developing I/O-efficient schedules is of high practical value [53, 57]. In linear algebra computations, this challenge is exacerbated by the fact that the matrices of interest can be prohibitively large. Simultaneously, large-scale linear algebra kernels such as matrix factorizations [40, 46] or tensor contractions [58], are the basis of many problems in scientific computing [16, 64]. Therefore, accelerating these routines is of great significance for numerous domains.

Analyzing I/O bounds of linear algebra kernels dates back to a seminal work by Hong and Kung [35], who derived a first asymptotic bound for matrix-matrix multiplication (MMM) using the red-blue pebble game abstraction. This method was subsequently extended and used by other works to derive asymptotic [26] and tight [42] bounds for more complex programs. Despite its expressibility, problems based on pebble game abstractions are notoriously hard to solve, as they are P-SPACE complete in the general case [43]. Other techniques include methods based on the Loomis-Whitney inequality [34], [6], [7], [19] and the polyhedral model program representation [8]. Ultimately, the existing methods are either problem-specific and hard to generalize [42]; provide only asymptotic or non-tight lower bounds [20], [34]; or are limited to only single-statement micro kernels, unable to capture more complex dependencies [12], [17].

To tackle these challenges, we first provide a *general* method for deriving *precise* I/O lower bounds of Disjoint Array Access

Programs (DAAP) – a broad range of programs composed of a sequence of statements enclosed in an arbitrary number of nested loops. Within this class, we explicitly model both the *per-statement data dependencies*, using the *X*-Partitioning abstraction [42], as well as *inter-statement data dependencies*, in which we model potential data reuse. In Section 6 we illustrate the applicability of our framework to derive a parallel I/O lower bound of LU factorization:  $\frac{2}{3} \frac{N^3}{P\sqrt{M}}$  elements, where  $N$  is the matrix size,  $P$  is the number of processors, and  $M$  is the local memory size.

Moreover, in Section 7, we use the insights from deriving the above lower bound to develop *CONfLUX*, a near *Communication Optimal LU factorization, X-Partitioning-based* algorithm. Our algorithm minimizes data movement across the 2.5D processor decomposition using a row-masking tournament pivoting strategy, resulting in a communication requirement of  $\frac{N^3}{P\sqrt{M}} + O(\frac{N^2}{P})$  elements per processor, which leading order term is only a factor of  $\frac{1}{3}$  over the lower bound.

In Section 8, we measure the communication volume of *CONfLUX* and we compare to other modern implementations of LU factorization. We consider a vendor-optimized ScaLAPACK from Cray’s LibSci [9] (an implementation tuned for Cray supercomputers based on 2D decomposition), CANDMC [54, 55] (code based on asymptotically optimal 2.5D decomposition), and SLATE [28] (a recent library targeting exascale systems with an LU implementation based on 2D decomposition). As the scope of this work is the I/O complexity, we focus on the communication volume of these implementations. We tested them on a wide range of problem sizes and numbers of processors inspired by real scientific applications. In our experiments on Piz Daint, we measure up to  $4.1\times$  communication reduction compared to the second-best implementation. Furthermore, our 2.5D decomposition is asymptotically better than SLATE and LibSci, with even greater expected speedups on exascale machines. Compared to the communication-avoiding CANDMC library with the I/O cost of  $5N^3/(P\sqrt{M})$  elements [56], *CONfLUX* communicates five times less.

In this work, we provide the following contributions:

- A general method for deriving parallel I/O lower bounds of a broad range of linear algebra kernels.
- An I/O lower bound of parallel LU factorization.
- *CONfLUX*, a provably near-I/O-optimal parallel algorithm for LU factorization.
- A full analysis of communication volume in *CONfLUX* and a comparison to the state-of-the-art implementations of LU factorization (LibSci, SLATE, CANDMC), showing consistent benefits of *CONfLUX* and thus our general approach over state-of-the-art libraries.

## 2 BACKGROUND

### 2.1 Machine Model

To model the algorithmic I/O complexity, we start with a model of a sequential machine equipped with a two-level deep memory hierarchy (Sections 3 and 4). In Section 5, we use the parallel machine model and show which complexity properties are invariant.

**Sequential machine.** A computation is performed on a sequential machine with a fast memory of limited size and unlimited slow memory. The fast memory can hold up to  $M$  elements at any given time. To perform any computation, all input elements must reside in fast memory, and the result is stored in fast memory.

**Parallel machine.** The sequential model is extended to a machine equipped with  $P$  processors, each equipped with a private fast memory of size  $M$ . There is no global memory of unlimited size — instead, elements are transferred between processors' fast memories.

### 2.2 Input Programs

We consider a general class of programs that operate on multidimensional arrays. Array elements can be loaded from slow to fast memory, stored from fast to slow memory, and computed inside fast memory. Elements have *versions*, which are incremented every time they are updated. We model the program execution as a computational directed acyclic graph (cDAG, details in Section 2.3), where each vertex corresponds to a different version of an element. E.g., for a statement  $A[i, j] \leftarrow f(A[i, j])$ , a vertex corresponding to  $A[i, j]$  after applying  $f$  is different from a vertex corresponding to  $A[i, j]$  before applying  $f$ . In a cDAG, we model it as an edge from vertex  $A[i, j]$  before  $f$  to vertex  $A[i, j]$  after  $f$ . Initial versions of each element do not have any incoming edges and thus form the cDAG inputs. *The distinction between elements and vertices* is important for our I/O lower bounds analysis, as we will investigate how many vertices are computed for a given number of loaded vertices.

A program is a sequence of statements  $S$  enclosed in loop nests, each of the following form (we use the loop nest notation used by Dinh and Demmel [21]):

$$\text{for } r^1 \in R^1, \text{ for } r^2 \in R^2(r^1), \dots \text{ for } r^l \in R^l(r^1, \dots, r^{l-1}) : \\ S : A_0[\phi_0(r)] \leftarrow f(A_1[\phi_1(r)], A_2[\phi_2(r)], \dots, A_m[\phi_m(r)])$$

where (cf. Figure 1 and Table 1 for summaries):

- (1) The *statement*  $S$  is nested in a loop nest of depth  $l$ .
- (2) Each loop in the  $t$ -th level,  $t = 1, \dots, l$  is associated with its *iteration variable*  $r^t$ , which iterates over its set  $r^t \in R^t$ . Set  $R^t$  may depend on iteration variables from outer loops  $r^1, \dots, r^{t-1}$  (denoted as  $R^t(r^1, \dots, r^{t-1})$ ).
- (3) All  $l$  iteration variables form the *iteration vector*  $r = [r^1, \dots, r^l]$  and we define the *iteration domain*  $R$  as the set of all iteration vectors  $\forall r : r \in R$ .
- (4) Each evaluation of statement  $S$  is a function on  $m$  input elements, each input belongs to a logical array  $A_j$ . Different logical arrays may refer to the same memory region. The dimension of a logical array is denoted as  $\dim(A_j)$ .
- (5) Elements of logical array  $A_j$  are referenced by an *access function vector*  $\phi_j = [\phi_j^1, \dots, \phi_j^{\dim(A_j)}]$ , which maps  $\dim(A_j)$  iteration variables to a *unique* element in array  $A_j$  (access function vector

Input prog. (§ 2.2)	$A_0$	Output of statement $S$ .
	$A_j, j = 1, \dots, m$	Input $j$ of statement $S$ .
	$r = [r^1, \dots, r^l]$	Iteration vector composed of $l$ iteration variables.
	$R^t$	Iteration domain of variable $r^t \in R^t$ , which may depend on iteration variables $1 \dots t-1$ .
	$\phi_j$	Access vector mapping $\dim(\phi_j)$ iteration variables to a $\dim(A_j)$ dimensional address in array $A_j$ .
X-Partitioning (§ 2.3)	$G = (V, E)$	computational Directed Acyclic Graph (cDAG) with $V$ vertices and $E \subset V \times V$ directed edges.
	$M$	Number of red pebbles (size of the fast memory).
	$V_h \subset V$	An $h$ -th subcomputation of an $X$ -partition, $h = 1, \dots, s$
	$Dom(V_h)$	Dominator set of subcomputation $V_h$ .
	$\mathcal{P}(X) = \{V_1, \dots, V_s\}$	An $X$ -partition composed of $s$ disjoint subcomputations.
	$\Pi(X)$	The set of all $X$ -partitions of size $X$ .
	$Q$	A number of I/O operations of a schedule.
	$\rho_h$	The computational intensity of subcomputation $V_h$ .
	$\rho = \max_h \{\rho_1, \dots, \rho_s\}$	The maximum computational intensity of $\mathcal{P}(X)$ .
DAAP sched. (§ 3)	$R_h^t$	Set of all values iteration variable $t$ takes during subcomputation $h$ .
	$R_{h,j}^k$	Set of all values $k$ -th iteration variable of access function vector $\phi_j$ takes during subcomputation $h$ .
	$R_h$	Iteration domain of subcomputation $h$ — set of all iteration vectors accessed during $h$ .
	$ A_j(R_h) $	Number of different vertices accessed from array $A_j$ during subcomputation $h$ .

**Table 1:** Notation used in the paper.

- is injective). Only vertices associated with the newest element versions can be referenced.
- (6) A given vertex can be referenced by only one access function vector per statement. We will refer to this as *disjoint access property*.
  - (7) The *access dimension* of  $A_j(\phi_j)$ , denoted  $\dim(A_j(\phi_j))$ , is the number of different iteration variables present in  $\phi_j$ . *Example: consider access  $A_j[k, k]$  used, e.g., in LU factorization. Its access function vector  $\phi_j = [k, k]$  is a function of only one iteration variable  $k$ . Therefore,  $\dim(A_j) = 2$ , but  $\dim(A_j(\phi_j)) = 1$ . If it is clear from the context, we will refer to  $\dim(A_j(\phi_j))$  simply as  $\dim(\phi_j)$ .*
  - (8) The result of a statement evaluation is stored in array  $A_0$ .

We denote an input program of this form as a *Disjoint Array Access Program* (DAAP). In summary, for each innermost loop iteration (and its corresponding iteration vector  $r$ ), each statement is an evaluation of some function  $f$  on  $m$  inputs, where every input is an element of array  $A_j, j = 1, \dots, m$ , and the result of  $f$  is stored to the output array  $A_0$  at location  $\phi_0(r)$ . The notation used in this work is summarized in Table 1, along with an example program (LU factorization) in Figure 1. We want to emphasize that even though the evaluation in this paper focuses mostly on the I/O minimization of the parallel LU factorization for illustrative purposes, our universal method can be applied to other kernels, like Cholesky and QR factorizations, or more general tensor contractions.

**Note: Elements and vertices.** Consider a program:

```
for k = 1:10    for i = k+1:10    for j = k+1:10
A(i, j) = A(i, j) - A(i, k)*A(k, j)
end; end; end;
```

Consider the element  $A(5, 3)$ . Even though it is referenced more than once, for example for  $k=1; i=5; j=3$ ; by access  $A_1(\phi_1)=A(i, j)$ , and

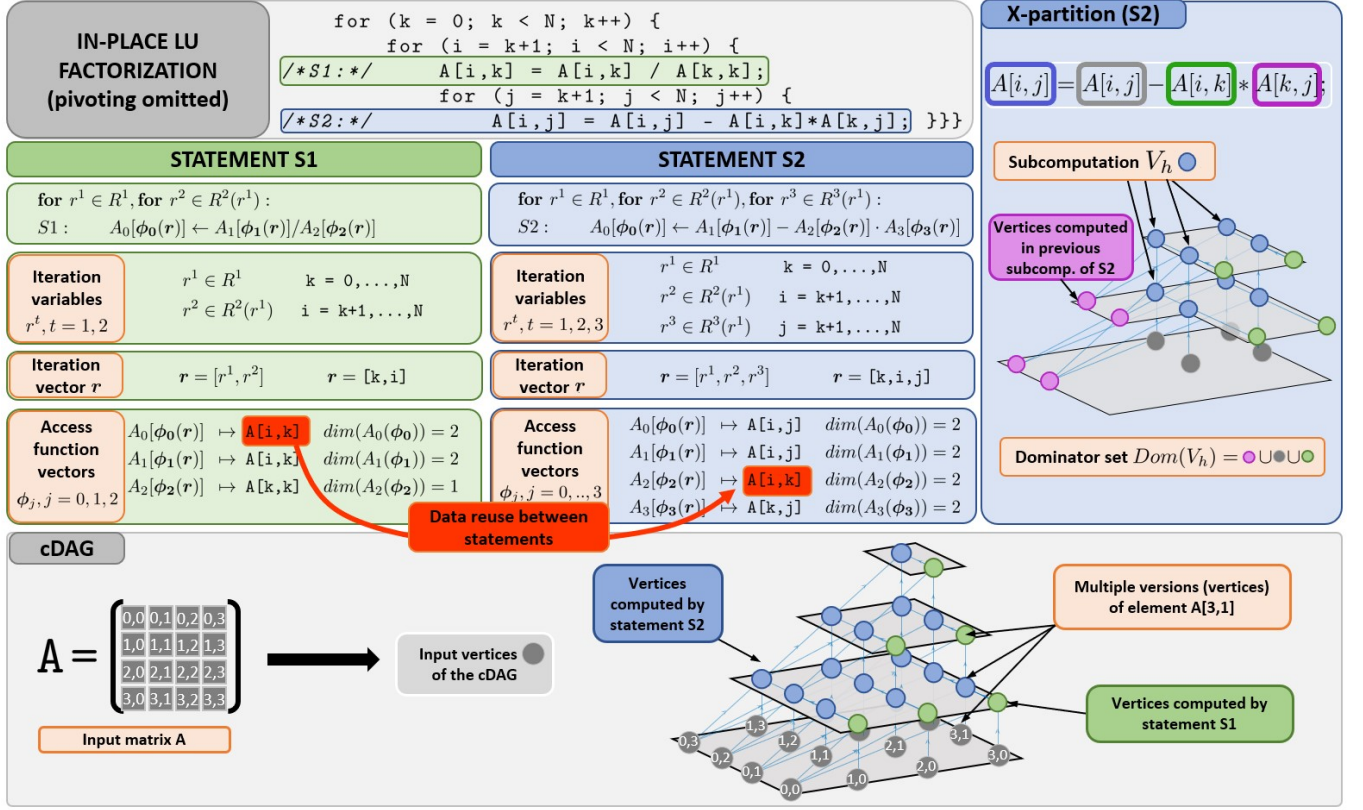


Figure 1: In-place LU factorization (for simplicity, no pivoting is performed). LU contains two statements (S1 and S2), for which we provide key components of our program representation, together with the corresponding cDAG for  $N = 4$ . For statement S2, we also provide a graphical visualization of a single subcomputation  $V_h$  in its X-partition.

for  $k=3; i=5; j=4$ ; (access  $A_2(\phi_2) = A(i, k)$ ), this element has been updated and has different versions in these two accesses, corresponding to different vertices in the cDAG. Observe however, that if the second loop iterated over range for  $i = k:10$ , this would not be a valid DAAP program, as it would invalidate the disjoint access property.

### 2.3 I/O Complexity and Pebble Games

We now establish the relationship between DAAP and the red-blue pebble game — a powerful abstraction for deriving lower bounds and optimal schedules of cDAGs evaluation.

**2.3.1 cDAG and Red-Blue Pebble Game.** Introduced by Hong and Kung [35], the red-blue pebble game is played on the computation directed acyclic graph (cDAG)  $G = (V, E)$ . Every vertex  $v \in V$  represents a result of a unique computation stored in some memory and a directed edge  $(u, v) \in E$  represents a data dependency. Vertices without any incoming (outgoing) edges are called *inputs (outputs)*. The vertices that are currently in fast memory are marked by a red pebble on the corresponding vertex of the cDAG. Since the size of fast memory is limited (we denote this size by the parameter  $M$ ), we can never have more than  $M$  red pebbles on the cDAG at any moment. Analogously, the contents of the slow memory (of unlimited size) is represented by an unlimited number of blue pebbles. To perform a computation, i.e., to evaluate the value corresponding

to vertex  $v$ , all direct predecessors of  $v$  must be loaded into fast memory.

**Rules and goal of the game.** The game proceeds as follows: First, all input vertices have blue pebbles placed on them, and no red pebbles are present in the cDAG. At any time, one of the following *pebbling moves* are allowed: 1) placing a red pebble on a vertex which has a blue pebble (load), 2) placing a blue pebble on a vertex which has a red pebble (store), 3) placing a red pebble on a vertex which all direct predecessors have red pebbles (compute), 4) removing any pebble from a vertex (discard). The goal of a game is to find a sequence of pebbling moves such that all output vertices have blue pebbles placed on them, and the number of load and store operations is minimized. For this, we need definitions of certain sets of vertices that impose a structure on the cDAG.

**2.3.2 Dominator and Minimum Sets.** For any subset of vertices  $V_h \subset V$ , a *dominator set*  $Dom(V_h)$  is a set such that every path in the cDAG from an input vertex that enters  $V_h$  must contain at least one vertex in  $Dom(V_h)$ . They further define the *minimum set*  $Min(V_h)$  as the set of all vertices in  $V_h$  that do not have any immediate successors in  $V_h$ . To avoid the ambiguity of non-uniqueness of dominator set size, we denote a *minimum dominator set*  $Dom_{min}(V_h)$  to be a dominator set with the smallest size.

**Intuition.** A dominator set abstracts a set of inputs required to execute subcomputation  $V_h$  and a minimum set a set of outputs of  $V_h$ . We

bound computation “volume” (number of vertices in  $V_h$ ) by its communication “surface”, comprised by its inputs - vertices in  $Dom_{min}(V_h)$  and outputs - vertices in  $Min(V_h)$ .

**2.3.3 X-Partitioning.** Introduced by Kwasniewski et al. [42], X-Partitioning generalizes the work by Hong and Kung [35]. An X-partition of a cDAG is a collection of  $s$  mutually disjoint subsets  $V_h$  (referred as subcomputations)  $\mathcal{P}(X) = \{V_1, \dots, V_s\}$  of  $V$  to  $s$  with two additional properties:

- no cyclic dependencies between subcomputations,
- $\forall h, |Dom_{min}(V_h)| \leq X$  and  $|Min(V_h)| \leq X$ .

For a given cDAG and for any given  $X > M$ , denote  $\Pi(X)$  a set of all its valid X-partitions,  $\mathcal{P}(X) \in \Pi(X)$ . Kwasniewski et al. prove that an I/O optimal schedule of  $G$ , which performs  $Q$  load and store operations, has an associated X-partition  $\mathcal{P}_{opt}(X) \in \Pi(X)$  with size  $|\mathcal{P}_{opt}(X)| \leq \frac{Q+X-M}{X-M}$  for any  $X > M$  ([42] extended version, Lemma 2).

**Intuition.** If a smallest dominator set of  $V_h$  contains  $X$  vertices, then at least  $X - M$  vertices need to be loaded. Note that there may exist a valid X-partition  $\mathcal{P}_{min}(X) \in \Pi(X)$  such that  $|\mathcal{P}_{min}(X)| < |\mathcal{P}_{opt}(X)|$ . Such X-partition cannot be directly translated to a valid schedule, but may serve as a lower bound.

**2.3.4 Deriving lower bounds.** The following lemma bounds the number I/O operations required to pebble a given cDAG:

**Lemma 1.** (Lemma 4 in [42], extended version) For any constant  $X_c$ , the number of I/O operations  $Q$  required to pebble a cDAG  $G = (V, E)$  with  $|V| = n$  vertices using  $M$  red pebbles is bounded by  $Q \geq n/\rho$ , where  $\rho = \frac{|V_{max}|}{X-M}$  is the maximal computational intensity,  $V_{max} = \arg \max_{V_h \in \mathcal{P}(X_c)} |V_h|$  is the largest subcomputation among all valid  $X_c$ -partitions.

**Limitations of existing methods.** While pebbling-based approaches have been successfully applied to algorithms like FFT [35], sorting [25], and parallel MMM [42], they still pose several limitations:

- **Parametric cDAGs.** Existing methods operate on cDAGs where vertices and edges are explicitly provided. To handle cDAGs of parametric sizes (e.g.,  $N^3$  vertices of MMM or  $N \log N$  vertices of FFT), additional, non-generalizable methods must be further applied.
- **Complexity.** Finding an optimal pebbling sequence is P-SPACE complete [43]; and S- or, more general, X-partitioning is NP-hard (reducible to max-cut).
- **Lower bounds vs. schedule.** There is no general, direct method to translate lower bounds derived from X-partitioning to a correct schedule.

In the following section, we take advantage of a DAAP structure (Section 2.2) to build up a new, general method for obtaining I/O lower bounds. This allows capturing *parametric cDAGs*, as all vertex sets are symbolic. It drastically reduces the *complexity*, as individual vertices do not need to be modeled anymore.

### 3 GENERAL I/O LOWER BOUNDS

In this section, we derive I/O bounds for a single statement. In Section 4 we extend our analysis to capture interactions and reuse between different statements in the program.

In this paper, we present the key lemmas and the intuition behind them to guide the reader to our main result – near optimal

parallel LU factorization. However, the method covers a much wider spectrum of algorithms. For curious readers, we present all proofs of provided lemmas, together with the full theoretical analysis, in the attached supplementary material.

We start with stating our key lemma:

**Lemma 2.** If  $|V_{max}|$  can be expressed as a closed-form function of  $X$ , that is  $|V_{max}| = \psi(X)$ , then the lower bound on  $Q$  may be expressed as:

$$Q \geq n \frac{(X_0 - M)}{\psi(X_0)}$$

where  $X_0 = \arg \min_X \rho = \arg \min_X \frac{\psi(X)}{X-M}$ .

**PROOF.** Note that Lemma 1 is valid for any  $X_c$  (i.e., for any  $X_c$ , it gives a valid lower bound). Yet, these bounds are not necessarily tight. As we want to find tight I/O lower bounds, we need to maximize the lower bound.  $X_0$  by definition minimizes  $\rho$ ; thus, it maximizes the bound. Lemma 2 then follows directly from Lemma 1 by substituting  $\rho = \frac{\psi(X_0)}{X_0-M}$ .  $\square$

**Intuition.**  $\psi(X)$  expresses computation “volume”, while  $X$  is its input “surface”.  $X_0$  corresponds to the situation where the ratio of this “volume” to the required communication is minimized (corresponding to a highest lower bound).

**Note.** If function  $\psi(X)$  is differentiable and has a global minimum, we can find  $X_0$  by, e.g., solving the equation  $\frac{d\psi(X)}{dX} = 0$ . The key limitation is that it is not always possible to find  $\psi$ , that is, to express  $|V_{max}|$  solely as a function of  $X$ . However, for many linear algebra kernels  $\psi(X)$  exists. Furthermore, one can relax this problem preserving the correctness of the lower bound, that is, by finding a function  $\hat{\psi} : \forall X \hat{\psi}(X) \geq \psi(X)$ .

#### 3.1 Iteration vector, domain, and access sizes

Each execution of statement  $S$  is associated with the *iteration vector*  $\mathbf{r} = [r^1, \dots, r^l] \in \mathbb{N}^l$  representing the current iteration, that is, values of iteration variables  $r^1, \dots, r^l$ . Each subcomputation  $V_h$  is uniquely defined by all iteration vectors associated with vertices pebbled in  $V_h$ :  $\{r_h^1, \dots, r_h^{|V_h|}\} = R_h$ . For each iteration variable  $r^t$ ,  $t = 1, \dots, l$ , denote the set of all values that  $r^t$  takes during  $V_h$  as  $R_h^t$ . We have  $r_h^t \in R_h^t \subseteq R^t \subseteq \mathbb{N}$ . We denote  $R_h \subseteq [R_h^1, \dots, R_h^l] \subseteq \mathbf{R}$  as the *iteration domain* of subcomputation  $V_h$ .

Furthermore, recall that each input access  $A_j[\phi_j(\mathbf{r})]$  is uniquely defined by  $dim(\phi_j)$  iteration variables  $r_j^1, \dots, r_j^{dim(\phi_j)}$ . Denote the set of all values each of  $r_j^k$  takes during  $V_h$  as  $R_{h,j}^k$ . Given  $R_h$ , we also denote the number of different vertices that are accessed from each input array  $A_j$  as  $|A_j(R_h)|$ .

We now state the lemma which bounds  $|V_h|$  by the iteration sets’ sizes  $|R_h^t|$ :

**Lemma 3.** Given the ranges of all iteration variables  $R_h^t$ ,  $t = 1, \dots, l$  during subcomputation  $V_h$ , if  $|V_h| = \prod_{t=1}^l |R_h^t|$ , then  $\forall j = 1, \dots, m : |A_j(R_h)| = \prod_{k=1}^{dim(\phi_j)} |R_{h,j}^k|$  and  $|V_h|$  is maximized among all valid subcomputations which iterate over  $R_h = [R_h^1, \dots, R_h^l]$ .

To prove it, we now introduce two auxiliary lemmas:

**Lemma 4.** For statement  $S$ , the size  $|V_h|$  of subcomputation  $V_h$  (number of vertices of  $S$  computed during  $V_h$ ) is bounded by the sizes of the iteration variables' sets  $R_h^t$ ,  $t = 1, \dots, l$ :

$$|V_h| \leq \prod_{t=1}^l |R_h^t|. \quad (1)$$

**PROOF.** Inequality 1 follows from a combinatorial argument: each computation in  $V_h$  is uniquely defined by its iteration vector  $[r^1, \dots, r^l]$ . As each iteration variable  $r^t$  takes  $|R_h^t|$  different values during  $V_h$ , we have  $|R_h^1| \cdot |R_h^2| \cdot \dots \cdot |R_h^l| = \prod_{t=1}^l |R_h^t|$  ways how to uniquely choose the iteration vector in  $V_h$ .  $\square$

Now, given  $R_h$ , we want to assess how many different vertices are accessed for each input array  $A_j$ . Recall that this number is denoted as access size  $|A_j(R_h)|$ .

We will apply the same combinatorial reasoning to  $A_j(R_h)$ . For each access  $A_j[\phi_j(\mathbf{r})]$ , each one of  $r_j^k$ ,  $k = 1, \dots, \dim(\phi_j)$  iteration variables loops over set  $R_{h,j}^k$  during subcomputation  $V_h$ . We can thus bound size of  $A_j(R_h)$  similarly to Lemma 4:

**Lemma 5.** The access size  $|A_j(R_h)|$  of subcomputation  $V_h$  (the number of vertices from the array  $A_j$  required to compute  $V_h$ ) is bounded by the sizes of  $\dim(\phi_j)$  iteration variables' sets  $R_{h,j}^k$ ,  $k = 1, \dots, \dim(\phi_j)$ :

$$\forall j=1, \dots, m : |A_j(R_h)| \leq \prod_{k=1}^{\dim(\phi_j)} |R_{h,j}^k| \quad (2)$$

where  $R_{h,j}^k \ni r_j^k$  is the set over which iteration variable  $r_j^k$  iterates during  $V_h$ .

**PROOF.** We use the same combinatorial argument as in Lemma 4. Each vertex in  $A_j(R_h)$  is uniquely defined by  $[r_j^1, \dots, r_j^{\dim(\phi_j)}]$ . Knowing the number of different values each  $r_j^k$  takes, we bound the number of different access vectors  $\phi_j(\mathbf{r}_h)$ .  $\square$

**Example:** Consider once more statement  $S1$  from LU factorization in Figure 1. We have  $\phi_0 = [i, k]$ ,  $\phi_1 = [i, k]$ , and  $\phi_2 = [k, k]$ . Denote the iteration subdomain for subcomputation  $V_h$  as  $R_h = \{[k^1, i^1], \dots, [k^{|V_h|}, i^{|V_h|}]\}$ , where each variable  $k$  and  $i$  iterates over its set  $k^g \in \{r_{k,1}, \dots, r_{k,K}\} = R_h^k$  and  $i^g \in \{r_{i,1}, \dots, r_{i,I}\} = R_h^i$ , for  $g = 1, \dots, |V_h|$ . Denote the sizes of these sets as  $|R_h^k| = K_h$  and  $|R_h^i| = I_h$ , that is, during  $V_h$ , variable  $k$  takes  $K$  different values and  $i$  takes  $I_h$  different values. For  $\phi_1$ , both iteration variables used are different:  $k$  and  $i$ . Therefore, we have (Equation 2)  $|A_1(R_h)| \leq K_h \cdot I_h$ . On the other hand, for  $\phi_2$ , the iteration variable  $k$  is used twice. Recall that the access dimension is the minimum number of different iteration variables that uniquely address it (Section 2.2), so its dimension is  $\dim(A_2) = 1$  and the only iteration variable needed to uniquely determine  $\phi_2$  is  $k$ . Therefore,  $|A_2(R_h)| \leq K_h$ .

**Dominator set.** Input vertices  $A_1, \dots, A_m$  form a dominator set of vertices  $A_0$ , because any path from graph inputs to any vertex in  $A_0$  must include at least one vertex from  $A_1, \dots, A_m$ . This is also the minimum dominator set, because of the disjoint access property (Section 2.2): any path from graph inputs to any vertex in  $A_0$  can include at most one vertex from  $A_1, \dots, A_m$ .

*Proof of Lemma 3.* For subcomputation  $V_h$ , we have  $|\bigcup_{j=1}^m A_j(R_h)| \leq X$  (by the definition of an  $X$ -partition). Again, by the disjoint access

property, we have  $\forall j_1 \neq j_2 : A_{j_1}(R_h) \cap A_{j_2}(R_h) = \emptyset$ . Therefore, we also have  $|\bigcup_{j=1}^m A_j(R_h)| = \sum_{j=1}^m |A_j(R_h)|$ . We now want to maximize  $|V_h|$ , that is to find  $V_{max}$  to obtain computational intensity  $\rho$  (Lemma 2).

Now we prove that to maximize  $|V_h|$ , inequalities 1 and 2 must be tight (become equalities).

From proof of Lemma 4 it follows that  $|V_h|$  is maximized when iteration vector  $\mathbf{r}$  takes all possible combinations of iteration variables  $r_h^t \in R_h^t$  during  $V_h$ . But, as we visit each combination of all  $l$  iteration variables, for each access  $A_j$  every combination of its  $[r_j^1, \dots, r_j^{\dim(\phi_j)}]$  iteration variables is also visited. Therefore, for every  $j = 1, \dots, m$ , each access size  $|A_j(R_h)|$  is maximized (Lemma 5), as access functions are injective, which implies that for each combination of  $[r_j^1, \dots, r_j^{\dim(\phi_j)}]$ , there is one access to  $A_j$ .  $\prod_{t=1}^l |R_h^t|$  is then the upper bound on  $|V_h|$ , and its tightness implies that all bounds on access sizes  $|A_j(R_h)| \leq \prod_{k=1}^{\dim(\phi_j)} |R_{h,j}^k|$  are also tight.  $\square$

**Intuition.** Lemma 3 states that if each iteration variable  $r^t$ ,  $t=1, \dots, l$  takes  $|R_h^t|$  different values, then there are at most  $\prod_{t=1}^l |R_h^t|$  different iteration vectors  $\mathbf{r}$  which can be formed in  $V_h$ . Therefore, to maximize  $|V_h|$ , all combinations of values  $r^t$  should be evaluated. On the other hand, this also implies maximization of all access sizes  $|A_j(R_h)| = \prod_{k=1}^{\dim(\phi_j)} |R_{h,j}^k|$ .

### 3.2 Finding the I/O Lower Bound

Denoting  $V_{max} = \arg \max_{V_h \in \mathcal{P}(X)} |V_h|$  the largest subcomputation among all valid  $X$ -partitions, we use Lemma 3 and combine it with the dominator set constraint. Note that all access set sizes are strictly positive integers  $|R_{max}^t| \in \mathbb{N}_+$ ,  $t = 1, \dots, l$ . Otherwise, no computation can be performed. However, as we only want to find the bound on number of I/O operations, we relax the integer constraints and replace them with  $|R_{max}^t| \geq 1$ . Then, we formulate finding  $\psi(X)$  (Lemma 2), as the optimization problem:

$$\begin{aligned} & \max \prod_{t=1}^l |R_{max}^t| \quad \text{s.t.} \\ & \sum_{j=1}^m \prod_{k=1}^{\dim(\phi_j)} |R_{max,j}^k| \leq X \\ & \forall 1 \geq t \geq l : |R_{max}^t| \geq 1 \end{aligned} \quad (3)$$

We then find  $|V_{max}| = \psi(X)$  as a function of  $X$  using Karush–Kuhn–Tucker conditions [41]. Next, we solve

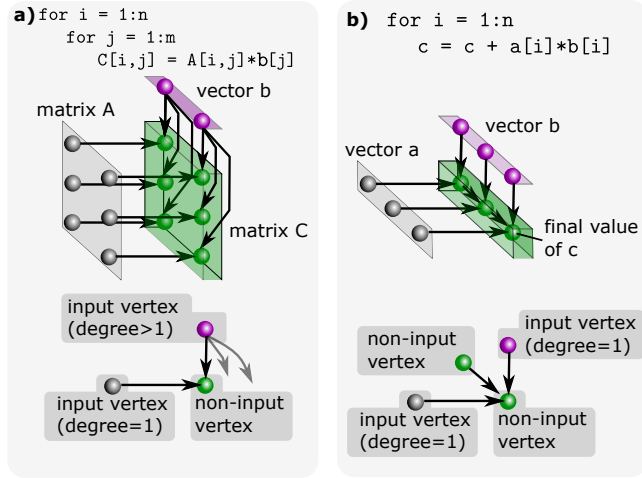
$$\frac{d \psi(X)}{dX} = 0. \quad (4)$$

Denoting  $X_0$  as solution to Equation 4, we finally obtain

$$Q \geq |V| \frac{(X_0 - M)}{\psi(X_0)}. \quad (5)$$

### 3.3 Out-degree-one Vertices

In some cDAGs, every non-input vertex has a certain number  $u \geq 0$  of direct predecessors, which are input vertices with out-degree 1. We can use it to put an additional bound on the computational intensity.



**Figure 2: cDAGs with out-degree 1 input vertices.** a)  $u_a = 1$ ,  $\rho_a \leq 1$ . b)  $u_b = 2$ ,  $\rho_b \leq \frac{1}{2}$ .

**Lemma 6.** *If in a cDAG  $G = (V, E)$  every non-input vertex has at least  $u$  direct predecessors, with out-degree one, which are graph inputs, then the maximum computational intensity  $\rho$  of this cDAG is bounded by  $\rho \leq \frac{1}{u}$ .*

**PROOF.** By the definition of the red-blue pebble game, all inputs start in slow memory, and therefore, have to be loaded. By the assumption on the cDAG, to compute any non-input vertex  $v \in V$ , at least  $u$  input vertices need to have red pebbles placed on them using a load operation. Because these vertices do not have any other direct successors (their out-degree is 1), they cannot be used to compute any other non-input vertex  $w$ . Therefore, each computation of a non-input vertex requires at least  $u$  unique input vertices to be loaded.  $\square$

*Example:* Consider Figure 2. In a), each compute vertex  $C[i, j]$  has two input vertices:  $A[i, j]$  with out-degree 1, and  $b[j]$  with out-degree  $n$ , thus  $u = 1$ . As both array  $A$  and vector  $b$  start in the slow memory (having blue pebbles on each vertex), for each computed vertex from  $C$ , at least one vertex from  $A$  has to be loaded, therefore  $\rho \leq 1$ . In b), each computation needs two out-degree 1 vertices, one from vector  $a$  and one from vector  $b$ , resulting in  $u = 2$ . Thus,  $\rho \leq \frac{1}{2}$ .

**Note.** We use the above lemma to derive the computational intensity of statement S1 in LU factorization (Figure 1).

## 4 DATA REUSE ACROSS MULTIPLE STATEMENTS

Almost all computational kernels contain multiple statements connected by data dependencies — e.g., column update (S1) and trailing matrix update (S2) in LU factorization (Figure 1). In this section we examine how these dependencies influence the total I/O cost of a program.

Consider a program containing two statements  $S$  and  $T$ :

$$\begin{aligned} & \text{for } \gamma^1 \in \Gamma^1, \text{ for } \gamma^2 \in \Gamma_2(\gamma^1), \dots, \text{ for } \gamma^k \in \Gamma_k(\gamma^1, \dots, \gamma^{k-1}) : \\ & \quad S : A_0[\phi_0(\gamma)] \leftarrow f(A_1[\phi_1(\gamma)], A_2[\phi_2(\gamma)], \dots, A_m[\phi_m(\gamma)]) \\ & \text{for } \lambda^1 \in \Lambda^1 : \text{ for } \lambda^2 \in \Lambda^2(\lambda^1), \dots, \text{ for } \lambda^l \in \Lambda^l(\lambda^1, \dots, \lambda^{l-1}) : \\ & \quad T : B_0[\chi_0(\lambda)] \leftarrow g(B_1[\chi_1(\lambda)], B_2[\chi_2(\lambda)], \dots, B_n[\chi_n(\lambda)]) \end{aligned}$$

Denote  $Q_S$  and  $Q_T$  as I/O costs of statements  $S$  and  $T$  if executed separately, and  $Q_{tot}$  a total I/O cost of the above program. Assume that there is at least one array that is accessed both in  $S$  and  $T$ , that is  $\exists i, j : A_i = B_j$ . An I/O optimal schedule could take advantage of it by possibly fusing statements  $S$  and  $T$ : once some vertices of  $A_i$  are loaded, they could be used to compute both  $A_0$  (statement  $S$ ) and  $B_0$  (statement  $T$ ), yielding  $Q_{tot} < Q_S + Q_T$ . However, determining explicitly which loops should be fused to maximize locality is proven to be NP-hard [37]. Therefore, here we focus only on the I/O lower bounds, or, in other words, what is the maximum possible “benefit” of any data reuse between statements.

There are two cases in which the data reuse can occur (Figure 3): **I)** input overlap, where shared arrays are inputs for all statements, **II)** output overlap, where the output array of one statement is the input array of another.

**Case I).** Assume there are  $w$  statements in the program, and there are  $k$  arrays  $A_j$ ,  $j = 1, \dots, k$  which are shared between at least two statements. We still evaluate each statement separately, but we will subtract the upper bound on shared loads  $Q_{tot} \geq \sum_{i=1}^w Q_i - \sum_{j=1}^k |Reuse(A_j)|$ , where  $|Reuse(A_j)|$  is the reuse bound on array  $A_j$  (Section 4.1).

**Case II).** Consider each pair of “producer-consumer” statements  $S$  and  $T$ , that is, the output of  $S$  is the input of  $T$ . The I/O lower bound  $Q_S$  of statement  $S$  does not change due to the reuse. On the other hand, it may invalidate  $Q_T$ , as the dominator set of  $T$  formulated in Section 3.1 may not be minimum — inputs of a statement may not be graph inputs anymore. For each “consumer” statement  $T$  we reevaluate  $Q'_T \leq Q_T$  using Lemma 8. For a program consisting of  $w$  statements connected by the output overlap, we have  $Q_{tot} \geq \sum_{i=1}^w Q'_i$ . Note that for each “producer” statement  $i$ ,  $Q'_i = Q_i$  (output overlap does not change their I/O lower bound).

### 4.1 Case I. Input Reuse and Reuse Size

Consider two statements  $S$  and  $T$ , which share one input array  $A_i$ . Denote  $|A_i(R_S)|$  the total number of accesses to  $A_i$  during the I/O optimal execution of a program that contains only statement  $S$ . Analogously, denote  $|A_i(R_T)|$  for a program containing only  $T$ . Define  $Reuse(A_i)$  as a number of loads from  $A_i$  which are shared between statements.

**Lemma 7.** *The I/O cost of a program containing statements  $S$  and  $T$  which share the input array  $A_i$  is bounded by*

$$Q_{tot} \geq Q_S + Q_T - Reuse(A_i)$$

where  $Q_S, Q_T$  are the I/O costs of a program containing only statement  $S$  or  $T$ , respectively. Furthermore, we have:

$$Reuse(A_i) \leq \min\{|A_i(R_S)|, |A_i(R_T)|\}$$

where  $|A_i(R_S)|$  and  $|A_i(R_T)|$  are the number of accesses to  $A_i$  during the optimal execution of statements  $S$  and  $T$  separately.

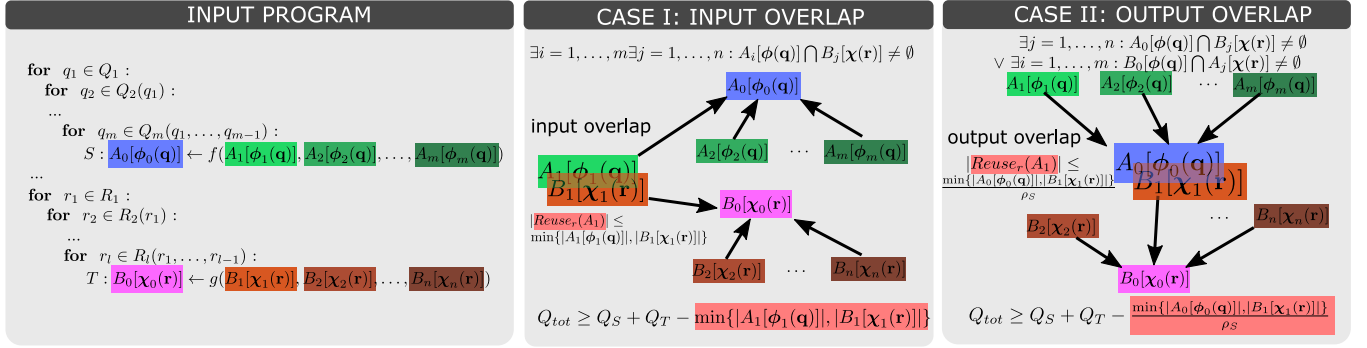


Figure 3: Data reuse across multiple statements.

**PROOF.** Consider an optimal sequential schedule of a cDAG  $G_S$  containing statement  $S$  only. For any subcomputation  $V_S$  and its associated iteration domain  $R_S$  its minimum dominator set is  $Dom(V_S) = \bigcup_{j=1}^m A_j(R_S)$ . To compute  $V_S$ , at least  $\sum_{i=1}^m |A_j(R_S)| - M$  vertices have to be loaded, as only  $M$  vertices can be reused from previous subcomputations.

We seek if any loads can be avoided in the common schedule if we add statement  $T$ , denoting its cDAG  $G_{S+T}$ . Consider a subset  $A_i(R_x)$  of vertices in  $A_i$ .

Consider some subset of vertices in  $A_i$  which potentially could be reused and denote it  $\Theta_i$ . Now denote all vertices in  $A_0$  (statement  $S$ ) which depend on any vertex from  $\Theta_i$  as  $\Theta_S$ , and, analogously, set  $\Theta_T$  for statement  $T$ . Now consider these two subsets  $\Theta_S$  and  $\Theta_T$  separately. If  $\Theta_S$  is computed before  $\Theta_T$ , then it had to load all vertices from  $\Theta_i$ , avoiding no loads compared to the schedule of  $G_S$  only. Now, computation of  $\Theta_T$  may take benefit of some vertices from  $\Theta_i$ , which can still reside in fast memory, avoiding up to  $|\Theta_i|$  loads.

The total number of avoided loads is bounded by the number of loads from  $A_i$  which are shared by both  $S$  and  $T$ . Because statement  $S$  loads at most  $|A_i(R_S)|$  vertices from  $A_i$  during optimal schedule of  $G_S$ , and  $T$  loads at most  $|A_i(R_T)|$  of them for  $G_T$ , the upper bound of shared, and possibly avoided loads is  $Reuse(A_i) = \min\{|A_i(R_S)|, |A_i(R_T)|\}$ .

□

The **reuse size** is defined as  $Reuse(A_i) = \min\{|A_i(R_S)|, |A_i(R_T)|\}$ . Now, how to find  $|A_i(R_S)|$  and  $|A_i(R_T)|$ ?

Observe that  $|A_i(R_S)|$  is a property of  $G_S$ , that is, the cDAG containing statement  $S$  only. Denote the I/O optimal schedule parameters of  $G_S$ :  $V_{max}^S$ ,  $X_0^S$ , and  $|A_i(R_{max}^S(X_0^S))|$  (Section 3.2). Similarly, for  $G_T$ :  $V_{max}^T$ ,  $X_0^T$ , and  $|A_i(R_{max}^T(X_0^T))|$ . We now derive: 1) at least how many subcomputations does the optimal schedule have:  $s \geq \frac{|V|}{|V_{max}^S|}$ , 2) at least how many accesses to  $A_i$  are performed per optimal subcomputation  $|A_i(R_{max}(X_0))|$ . Then:

$$Reuse(A_i) = \min\{|A_i(R_{max}^S(X_0^S))| \frac{|V^S|}{|V_{max}^S|}, |A_i(R_{max}^T(X_0^T))| \frac{|V^T|}{|V_{max}^T|}\} \quad (6)$$

**Example:** Consider the following code:

```

1 for i = 1:N   for j = 1:N   for k = 1:N
2 S : D[i, j, k] = A[i, k] * B[k, j]
3 T : E[i, j, k] = C[i, k] * B[k, j]
4 end; end; end

```

We now derive the I/O lower bound of this program:

(1) **statement S.** Denote  $I_h, J_h, K_h$  as the number of different values iteration variables  $i, j$ , and  $k$  take during the maximal subcomputation  $V_h$ . Then:

- Access sizes (Lemma 3):

$$|V_h^S| = I_h J_h K_h, |A[i, k](R_h^S)| = I_h K_h, |B[k, j](R_h^S)| = K_h J_h$$

- Finding  $\psi(X)$  (Optimization problem 3):

$$|V_h^S| = \left(\frac{X}{2}\right)^2, |A[i, k](R_h^S)| = |B[k, j](R_h^S)| = \left(\frac{X}{2}\right)^2$$

- Finding  $X_0$  (Equation 4):

$$X_0^S = 2M, I_h = J_h = K_h = M, V_h^S = M^2,$$

- Finding the lower bound (Equation 5):

$$\rho_S = M, Q_S = \frac{N^3}{M}$$

(2) **statement T.** Analogous to S

(3) Reuse(B)

$$\frac{|V^S|}{|V_{max}^S|} = \frac{|V^T|}{|V_{max}^T|} = \frac{N^3}{M^2}, |B[k, j](R_{max}^S)| = KJ = M,$$

- Reuse(B) =  $\frac{N^3}{M}$

(4) **I/O lower bound (Lemma 7):**  $Q_{tot} = Q_S + Q_T - Reuse(B) = \frac{N^3}{M}$

**Note:** This bound is attainable by fusing the statements, caching  $M - 1$  elements of matrix  $B$ , and streaming matrices  $A$  and  $C$ .

## 4.2 Case II. Output Reuse and Access Sizes

Consider the case where *output*  $A_0$  of the statement  $S$  is also the *input*  $B_j$  of statement  $T$ . Consider furthermore subcomputation  $V_h$  of statement  $T$  (and its associated iteration domain  $R_h$ ). Any path from the graph inputs to vertices in  $B_0(R_h)$  must pass through vertices in  $B_j(R_h)$ . Now the question is the following: is there a smaller set of vertices  $B'_j(R_h)$ ,  $|B'_j(R_h)| < |B_j(R_h)|$  such that every path from graph inputs to  $B_j(R_h)$  must pass through it?

Denote computational intensity of statement  $S$  as  $\rho_S$ . Then we state the following lemma:

**Lemma 8.** Any dominator set of set  $B_j(R_h)$  must be of size at least  $|Dom(B_j(R_h))| \geq \frac{|B_j(R_h)|}{\rho_S}$ .

PROOF. By Lemma 1, for one loaded vertex, we may compute at most  $\rho_S$  vertices of  $A_0$ . These are also vertices of  $B_j$ . Thus, to compute  $|B_j(\mathbf{R}_h)|$  vertices of  $B_j$ , at least  $\frac{|B_j(\mathbf{R}_h)|}{\rho_S}$  loads must be performed. We just need to show that at least that many vertices have to be in any dominator set  $Dom(B_j(\mathbf{R}_h))$ . Now, consider the converse: There is a vertex set  $D = Dom(B_j(\mathbf{R}_h))$  such that  $|D| < \frac{|B_j(\mathbf{R}_h)|}{\rho_S}$ . But that would mean, that we could potentially compute all  $|B_j(\mathbf{R}_h)|$  vertices by only loading  $|D|$  vertices, violating Lemma 1.  $\square$

**Corollary 1.** *Combining Lemmas 8 and 3, the data access size of  $|B_j(\mathbf{R}_h)|$  during subcomputation  $V_h$  is*

$$|B_j(\mathbf{R}_h)| \geq \frac{\prod_{k=1}^{dim(\phi_j)} |R_{h,j}^k|}{\rho_S}. \quad (7)$$

**Example (Modified Matrix Multiplication [12]):**

```

1  for i = 1:N
2  for j = 1:N
3 S:   A[i, j] = e2π√-1(i-1)(j-1)/N
4     for k = 1:N
5 T:   C[i, j] = A[i, k]*B[k, j] + C[i, j]
6 end; end; end
    
```

Consider the code above. Statement  $S$  does not have any input arrays (we assume that iteration variables  $i$  and  $j$  are always loaded in the registers. Therefore, there are no loads performed during the execution of  $S$ , so  $\rho_S \rightarrow \infty$  for large  $N$ . Statement  $T$ , on the other hand, if executed separately, would perform at least  $Q_T \geq \frac{2N^3}{\sqrt{M}}$  loads. However, using Corollary 1, we obtain access size

$|A_1(\mathbf{R}_h)| \geq \frac{|R_h^i| |R_h^k|}{\rho_S} \geq 0$ , and the combined bound is  $Q_{T+S} \geq \frac{N^3}{M}$ . This bound is tight, as the I/O optimal schedule would cache  $M - 1$  vertices of  $C$ , and for each loaded vertex of  $B$  would compute  $M - 1$  new vertices of  $C$ .

## 5 DERIVING PARALLEL I/O LOWER BOUNDS

We now establish how our method applies to a parallel machine with  $P$  processors (Section 2.1). Each processor  $p_i$  owns its private fast memory which can hold up to  $M$  words, represented in the cDAG as  $M$  red vertices with  $p_i$ 's "hue". Red vertices of different hues (belonging to different processors) cannot be shared between them, but any number of different red pebbles may be placed on one vertex.

All the standard red-blue pebble game rules apply with the following modifications:

- (1) **compute** if all direct predecessors of vertex  $v$  have red pebbles of  $p_i$ 's hue placed on them, one can place a red pebble of  $p_i$ 's hue on  $v$  (no sharing of red pebbles between processors),
- (2) **load** if a vertex  $v$  has *any* pebble placed on them, a red pebble of any other hue may be placed on a vertex.

From this game definition, it follows that from a perspective of a single processor  $p_i$ , any data is either local (the corresponding vertex has  $p_i$ 's red pebble placed on it), or remote, without a distinction on the remote location (remote access cost is uniform).

**Lemma 9.** *The minimum number of I/O operations in a parallel red-blue pebble game, played on a cDAG with  $|V|$  vertices with  $P$  processors each equipped with  $M$  red pebbles, is  $Q \geq \frac{|V|}{P \cdot \rho}$ , where  $\rho$  is the maximum computational intensity independent of  $P$  (Lemma 1).*

PROOF. Following the analysis of Section 3 and the parallel machine model (Section 5), the computational intensity  $\rho$  is independent of a number of parallel processors - it is solely a property of a cDAG and private fast memory size  $M$ . Therefore, following Lemma 1, what changes with  $P$  is the volume of computation  $|V|$ , as now at least one processor will compute at least  $|V_p| = \frac{|V|}{P}$  vertices. By the definition of the computational intensity, the minimum number of I/O operations required to pebble these  $|V_p|$  vertices is  $\frac{|V_p|}{\rho}$ .  $\square$

## 6 BOUNDS OF PARALLEL LU FACTORIZATION

In the previous sections, we have analyzed all components of the LU factorization algorithm (Figure 1) separately. We now provide a full, end-to-end derivation of its parallel I/O lower bound using our method. Previously, Olivry et al. [49] reported a lower bound for a sequential machine  $\frac{2}{3} \frac{N^3}{\sqrt{M}}$ . To the best of our knowledge, this is the first parallel result for this algorithm.

Recall that the algorithm contains two statements:

**S1:**  $\mathbf{A}[\mathbf{i}, \mathbf{k}] = \mathbf{A}[\mathbf{i}, \mathbf{k}] / \mathbf{A}[\mathbf{k}, \mathbf{k}]$

Denote  $|R_h^k| = K_h$ ,  $|R_h^i| = I_h$ . Then, we have the following (Lemma 3):

- $|V_h| = K_h I_h$
- $|A_1(\mathbf{R}_h)| = K_h I_h$ ;  $|A_2(\mathbf{R}_h)| = K_h$
- $|Dom(V_h)| = |A_1(\mathbf{R}_h)| + |A_2(\mathbf{R}_h)| = K_h I_h + K_h$

We then solve the optimization problem from Section 3.2:

$$\begin{aligned} \max \quad & K_h I_h, \quad \text{s.t.} \\ & K_h I_h + K_h \leq X \\ & I_h \geq 1 \\ & K_h \geq 1 \end{aligned}$$

Which gives  $|V_{max}| = \psi(X) = X - 1$  for  $K_h = 1$  and  $I_h = X - 1$ . Then  $\rho(X) = \frac{|V_{max}|}{X - M} = \frac{X - 1}{X - M}$ . However, because  $A_1$  has out-degree 1, we use the bound from Lemma 6:  $\rho_{S1} \leq 1$ . Preserving the correctness of I/O lower bounds, we use its upper bound  $\rho_{S1} = 1$ .

Finally, we calculate total number of vertices in statement **S1**:  $|V_{S1}| = \sum_{k=1}^N (N - k - 1) = \frac{N(N-1)}{2}$  and conclude that  $Q_{S1} \geq \frac{|V_1|}{\rho_1} = \frac{N(N-1)}{2}$  (Lemma 1).

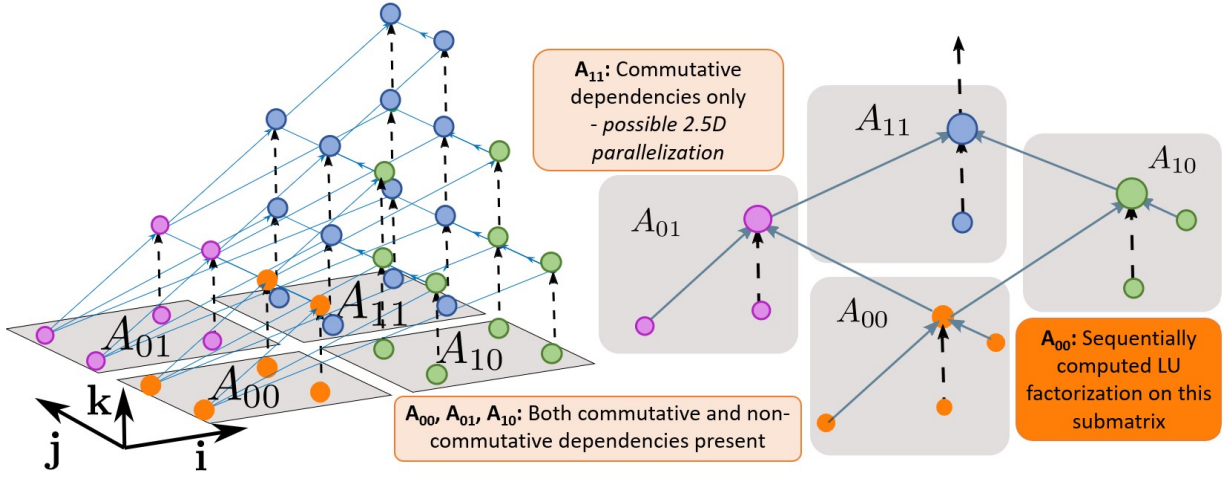
**S2:**  $\mathbf{A}[\mathbf{i}, \mathbf{j}] = \mathbf{A}[\mathbf{i}, \mathbf{j}] - \mathbf{A}[\mathbf{i}, \mathbf{k}] * \mathbf{A}[\mathbf{k}, \mathbf{j}]$

Denote  $|R_h^k| = K_h$ ,  $|R_h^i| = I_h$ ,  $|R_h^j| = J_h$ . Observe that there is an output reuse (Section 4.2) of  $\mathbf{A}[\mathbf{i}, \mathbf{k}]$  between statements **S1** (as  $A_0$ ) and **S2** (as  $A_2$ ). We therefore have the access size in statement **S2**:  $|A_2(\mathbf{R}_{S2})| = \frac{I_h K_h}{\rho_{S1}} = I_h K_h$  (Equation 7). Note that in this case, where the computational intensity is  $\rho_{S1} \leq 1$ , the output reuse does not change the access size  $|A_2(\mathbf{R}_{S2})|$  of statement **S2**. This follows the intuition that it is not beneficial to recompute vertices if the recomputation cost is not lower than loading it from the memory.

The remaining steps of the I/O lower bound analysis are similar to **S1**. We then obtain  $\rho_{S2} = \frac{\sqrt{M}}{2}$ ,  $|V_{S2}| = \frac{N^3}{3} - N^2 + \frac{2N}{3}$  and finally  $Q_{S2} \geq \frac{2N^3 - 6N^2 + 4N}{3\sqrt{M}}$ . The I/O lower bound of the full LU factorization is therefore:

$$Q_{LU} \geq Q_1 + Q_2 \geq \frac{2N^3 - 6N^2 + 4N}{3\sqrt{M}} + \frac{N(N-1)}{2}$$





**Figure 4: LU cDAG for  $n = 4$  together with the logical decomposition to  $A_{00}$ ,  $A_{10}$ ,  $A_{01}$ , and  $A_{11}$ . Dashed arrows represent commutative dependencies (reduction of a value). Solid arrows represent non-commutative operations, so any parallel pebbling has to respect the induced order (e.g., no vertex in  $A_{11}$  can be pebbled before  $A_{00}$  is pebbled).**

Using Lemma 9 we have the parallel I/O lower bound

$$Q_{P,LU} \geq \frac{2N^3 - 6N^2 + 4N}{3P\sqrt{M}} + \frac{N(N-1)}{2p} = \frac{2N^3}{3P\sqrt{M}} + O\left(\frac{N^2}{P}\right),$$

which is one of the main contributions of our work.

## 7 CONfLUX

In this section we present CONfLUX — a near *Communication Optimal LU factorization using X-Partitioning*.

### 7.1 LU Dependencies and Parallelization

Due to the dependency structure of LU, the input matrix is often divided recursively into four submatrices  $A_{00}$ ,  $A_{10}$ ,  $A_{01}$ , and  $A_{11}$  [23, 56]. Arithmetic operations performed in LU create non-commutative dependencies (Figure 4) between vertices in  $A_{00}$  (LU factorization of the top-left corner of the matrix),  $A_{10}$ , and  $A_{01}$  (triangular solve of vertical and top panels of the matrix). Only  $A_{11}$  (Schur complement update) has no such dependencies, and may therefore be efficiently parallelized in the reduction dimension. Our parallel algorithm utilizes this fact and applies different strategies for different parts. Its high-level summary is presented in Algorithm 1.

### 7.2 Computation Routines

The computation is performed in  $\frac{N}{v}$  steps, where  $v$  is a tunable blocking parameter. In each step, only submatrix  $A_t$  of input matrix  $A$  is updated. Initially,  $A_t$  is set to  $A$ .  $A_t$  is further decomposed to four submatrices  $A_{00}$ ,  $A_{10}$ ,  $A_{01}$ , and  $A_{11}$  which are updated by routines *TournPivot*, *FactorizeA<sub>10</sub>*, *FactorizeA<sub>01</sub>*, and *FactorizeA<sub>11</sub>* (see Figure 5):

- $A_{00}$ . This  $v \times v$  submatrix contains first  $v$  elements of current  $v$  pivot rows. It is computed during *TournPivot*, and as it is required to compute  $A_{10}$  and  $A_{01}$ , it is redundantly copied to all processors.
- $A_{10}$  and  $A_{01}$ . Submatrices  $A_{10}$  and  $A_{01}$  of sizes  $(N - t \cdot v) \times v$  and  $v \times (N - t \cdot v)$  are distributed using 1D decomposition among all processors. They are updated using a triangular solve. 1D decomposition guarantees that there are no dependencies between

### Algorithm 1 CONfLUX

---

```

 $A_t \leftarrow A$ 
for  $t = 1, \dots, \frac{N}{v}$  do
  1. Reduce next block column ▷ Cost:  $\frac{(N-t \cdot v) \cdot v \cdot M}{N^2}$ 
  2. TournPivot( $A_t$ ) ▷ Cost:  $v^2 \left[ \log\left(\frac{N}{\sqrt{M}}\right) \right]$ 
  3. Scatter computed  $A_{00}$  and  $v$  pivot rows ▷ Cost:  $v^2 + v$ 
  4. Scatter  $A_{10}$  ▷ Cost:  $\frac{(N-t \cdot v)v}{p}$ 
  5. Reduce  $v$  pivot rows ▷ Cost:  $\frac{(N-t \cdot v) \cdot v \cdot M}{N^2}$ 
  6. Scatter  $A_{01}$  ▷ Cost:  $\frac{(N-t \cdot v)v}{p}$ 
  7. FactorizeA10( $A_t$ ) ▷ 1D parallel, block-row
  8. Send data from panel  $A_{10}$  ▷ Cost:  $\frac{(N-t \cdot v)N \cdot v}{P\sqrt{M}}$ 
  9. FactorizeA01( $A_t$ ) ▷ 1D parallel, block-column
  10. Send data from panel  $A_{01}$  ▷ Cost:  $\frac{(N-t \cdot v)N \cdot v}{P\sqrt{M}}$ 
  11. FactorizeA11( $A_t$ ) ▷ 2.5D parallel
   $A_t \leftarrow A_t[\text{rows}, v : \text{end}]$ 
end for

```

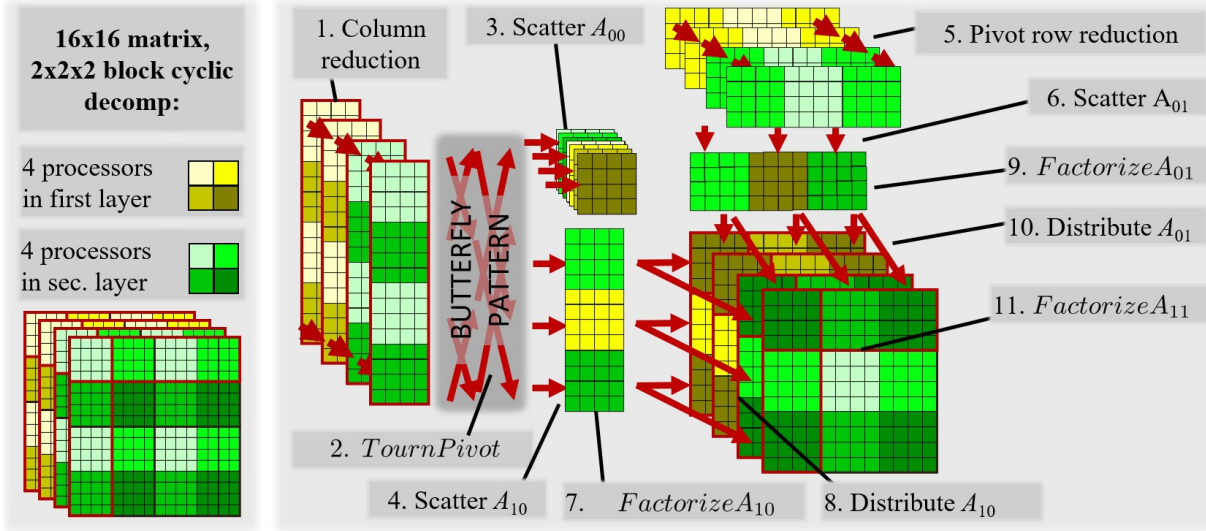
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- processors, so no communication or synchronization is performed during computation ( $A_{00}$  is already owned by every processor).
- $A_{11}$  This  $(N - t \cdot v) \times (N - t \cdot v)$  submatrix is distributed using 2.5D, block-cyclic distribution (Figure 5). First, updated submatrices  $A_{10}$  and  $A_{01}$  are broadcast among the processes. Then,  $A_{11}$  (Schur complement) is updated. Finally, the first block column and  $v$  chosen pivot rows are reduced, which will form  $A_{10}$  and  $A_{01}$  in the next iteration.

**Blocking parameter  $v$ .** The minimum size of each block is the number of processor layers in the reduction dimension  $v \geq c = \frac{PM}{N^2}$ . However, to secure high performance, this value should also be adjusted to hardware parameters of a given machine (e.g., vector length, prefetch distance of a CPU, or warp size of a GPU). Throughout the analysis, we assume that  $v = a \cdot \frac{PM}{N^2}$  for some small constant  $a$ .

### 7.3 Pivoting

Our pivoting strategy differs from state-of-the-art block [4], tile [3], or recursive [24] pivoting approaches in two aspects:



**Figure 5: COntLUX parallel decomposition for  $P = 8$  processors decomposed into  $2 \times 2 \times 2$  grid, together with indicated steps of Algorithm 1.**

- To minimize I/O, we do not swap pivot rows. Instead, we keep track which rows were chosen as pivots and we use masks to update remaining rows.
- To reduce latency, we take advantage of our derived blocks and use tournament pivoting [29].

The tournament pivoting finds  $v$  pivot rows in each step, which are then used to mask which rows will form the new  $A_{01}$  and then filter the non-processed row in the next step.

**Tournament Pivoting** is shown to be as stable as partial pivoting [29], which might be an issue for, e.g., incremental pivoting [50]. On the other hand, it reduces the  $O(N)$  latency cost of the partial pivoting, which requires step-by-step column reduction to find consecutive pivots, to  $O(\frac{N}{v})$ , where  $v$  is the tunable block size parameter.

**Row Swapping vs. Row Masking.** To achieve close to optimal I/O cost, we use 2.5D decomposition. This, however, implies that in the presence of extra memory, the matrix data is replicated  $\frac{PM}{N^2}$  times. This increases the row swapping cost from  $O(\frac{N^2}{P})$  to  $O(\frac{N^3}{P\sqrt{M}})$  which asymptotically matches the I/O lower bound of the entire factorization. Performing row swapping would then increase the constant term of the leading factor of the algorithm from  $\frac{N^3}{P\sqrt{M}}$  to  $\frac{2N^3}{P\sqrt{M}}$ . To keep the I/O cost of our algorithm as low as possible, instead of performing row-swapping, we only propagate pivot row indices. When the tournament pivoting finds the  $v$  pivot rows, they are broadcast to all processors with only  $v$  cost per step.

**Pivoting in COntLUX.** In each step  $t$  of the outer loop (line 1 in Algorithm 1),  $\frac{N}{\sqrt{M}}$  processors perform a tournament pivoting routine using a butterfly communication pattern [51]. Each processor owns  $\sqrt{M}\frac{N-vt}{N}$  rows, among which it chooses  $v$  local candidate pivots. Then, final pivots are chosen in  $\log(\frac{N}{\sqrt{M}})$  of “playoff-like” tournament rounds, after which all  $\frac{N}{\sqrt{M}}$  processors own both  $v$  pivot row indices and already factored new  $A_{00}$ . This result is distributed

to all remaining processors (line 2). Pivot row indices are then used to determine which processors participate in the reduction of current  $A_{01}$  (line 4). Then, the new  $A_t$  is formed by masking currently chosen rows  $A_t \leftarrow A_t[\text{rows}, v : \text{end}]$  (Line 12).

#### 7.4 I/O cost of COntLUX

We now prove the I/O cost of COntLUX, which is only a factor of  $\frac{1}{3}$  higher than the lower bound for large  $N$ .









**Lemma 10.** *The total I/O cost of COntLUX, presented in Algorithm 1, is  $Q_{\text{COntLUX}} = \frac{N^3}{P\sqrt{M}} + O\left(\frac{N^2}{P}\right)$ .*

**PROOF.** We assume that the input matrix  $A$  is already distributed in the block cyclic layout imposed by the algorithm. Otherwise, any data reshuffling imposes only a  $\Omega(\frac{N^2}{P})$  cost, which does not contribute to the leading order term. We first derive the cost of a single iteration  $t$  of the main loop of the algorithm, proving its cost to be  $Q_{\text{step}}(t) = \frac{2Nv(N-tv)}{P\sqrt{M}} + O\left(\frac{Nv}{P}\right)$ . Then, the total cost after  $\frac{N}{v}$  iterations is:

$$Q_{\text{COntLUX}} = \sum_{t=1}^{\frac{N}{v}} Q_{\text{step}}(t) = \frac{N^3}{P\sqrt{M}} + O\left(\frac{N^2}{P}\right).$$

We denote  $P1 = \frac{N^2}{M}$  and  $c = \frac{PM}{N^2}$ .  $P$  processors are decomposed in the 3D grid  $[\sqrt{P1}, \sqrt{P1}, c]$ . We refer to all processors which share the same second and third coordinate as  $[:, j, k]$ . We now examine each of 11 steps of Algorithm 2.

**Step 1.**  $[:, t \bmod \sqrt{P1}, t \bmod c]$  processors perform the tournament pivoting. Every processor owns first  $v$  elements of  $N - (t-1)v$  rows, among which they choose the next  $v$  pivots. First, they locally perform the LUP decomposition to choose local  $v$  candidate rows. Then, in  $\lceil \log_2(\sqrt{P1}) \rceil$  rounds they exchange  $v \times v$  blocks to decide on the final pivots. After the exchange, these processors also hold the factorized submatrix  $A_{00}$ . *I/O cost per proc.:*  $v^2 \lceil \log_2(\sqrt{P1}) \rceil$ .

	LibSci	SLATE	CANDMC	CONfLUX
<b>Decomposition</b>	2D, panel decomp.	2D, block decomp.	Nested 2.5D, block decomp.	1D / 2.5D, block decomp.
<b>Block size</b>	 user-specified	 user-specified, (default 16)	 $\frac{N^3}{P \cdot M} \cdot \frac{N^2}{P \sqrt{M}}$	 tunable, $\geq \frac{P \cdot M}{N^2}$
<b>User param. required</b>	yes 	no 	no 	no 
<b>Parallel I/O cost</b>	$\frac{N^2}{\sqrt{P}} + O\left(\frac{N^2}{P}\right)$	$\frac{N^2}{\sqrt{P}} + O\left(\frac{N^2}{P}\right)$	$\frac{5N^3}{P\sqrt{M}} + O\left(\frac{N^2}{P\sqrt{M}}\right)$ [56]	$\frac{N^3}{P\sqrt{M}} + O\left(\frac{N^2}{P\sqrt{M}}\right)$
<b>Total comm. volume for <math>N = 4,096</math> measured/modeled [GB] (prediction %)</b>				
$P = 64$	1.17 / 1.21 (102%)	1.18 / 1.21 (102%)	2.5 / 4.9 (196%)	1.11 / 1.08 (97%)
$P = 1,024$	4.45 / 4.43 (99%)	4.35 / 4.43 (102%)	9.3 / 12.13 (130%)	3.13 / 3.07 (98%)
<b>Total comm. volume for <math>N = 16,384</math> measured/modeled [GB] (prediction %)</b>				
$P = 64$	18.79 / 19.33 (103%)	18.84 / 19.33 (102%)	39.8 / 78.74 (197%)	17.61 / 17.19 (98%)
$P = 1,024$	70.91 / 70.87 (99.9%)	71.1 / 70.87 (99.7%)	144 / 194.09 (135%)	45.42 / 44.77 (98%)

**Table 2:** Classification and I/O cost models of the measured LU factorization implementations. CANDMC model is taken from the authors [56]. Due to the space constraints, we omit the lower order terms of the models.

**Steps 2, 3, 5.** Factorized  $A_{00}$  and  $v$  pivot row indices are broadcast. First  $v$  columns and  $v$  pivot rows are scattered to all  $P$ . *I/O cost per proc.:*  $v^2 + v + \frac{2(N-tv)v}{P}$ .

**Steps 4 and 11.** Reduce  $v$  columns and  $v$  pivot rows. With high probability, pivots are evenly distributed among all processors. There are  $c$  layers to reduce, each of size  $(N-tv)v$ . *I/O cost per proc.:*  $\frac{(N-tv)vc}{P} = \frac{2(N-tv)vM}{N^2}$ .

**Steps 6, 8, 10.** The updates  $FactorizeA_{10}$ ,  $FactorizeA_{01}$ , and  $FactorizeA_{11}$  are local and incur no additional I/O cost.

**Steps 7 and 9.** Factorized  $A_{10}$  and  $A_{01}$  are scattered among all processors. Each processor requires  $\frac{v(N-tv)}{c\sqrt{P1}}$  elements from  $A_{10}$  and  $A_{10}$ . *I/O cost per proc.:*  $\frac{2(N-tv)Nv}{P\sqrt{M}}$ .

Summing steps 1-11:  $Q_{step}(t) = \frac{2Nv(N-tv)}{P\sqrt{M}} + O\left(\frac{Nv}{P}\right)$ .  $\square$

## 8 EXPERIMENTAL EVALUATION

We implement CONfLUX and compare it with state-of-the-art implementations of distributed LU factorization. We measure their I/O complexity by counting their aggregated communication volume in distributed runs. We provide both measured values and theoretical cost models, on a variety of problem sizes and number of nodes based on scientific computing applications.

**Implementation.** We implement CONfLUX in C++ using MPI one-sided [31] for inter-node communication. To secure the best performance for all combinations of processor counts and matrix sizes, we use Processor Grid Optimization [42], which finds the 3D processor grid with the lowest communication cost by possibly disabling a minor fraction of nodes. Other implementations, which greedily try to utilize all resources, often find communication-suboptimal decompositions for difficult-to-factorize number of ranks.

**Infrastructure and Measurement.** We run our experiments on the CSCS Piz Daint supercomputer, which comprises 5,704 XC50 nodes equipped with Intel Xeon E5-2690 v3 processors (12 cores, 64 GiB DDR3 RAM), interconnected by the Cray Aries network with a Dragonfly network topology. To measure communication volume, we instrument the implementations with the Score-P library [39] and count the aggregate bytes sent over the network.

**Comparison Targets.** For comparison, we use 1) the vendor-optimized ScaLAPACK implementation on Piz Daint (Cray LibSci v19.06.1). While the library is proprietary, our measurements reaffirm that,

like ScaLAPACK, the implementation uses the suboptimal 2D processor decomposition; 2) SLATE [28] – a state-of-the-art distributed linear algebra framework targeted at exascale supercomputers; 3) the latest version of the CANDMC library [54], which uses the asymptotically-optimal 2.5D decomposition. The implementations and their characteristics are listed in Table 2.

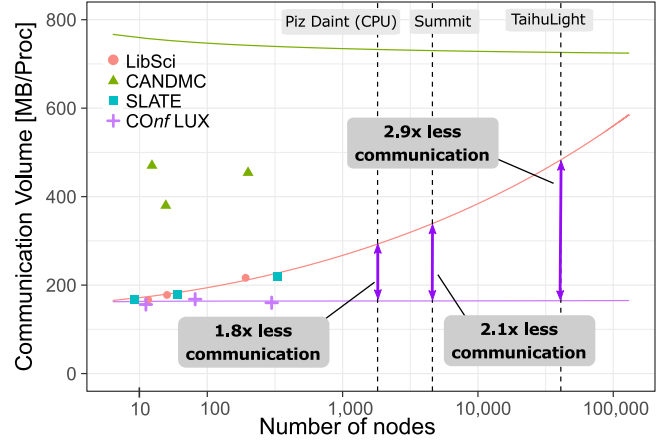
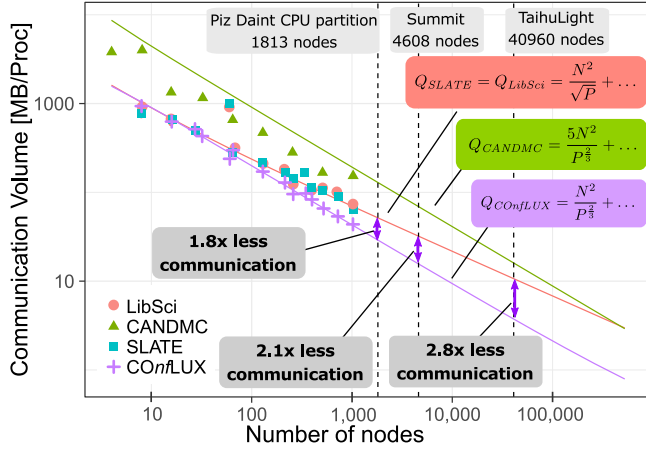
**Problem Sizes.** We choose our benchmarks to reflect problems in scientific computing. Specifically, we choose  $4,096 \leq N \leq 16,384$ . For example, Physical Chemistry or Density Functional Theory (DFT) simulations require factorizing matrices of atom interactions, yielding sizes of  $N \geq 10,000$  [65]. For node count, we measure the algorithms starting from small square and cube nodes ( $P = 4, 8$ ) up to  $P = 1,024$ , reflecting different scales for various use-cases. In other domains, matrix sizes can be larger – the High-Performance Linpack benchmark uses a maximal size of  $N = 16,473,600$  [60], and in quantum physics matrix size scales with  $2^{\text{qubits}}$ . Therefore, we extrapolate our models to match these problem sizes and the number of processors on the current top supercomputers (Summit, TaihuLight) and show predicted communication results.

**Theoretical Models.** Together with empirical measurements, we put significant effort into understanding the underlying communication patterns of the compared LU factorization implementations. Both LibSci and SLATE base on the standard partial pivoting algorithm using the 2D decomposition [9]. For CANDMC, we use the model provided by the authors [56]. For CONfLUX, we use the results from Section 7. These models are summarized in Table 2.

## 9 RESULTS

Our experiments confirm a clear advantage of CONfLUX in terms of communication volume over all other implementations tested. Not only do the measured values exhibit a significant communication reduction (1.42 times compared with the second-best implementation for  $P = 1,024$ ), but the performance models predict even greater benefits for larger runs (expected 2.1 times communication reduction for a full-machine run on the Summit supercomputer).

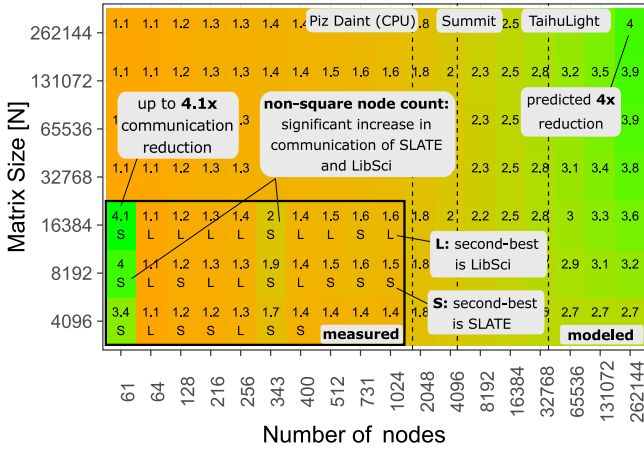
**Scaling Experiments.** Fig. 6a presents the measured communication volume per node, as well as our derived cost models (Table 2) presented with solid lines, for  $N = 16,384$ . Observe that CONfLUX communicates the least for all values of  $P$ . Furthermore, thanks to the Processor Grid Optimization, it always finds the best processor grid given available resources, resulting in smooth and predictable performance. Other implementations try to aggressively use all



(a) Communication volume per node for varying node counts  $P$  and a fixed  $N = 16,384$ . Only the leading factors of the models are shown. The models are scaled by the element size (8 bytes).

(b) Communication volume per node for weak scaling (constant work per node),  $N = 3200 \cdot \sqrt[3]{P}$ . 2.5D algorithms (CANDMC and CONfLUX) retain constant communication volume per processor.

**Figure 6:** Communication volume measurements across different scenarios for LibSci, SLATE, CANDMC, and CONfLUX. In all considered scenarios, enough memory  $M \geq \frac{N^2}{P^{2/3}}$  was present to allow the maximum number of replications  $c = P^{1/3}$ .



**Figure 7:** Communication reduction vs. second-best algorithm (L=LibSci, S=SLATE), for varying  $P, N$ , for both measured and predicted scenarios.

available resources, which leads to suboptimal performance and visible outliers with highly increased communication, as seen in the inset. Note that since both LibSci and SLATE use similar 2D decomposition, their communication volumes are mostly equal, with a slight advantage of SLATE for non-square processor grids. In Fig. 6b, we show the weak scaling characteristics of the analyzed implementations. Observe that for a fixed work per node, the 2D algorithms - LibSci and SLATE - scale sub-optimally.

**Implications for Exascale.** Figure 7 summarizes the communication volume reduction of CONfLUX compared with the second-best implementation, both for measurements and theoretical predictions. It can be seen that in all combinations of  $P$  and  $N$ , CONfLUX always communicates less. For all measured data points, the asymptotically optimal CANDMC performed worse than LibSci or SLATE. The

figure also presents the predicted communication cost of all considered implementations for up to  $P = 262,144$ , based on our theoretical models. Considering the use of one (MPI) process per socket and/or accelerator of each node, such scales will be attainable in the near future. Observe that (a) the asymptotically optimal CANDMC is predicted to communicate less than suboptimal 2D implementations only for  $P > 450,000$  ranks for  $N = 16,384$ , showing that asymptotic optimality is not enough to secure practical performance; and (b) for a full-scale run on Summit, CONfLUX is expected to communicate 2.1 times less than SLATE, a library designed specifically for such machines.

## 10 RELATED WORK

Data movement analysis, while being prevalent for decades, has branched in multiple directions. In summary, previous work can be categorized into three classes (see Table 3): (1) work based on direct pebbling or variants of it, such as Vitter’s block-based model [63]; (2) works using geometric arguments of projections based on the Loomis Whitney inequality [44]; and (3) works applying optimizations limited to specific structural properties of computations such as affine loops [27], and more generally, the polyhedral model program representation [8, 45, 49]. Although the scopes of those approaches significantly overlap – for example, kernels like matrix multiplication can be captured by most of the models – there are still important differences both in methodology and end-results they provide, as summarized in Table 3.

Dense linear algebra operators are among the standard core kernels in scientific applications. Ballard et al. [7] present a comprehensive overview of their asymptotic I/O lower bounds and I/O minimizing schedules, both for sparse and dense matrices. Recently, Olivry et al. introduced IOLB [49] – an automated framework for assessing sequential lower bounds for polyhedral programs. However, their computational model disallows recomputation, and therefore cannot capture programs like the one presented in Section 4.2.

	Pebbling [11, 25, 36, 42, 52]	Projection-based [7, 13, 18, 20, 22, 49]	Problem specific [1, 8, 15, 45, 65]
<b>Scope</b>	👍👍 General cDAGs	👍 Programs with static geometric structure of iteration space	👎 Individually tailored for given problem
<b>Key Features</b>	<ul style="list-style-type: none"> <li>👍 General scope - can handle irregular program structures</li> <li>👍 Expresses complex data dependencies</li> <li>👍 Directly exposes schedules</li> <li>👍 Intuitive</li> <li>👎 P-SPACE complete in general case</li> <li>👎 No guarantees that a solution exists</li> <li>👎 No well-established method how to automatically translate code to cDAGs</li> </ul>	<ul style="list-style-type: none"> <li>👍 Well-developed theory and tools</li> <li>👍 Guaranteed to find solution for given class of programs</li> <li>👎 Bounds are often not tight</li> <li>👎 Fails to capture dependencies between statements</li> <li>👎 Limited scope</li> </ul>	<ul style="list-style-type: none"> <li>👍 Takes advantage of problem-specific features</li> <li>👍 Tends to provide best practical results</li> <li>👎 Requires large manual effort for each algorithm separately</li> <li>👎 Difficult to generalize</li> <li>👎 Often based on heuristics with no guarantees on optimality</li> </ul>

Table 3: Overview of different approaches to modeling data movement.

As such, linear solvers are implemented in various libraries for shared-memory environments [3, 4, 19, 30, 33, 47, 59]. For distributed memory, vendor-optimized libraries [14, 33] typically implement the ScaLAPACK interface [9], and are based on 2D decomposition, as we empirically verify (Section 8). On the algorithmic side, research is conducted into implementing communication-avoiding solvers with 2.5D [55, 56], and 3D decomposition [5, 32] strategies. For heterogeneous hardware (e.g., GPU-accelerated) systems, recent frameworks focus on implementing modified interfaces for asynchronous offloading [10], and fine-grained task parallelism [2, 28].

## 11 CONCLUSIONS

In this work, we present a novel method of analyzing DAAP — a general class of programs that covers many fundamental computational motifs. We show, both theoretically and in practice, that our pebbling-based approach for deriving the I/O lower bounds is **more general**: programs with disjoint array accesses cover a wide variety of applications, **more powerful**: it can explicitly capture inter-statement dependencies, **more precise**: it derives tighter I/O bounds, and **more constructive**:  $X$ -partition provides powerful hints for obtaining parallel schedules.

When applying the approach to LU factorization, we were able to derive new lower bounds, as well as the  $CONfLUX$  schedule. Not only is  $CONfLUX$  asymptotically optimal, but we also see that in practice, the reduction in the leading term yields communication volumes that are better than state-of-the-art 2D and 3D decomposition, by a factor of up to 4.1 $\times$ . This promising result mandates the exploration of the parallel pebbling strategy to algorithms such as Cholesky factorization, other nontrivial dense linear algebra kernels, and beyond.

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